FPGA-based System for In-Line Measurement of Velocity Profiles of Fluids in Industrial Pipe Flow

FPGA-Based System for In-Line Measurement of Velocity Profiles of Fluids in Industrial Pipe Flow

Stefano Ricci, *Senior Member, IEEE*, Valentino Meacci, *Student Member, IEEE*,
Beat Birkhofer, Johan Wiklund

Abstract—The rheology of a fluid flowing in an industrial process pipe can be calculated by combining the pressure drop and the velocity profile that the fluid develops across the tube diameter. The profile is obtained non-invasively through an ultrasound Doppler investigation. Unfortunately, at present, no system capable of real-time velocity profile assessment is available for in-line industrial rheological measurements, and tests are operated by manually moving fluid specimens to specialized laboratories. In this work we present an embedded system capable of in-line and real-time measurement of velocity profile and pressure drop, which enables the automatic rheological characterization of non-Newtonian fluids in process pipes. The system includes all the electronics for the ultrasound front-end, as well as the digital devices for the real-time calculation of the velocity profile. The proposed system is high programmable, low-noise and specifically targeted for industrial use. It is shown capable of producing, for example, 512-point velocity profiles at 45 Hz rate. An application is presented where a sludge fluid, flowing at 600 L/min in a 48 mm diameter high-grade stainless steel pipe, is characterized in real-time with a ±5% accuracy.

Index Terms— Fluid flow control, Fluid flow measurement, Doppler measurement, Fluid characterization

I. INTRODUCTION

IN chemical, pharmaceutical and food industries the final product is obtained through several manufacturing processes that involve different fluids and suspensions. An accurate monitoring of the characteristics of such fluids during the production is of paramount importance for ensuring the quality of the final product [1]. While parameters like temperature and pressure are easily acquired in-line with simple sensors, the measurement of rheological data, like the fluid viscosity, presents several challenges. Currently, fluid specimens are manually extracted from the production chain, moved to laboratory, and analyzed off-line by rotational rheometers. This procedure is time consuming, only part of the fluid is monitored, and the result is not available in real-time. Moreover, this manual procedure is not compatible with the computerized and automatic process control of the industry. A few in-line rheometers have been tested for a small number of applications, but since they are typically able to determine the viscosity only for a single shear rate, their success was limited.

Rheological parameters of a fluid flowing in a process pipe can be obtained in-line by measuring the pressure drop between 2 points at known distance, and the velocity profile that the fluid develops along the diameter [2]. The velocity profile can be acquired through nuclear magnetic resonance or laser velocimetry [2][3], but the equipment is expensive, cumbersome, needs windows and/or modification of the pipe, and, moreover, laser light does not penetrate opaque fluids.

Ultrasound techniques have been playing an important role in the monitoring of industrial fluids for long time [4]. Among these techniques, the Pulsed Ultrasound Velocimetry (PUV) method allows the assessment of the velocity profile, and thus represents an attractive alternative for rheological measurements. Although the PUV method is known for industrial applications since the 1980s [5], the few available industrial instruments that exploit PUV are limited to simple acquisition boards without computational capability. They should be connected to a centralized host computer where the velocity profile is calculated out-of-line, and do not support a real-time, continuous monitoring of the fluid.

Embedding the calculation of the velocity profile in the board represents a necessary step towards a compact industrial instrument with real-time capability. Unfortunately, the velocity profile calculation includes high-demanding steps, like coherent demodulation, data reordering, spectral analysis, filtering, etc. that require devices capable of moving and processing large quantities of data in limited temporal slots. Field Programmable Gate Arrays (FPGAs) [6] offer a wide calculation power at low cost, and are nowadays employed in several industrial systems [7], including ultrasound apparatuses [8] and flow-control instruments [9].

In this work we present a compact, fully programmable and

S. Ricci (corresponding author) and V. Meacci are with the Information Engineering Department, University of Florence, Florence, Italy. (e-mail: stefano.ricci@unifi.it; valentino.meacci@unifi.it). B. Birkhofer is with Sika Services AG, Zurich, Switzerland (e-mail: beat@birkhofer.ch). J. Wiklund is with the Soft Materials Science Department of SP Technical Research Institute of Sweden, Göteborg, Sweden, (e-mail: johan.wiklund@sp.se)
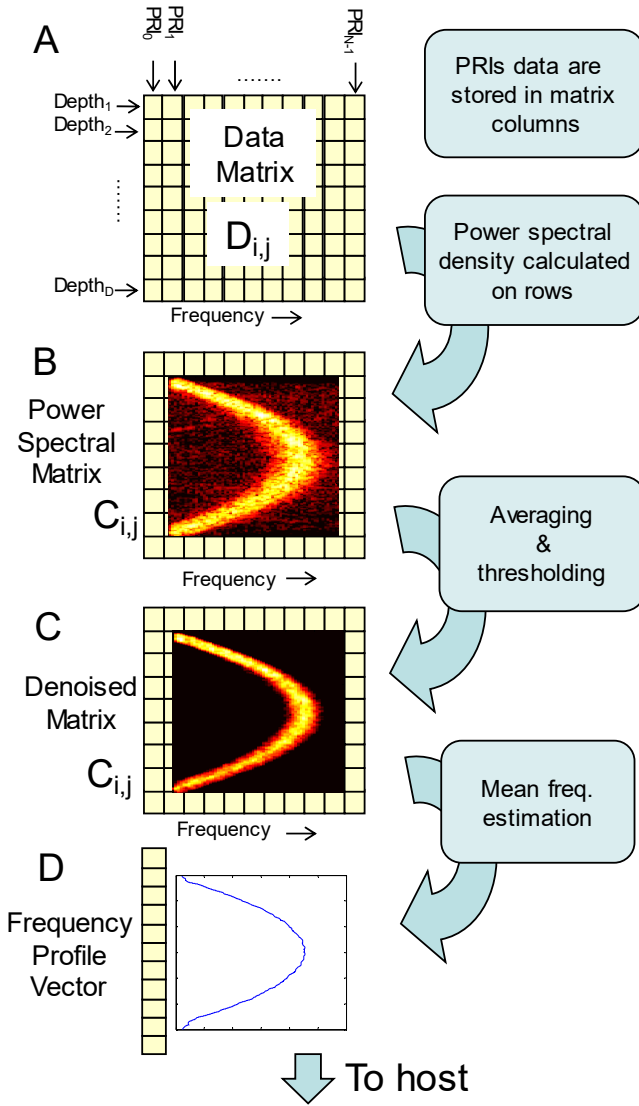
Fig. 1. Basic steps for calculating the power Doppler spectral matrix. Data acquired from each PRI are demodulated and arranged in the columns of a data matrix (A). Every row is processed through windowing, FFT and power extraction. The matrix, color coded, produces an intuitive graphical representation of the frequency profile (B). The noise is filtered by applying a threshold (C). The frequency profile vector (D) is finally obtained by calculating a power-weighted mean of each row of the denoised matrix.

low cost PUV system that includes all the electronics for generating/receiving the ultrasound bursts, and exploits an FPGA for calculating the flow velocity profile in-line and in real-time. It represents the latest generation of a sequence of research tools that starts with a multigate board initially dedicated to biomedical applications [10][11], followed by a first prototype adapted to industrial use [12]. The new PUV system has been successfully integrated as part of the patented Flow-Viz™ instrument (SP, Sweden) [13].

The paper is organized as follows: the theoretical basics are summarized in Sec. II, the electronics is described in Sec. III, while Sec. IV details the FPGA implementation. Noise and accuracy characterization, and a complete measurement on an industrial fluid, are reported in Sec. V.

II. METHOD

A. Velocity profile detection through ultrasound

Every pulse repetition interval (PRI) an ultrasound burst, typically constituted by 3 to 10 sinusoidal cycles at $f_t = 0.2 - 10$ MHz frequency, is transmitted, and propagates in the fluid with velocity c. A particle moving at velocity v in axial direction generates an echo whose frequency, according to the Doppler effect, is affected by the shift:

$$f_D = 2f_t \frac{v}{c} \cos(\delta) \qquad (1)$$

where δ is the angle between the direction of the moving particle and the ultrasound beam [14].

Every PRI, the received echoes are sampled, demodulated in in-phase and quadrature components (I/Q) by multiplying the samples by $\sin(2\pi f_i t)$ and $\cos(2\pi f_i t)$, and low-pass filtered. The complex samples are stored along the columns of a matrix. Adjacent columns, (from left to right Fig.1, A), collect data corresponding to successive PRIs. The sample frequency is typically between 40 and 100 MHz and about 500 to 8000 samples per PRI are collected.

When the matrix holds enough data (e.g. 128 or 256 columns), the spectral analysis starts. Every row of the matrix, which stores the samples corresponding to the same depth, is processed through windowing, FFT, and power extraction. The resulting spectral matrix is color-coded and displayed. It shows an intuitive representation of the velocity profile of the fluid (Fig.1, B), similar to that used in biomedical echography when investigating blood [11].

The background noise is reduced by applying a threshold to the spectral matrix (Fig.1, C), and, from each row of the denoised data, the Doppler shift f_D at depth d is calculated:

$$f_{Dd} = \frac{1}{\text{PRI}} \frac{n_d}{N} \quad \text{where} \quad n_d = \sum_{i=0}^{N-1} i \cdot |C_{d,i}|^2 \Big/ \sum_{i=0}^{N-1} |C_{d,i}|^2 \qquad (2)$$

$C_{d,i}$ is the matrix element corresponding to depth d and FFT bin i, and N is the number of frequency bins. The flow velocity is finally obtained by substituting f_{Dd} in (1) for all of the n depths. An example of flow profile is shown in Fig.1, D.

B. Basics of rheology assessment

The method employed for the rheology characterization of a fluid can be found in [2][18][19][20]. It is summarized here for reader's convenience. The first step is the measurement of the pressure drop ΔP over a distance L along the pipe of radius R; and the fluid velocity distribution in radial direction $v(r)$, where r is the distance from the pipe center ($0 < r < R$). The shear stress $\tau(r)$, linear in r, has its maximum at the wall and is null in the pipe center [2]:

$$\tau(r) = \frac{\Delta P \cdot r}{2 \cdot L \cdot R} \qquad (3)$$

The shear rate $\dot{\gamma}$ along the radius r is obtained as the derivative of the flow velocity $v(r)$.

$$\dot{\gamma}(r) = -\frac{dv(r)}{dr} \qquad (4)$$
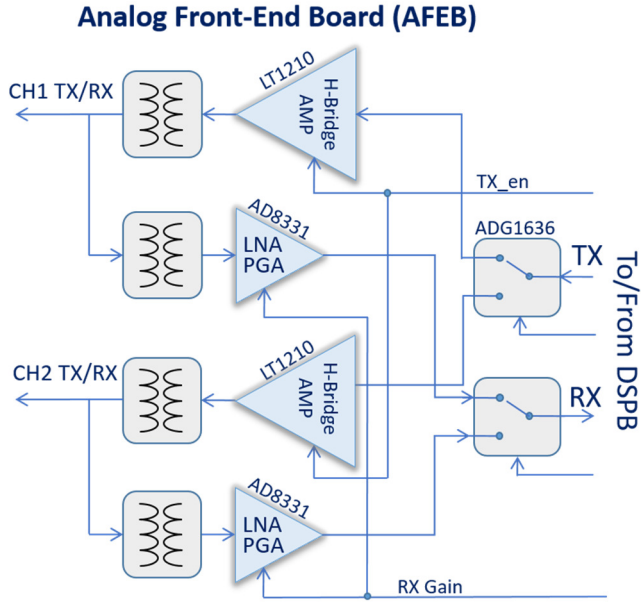
Analog Front-End Board (AFEB)

Fig. 2. The AFEB includes the linear power amplifiers and the LNAs/PGAs for 2 TX/RX channels. The multiplexers select the TX and RX channels, which are connected to the DSPB.
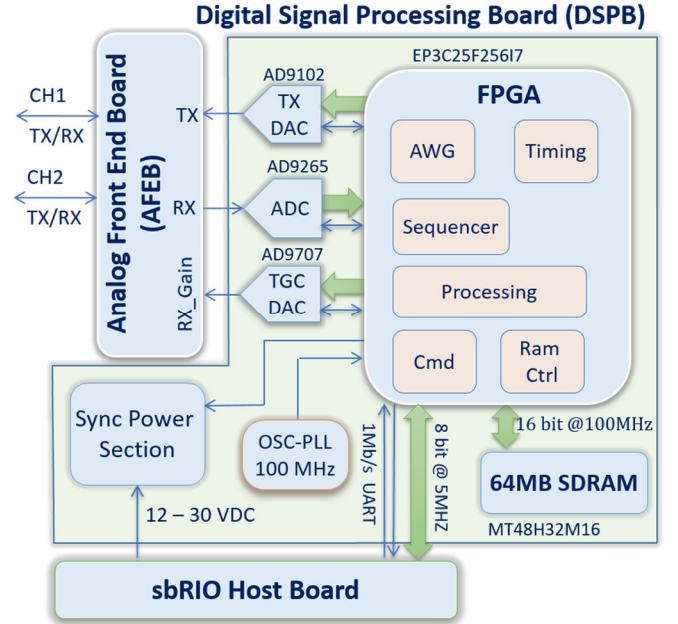
Digital Signal Processing Board (DSPB)

Fig. 3. The DSPB hosts the analog-to-digital and digital-to-analog converters, the FPGA, the SDRAM for data processing, the power section, and the clock generator. It is connected to the AFEB and the sbRIO host board.

By combining the previous equations, the shear rate dependent viscosity, η, is finally calculated:

$$\eta(r) = \frac{\tau(r)}{\dot{\gamma}(r)} \qquad (5)$$

The viscosity η is simultaneously evaluated for the range of shear rate values present in the investigated flow profile, i.e. from $\dot{\gamma}(r)|_{r=0} = 0$ at pipe centre, to the maximum value at the wall position $(\dot{\gamma}(r)|_{r=R})$. In case of yield stress fluids, the yield stress τ_0 can be determined from the radial extension of the plug region, i.e. the plug radius R^* measured from the flow velocity profile:

$$\tau_0 = \frac{\Delta P \cdot R^*}{2 \cdot L} \qquad (6)$$

III. THE PUV SYSTEM

A. The Electronics

The system is constituted by 2 electronic boards: the Analog Front-End Board (AFEB) and the Digital Signal Processing Board (DSPB). The AFEB is located on top of the DSPB, so that the overall dimensions are limited to 10×12 cm. Two transmit (TX) and two receive (RX) channels are available on the system, which can be connected to two separate ultrasound transducers. Although the 2 channels cannot be simultaneously active, this configuration allows the dynamic switching between pitch-catch and single transducer operations. The PUV system is connected to a host, namely an sbRIO 9607 board from National Instruments (Austin, TX). The host configures the system, commands the start of operations, and downloads the measurements. The main features are listed in Tab. I.

B. The Analog Front-End Board (AFEB)

The AFEB is detailed in Fig. 2. It includes a complete ultrasound front-end where the TX/RX ultrasound pulses are analog conditioned. During the transmission phase, the differential TX signal, synthetized in the DSPB, is forwarded to the active TX channel (CH1 or CH2 in Fig. 2) through an analog multiplexer controlled by the DSPB. The signal is then processed by a power amplifier realized by 2 linear differential amplifiers with current feedback (LT1210 from Analog Device, Norwood, MA) connected in an H-bridge configuration. Each pairs of amplifiers features a low impedance output that can reach 30 Vpp. It is applied to a transformer that raises the voltage up to 80 Vpp and adjusts the impedance to fit the input of the ultrasonic transducer. Under the control of the DSPB, the power amplifiers are enabled (TX_en in Fig. 2) only when the short excitation

TABLE I
MAIN FEATURES OF THE PUV SYSTEM

| Parameter	Value
TX/RX channels	2, multiplexed
Dimension	10×12 cm
Power consumption	5 W max
RX Analog Gain	$7 - 55$ dB
TX voltage	$10 - 80$ Vpp
2 TX/RX frequency ranges	Low: $0.2 - 3$ MHz; High: $1.5 - 7$ MHz
TX burst	Arbitrary waveform
Internal buffer	64 MB
Sampling Freq.	100 MHz
Processing time	42 μs/depth
Input noise on 50 Ohm	1.5 nV√Hz
Data available to host	RF and IQ data, Spectral Matrix, Fequency Profile
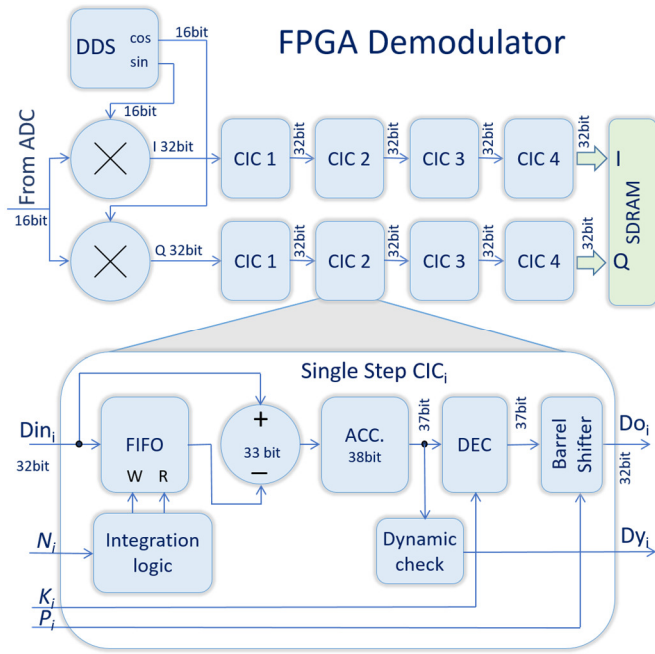
Fig. 4. Architecture of the coherent demodulator integrated in the FPGA. The input samples are multiplied by a synthetized sin/cos signal and filtered by 2 identical 4-step CIC filters. The details of a CIC stage are described in the lower part.
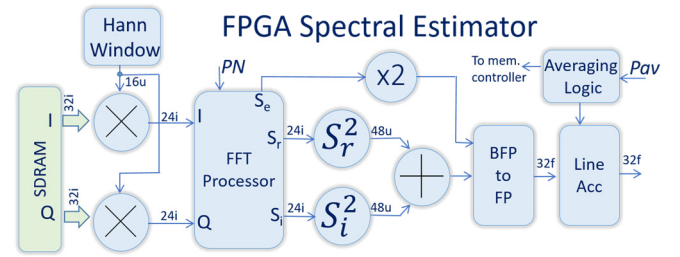

Fig. 5. Processing chain for spectral assessment and averaging. A I/Q data block is read from the SDRAM, windowed, processed by FFT. The result is squared, summed, and accumulated with other blocks from the same depth.

bursts should be transmitted. This allows a significant reduction of the noise injected in the sensitive RX channels during the RX phase.

The RX phase starts as soon as the transmission of the excitation pulse ends. Each of the 2 RX inputs is connected to a transformer that adjusts the impedance between the transducer and the low noise amplifier (LNA), integrated in the AD8331 (Analog Devices, Norwood, MA). The device incudes also a programmable gain amplifier (PGA). This stage features a 7 – 55 dB gain, controlled by the DSPB through the RX_Gain analog signal (see Fig. 2). A multiplexer selects, from the active RX channel, the signal that is moved to the DSPB for digital conversion. Two interchangeable AFEBs were designed for covering different frequency ranges. The separation AFEB/DSPB allows their easy replacement according to the specific needs.

Since the echoes gathered from the transducer are quite weak (in the range of 10's of μV to 100 μV), the input noise reduction was a major concern: the LNA section of the board is completely shielded, an 8-layer PCB is used to better isolate the potential sources of noise, the power is locally re-generated through low-dropout regulators and filters, and every non-necessary device is switched down during the RX phase.

C. The Digital Signal Processing Board (DSPB)

The DSPB, sketched in Fig. 3, hosts the analog-to-digital (AD) and digital-to-analog (DA) converters, and the digital devices for the numerical signal processing. The heart of the board is an EP3C25F256 FPGA from the Cyclone family of Altera (Altera Cor., San Jose, CA). It includes an Arbitrary

Waveform Generator (AWG) that, during the TX phase, synthesizes the TX pulse with programmable frequency, number of cycles, and apodization window. The pulse is DA converted by an AD9102 (Analog Devices, Norwood, MA) and moved to the AFEB.

During the RX phase, the received signal, conditioned in the AFEB, is AD converted at 100 MHz, 16 bit in an AD9265 (Analog Devices, Norwood, MA). The raw data are collected by the FPGA, where they are processed according to the steps described in Sec. II.A and detailed in Sec. IV.A. A 64 MB SDRAM memory buffer, used for data storing, is connected to the RAM controller in the FPGA through a 200 MB/s bandwidth channel.

The DSPB hosts the power converters for all the electronics of the system. To reduce their switching noise, the FPGA synchronizes their frequency to the PRI phase (see Sec. V.A).

The host connects to the FPGA of the DSPB through a 1 Mb/s UART (for commands and parameters) and a parallel interface working at 10 MB/s (for streaming the processed data). A fast controller [21] implemented in the FPGA, manages the internal TX/RX procedures and data processing according to the programmed parameters.

IV. THE DATA PROCESSING IN FPGA

The FPGA is mainly devoted to the numerical processing of the acquired signal. The basic steps of the processing were discussed in Sec. II.A, the details of FPGA implementation follows.

A. Demodulator

The 16 bit samples acquired from the RX signal are streamed at 100 Msps from the AD converter to the FPGA. They feed the coherent demodulator, whose architecture is shown in Fig. 4, top. Raw data are multiplied by two sin/cos signals synthetized at 16 bit by a DDS, which is programmed to produce the same frequency as the TX pulse. The results of the multiplications, at 32 bit, are processed by two parallel Cascaded Integrator Comb (CIC) filters [15]. Each chain has 4 stages with input/output at 32 bit. The filtered and decimated IQ data are stored in the SDRAM buffer at 32+32 bit per complex sample.

The architecture of each CIC-stage is detailed in Fig. 4, bottom. The input sample, Din, enters a FIFO memory

controlled by a logic that produces the write (W) and read (R) signals so that the FIFO output is delayed by N samples with respect to the input. The delayed signal is subtracted from the input and the result is accumulated in ACC (see Fig. 4). According to this logic, the ACC output presents the sum of the Din samples included in a sliding window of N samples. The 38 bit accumulator allows a word-growth up to 6 bit with respect to the 32 bit input, so that N in the range $1 - 64$ can be applied with no risk of overflow. The sample sequence is decimated by a factor K in DEC and applied to a barrel shifter that selectively reduces the dynamics from 38 bit back to 32 bit (7 possible positions, selected by P). The default setting is the most cautious: for example, if $N = 13$, a max growth of 4 bit is expected, and the shifter selects bit $36 - 5$ from the 38 bit word. The demodulator works in-line at a throughput rate of 100 MHz, performing 2 32 bit multiplications and 8 38 bit accumulations per clock cycle.

For each CIC-stage, i, N_i, K_i $(1 < i < 4)$ are programmed by the host according to the desired frequency mask of the filter.

B. Multi-gate spectral estimator

The architecture of the processing chain for the calculation of the spectral matrix implemented in the FPGA is sketched in Fig. 5. The matrix is calculated line-by-line. A block of N I/Q data, corresponding to the same depth, acquired in adjacent PRIs, is read from the SDRAM. An N-point Hann window, generated at 16 bit, is applied to the 32 bit I and Q components. The dynamics of the multiplication result, at 48 bit, is reduced by selecting the most significant 24 bit. These are loaded in the FFT processor, implemented through the 13.1 FFT megacore Intellectual Property (IP) by Altera Cor. The processor is configured to accept a 24+24 bit input, and to produce the N-point complex FFT output in block floating point (BFP) format, i.e. it generates N values with 24+24 bit mantissa and a common 6 bit exponent (S_r, S_i, S_e in Fig. 5, respectively). The calculation of the spectral power is obtained by squaring and summing the mantissas (S_r, S_i) and doubling the common exponent. The new mantissa and exponent are combined and converted to single precision floating point (FP) format in the BFP-to-FP block. These N values represent a line of the spectral matrix. Other lines from the same depth, but different PRIs, can be calculated and accumulated in the Line-Acc block (see Fig. 5) for noise reduction. Once a line is produced, the internal logic commands the processing of the next line of the matrix, or, in case the current matrix is completed, the start of a new matrix. The host configures the number of lines to be averaged (accumulated) with parameter Pav. The spectral estimator works in-line at 100 MHz, producing an FFT line in 9 µs.

C. Mean frequency estimator

This FPGA section, represented in Fig. 6, reduces the background noise by applying a threshold and performs the calculation reported in (2). For each line of the spectral matrix a single value is produced that represents the normalized Doppler shift.

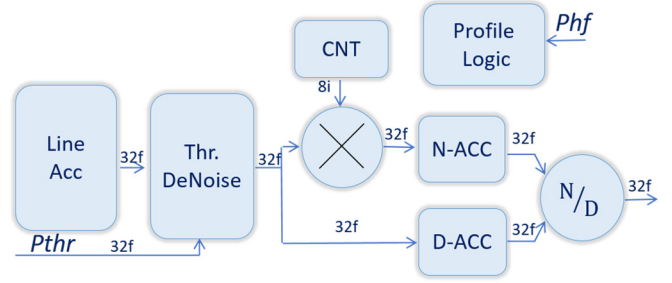The line of the spectral matrix produced by the spectral

Fig. 6. Processing chain for frequency profile calculation. The accumulated line is denoised, the numerator and denominator of (2) are calculated and finally divided.

estimator is read from the Line-Acc block. The values lower than the $Pthr$ threshold, set by host, are cut to zero in the Thr.DeNoise block. The counter CNT produces the sequence of integers that, multiplied to the line values, produces the numerator of (2). The summation is performed by the FP accumulator N-ACC. The accumulator D-ACC calculates the denominator of (2). Once the N values of the line are processed and the accumulators are ready, the final division is performed in N/D. This section, working at 100 MHz, needs 3 clock cycles per sample for the accumulations, and 16 cycles for the final division. A 128-point line is thus processed in 400 cycles, i.e. 4 µs.

V. PUV SYSTEM TESTS AND RESULTS

A. Noise characterization

The input noise performance was tested in the worst condition (PGA set for the maximum gain of 55 dB). The input was loaded on 50 Ohm. In this condition, the AD

TABLE II
PARAMETERS EMPLOYED IN THE ULTRASONIC SIMULATION

| Parameter	Symbol	Value
General		
Speed of sound	c	1540 m/s
Sampling Frequency	f_c	100 MHz
Scatterer density		1000/cm³
Scattering strength distribution		Normal, 1±0.4
Doppler Angle	θ	60°
Transducer Radius		
Flow Peak Velocity	V_p	0.5 m/s
Pipe radius	R	50 mm
Transmission		
Frequency	f_{Tx}	7 MHz
Transmission cycles	N	5
Apodization window		Tukey
Pulse Repetition Frequency	f_{PRF}	6 kHz
Noise		
Attenuation		8 dB/cm
SNR range tested		+20 ↔ -20 dB
Distribution		Gaussian
Spectral density		Constant
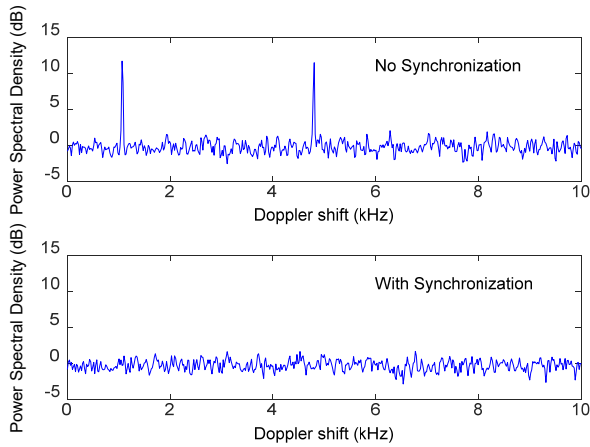
Fig. 7. Doppler shift measured at 55 dB gain, on a 50 Ohm load, at PRI = 100 μs, with power switching converters not synchronized to PRI start (top), and with synchronization (bottom).

converter acquired a white noise of 3 mV rms. This noise is generated by the LNA over the input bandwidth of 0.2 – 10 MHz, and is only 2 dB higher than the thermal noise produced by the input resistor (50 Ohm) at 25 °C. Since the AD converter accepts a 2 Vpp signal, the SNR at 55 dB gain is 47 dB. At lower gain, the thermal noise at the AD converter input lowers, and the achievable SNR rises correspondingly. The maximum SNR is limited by the ADC quantization noise of 80 dB (16 bit resolution, 12.7 Effective Number of Bits).

The following test was carried out to check the presence of narrow bandwidth noise. The PUV system, set at 55 dB gain, 50 Ohm load at input, was configured for calculating the spectral matrix with a PRI =100 μs. Narrow peaks, about 12 dB higher with respect to the background noise, are clearly visible in Fig. 7, top, which shows a row of the matrix. The test was repeated after synchronizing the power supplies to the PRI start, and results are shown in Fig. 7, bottom.

B. Data processing accuracy

In this test the accuracy of the mathematics of the processing chain integrated in the FPGA (see Sec. IV) has been evaluated. A data set of 600 PRIs was generated in Matlab (The Mathworks, Natick, MA) by using the ultrasound simulator software Field II [16][17] (freely available at http://field-ii.dk/). Field II, given the positions of a set of scatterers, the transducer characteristics, and the TX pulse, produces the RF echo data generated in each PRI by the investigated configuration. In this test, a 50 mm diameter pipe, insonated by a piston transducer with 7 MHz bursts, was simulated. The scatterer positions were updated in each PRI to mimic a parabolic flow with 0.5 m/s peak velocity. The details of the employed setting are listed in Tab. II, in *general* and *transmission* sections. No noise was added to the RF data in this test. The simulated RF data were quantized at 16 bit and introduced at the input of the FPGA (see 'From ADC' in Fig. 4, top). The FPGA was programmed to calculate spectral matrices by accumulating 1 and 8 lines (see Line-Acc in Fig. 5), and to extract the corresponding frequency profiles. The matrices and profiles were saved.
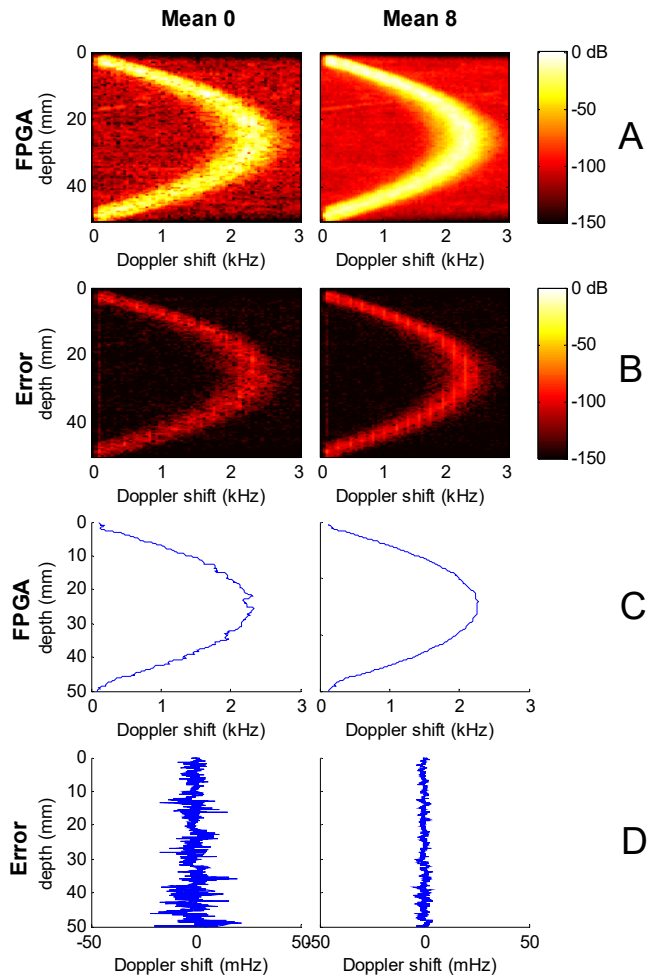
The same RF data used as input to the FPGA were

Fig. 8. Spectral matrices (A) and frequency profiles (C) calculated by the FPGA, and corresponding errors (B, D, respectively) with respect to the references calculated in double precision. Results without averaging (left) and 8-frame averaging (right) are reported.

processed in Matlab®, where the FPGA processing chain was replicated in double precision. The matrices and profiles calculated in Matlab® were compared to the corresponding matrices and profiles calculated by the FPGA.

In Fig. 8 the spectral matrices calculated by the FPGA without (left) and with (right) 8-frame averaging, are reported on A panel, while the B panel shows the difference with respect to the Matlab® reference. The matrices, displayed over a 150 dB dynamics, are reported before the application of the threshold. The error generated by the FPGA mathematics is lower than -100 dB. A similar test was performed for the frequency profiles. The profiles calculated by FPGA from the non-averaged (left) and averaged (right) matrices are reported in Fig. 8 C. The difference with respect to the corresponding profiles, calculated in Matlab®, are reported on the last row. The error is in the order of mHz.

C. Input dynamics

This test aims to quantify the dynamics available at the interface between the AD converter and the FPGA. A Gaussian noise was added to the Field II data used in the previous test. The power of the noise raised with increasing
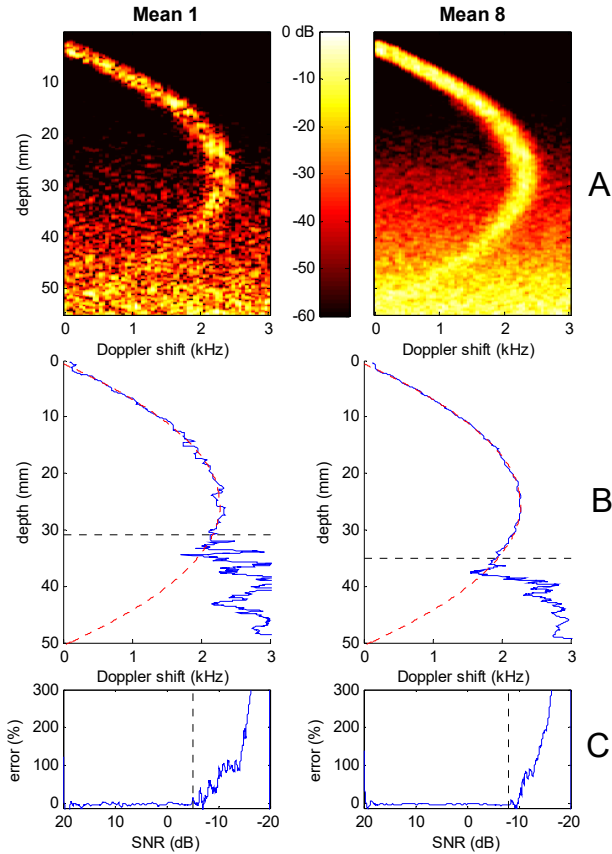
Fig. 9. A: Spectral matrices calculated on signal with depth-dependent noise (SNR in the range -20 dB to 20 dB). B: Calculated frequency profiles (blue) and theoretical parabolic profiles (dashed-red). C: Profile error. The profile is detected for a SNR higher than -5 dB and -8 dB when non-averaging and 8-frame averaging is applied (left and right, respectively).

depth, so that an SNR decreasing with a -8 dB/cm rate, and ranging from 20 dB (proximal pipe wall) to -20 dB (distal pipe wall), was generated (see Tab. II, '*noise*' section). This test signal was processed by the FPGA, and the spectral matrices calculated without averaging and with 8-frame averaging were saved together with the corresponding frequency profiles. Fig. 9 A, reports the spectral matrices color-coded and represented over a 60 dB dynamics, while the frequency profiles are shown in Fig. 9 B (blue line) together with the ideal parabolic profile (red-dashed curve). Fig. 9 C shows the profile errors, i.e. the difference between the calculated and the ideal frequency profile. In this latter panel, the horizontal axis reports the SNR of the RF test signal, which scales linearly, in dB, with the depth.

While the spectral profile is clearly detectable at low depths, it is no more distinguishable from noise starting at a depth that depends on the averaging. In particular, the profile is recovered within a ± 1% accuracy for depths lower than 31 and 35 mm in case of non- and 8-frame averaging, respectively (see dashed horizontal lines in central panel). These depth limits correspond to a SNR of –5dB and –8dB, respectively (see dashed vertical lines in panel C).

TABLE III
RESOURCES OF EP3C25F256I7 FPGA

Section	Mem. (bit)	DSP	LCS	Reg
AD interface	8192	0	1235	487
Demodulator	33536	4	2140	500
CIC stage	4288	0	483	121
Spectral Estimator	17410	26	5112	4465
Frequency Profile Es.	0	3	3134	700
SDRAM Controller	0	0	424	264
TX AWG	*16384*	10	1302	653
Host Comm	16384	0	1934	1092
Timing	0	0	439	61
Other	4096	0	1722	1271
Total Used	96002	43	17442	9439
% Used	16%	33%	71%	38%

D. FPGA resources and temporal performance

The project was fitted on the EP3C25F256I7 FPGA, suitable for the industrial temperature range. Tab. III lists the resources employed by the main sections of the FPGA. For example, the demodulator reported in Fig. 4, requires about 2k LCS, 500 registers, 4 9x9 multipliers and 33 kbit of memory. A single CIC stage, which is part of the demodulator, requires about 500 LCS, 100 registers, no multipliers and 4 kbit of memory (used for the FIFO delay chain, see Sec. IV.A). The spectral and frequency profile estimator refers to the blocks described in Sec. IV.B and IV. C, respectively. The remaining lines of the table detail the requirements of the AD converter interface (AD interface), the SDRAM memory controller (SDRAM controller), the arbitrary waveform transmitter (TX AWG), the module in charge of receiving commands from the host and downloading data (Host Comm), the generator of the timings for the synchronization of the FPGA operations (timing). The last 2 lines report the total resource usage and the percentile with respect to the available resources.

The time closure of the project was achieved for 100 MHz with a 0.117 ns slack. The FPGA processes a line of the spectral matrix with the corresponding frequency profile in 42 μs, so that a frequency profile at, e.g. 1024 depths, is produced at a rate of more than 20 Hz.

E. Test on Industrial Fluid

A non-Newtonian industrial fluid (sludge) with a particle concentration of 26% (w/w) flowed at 360 L/min in a stainless steel pipe with an inner diameter of 48 mm. Single-element, non-invasive ultrasound sensors were installed on the pipe as detailed in [22] and connected to the PUV system. Pressure sensors where installed on the pipe at a distance L = 1 m. The PUV system was configured to transmit 2.5 MHz pulses at PRI = 80 μs, acquire 8192 samples per transmission (to cover the full pipe diameter) and process the data to generate the spectral matrices and the frequency profile. Results were calculated in-line and downloaded to the host.

Fig. 10 shows, on the left, one of the spectral matrices calculated by the system with no averaging, while the corresponding frequency profile is reported on the right. In spite of the high fluid attenuation (about 5 dB/cm), the profile is clearly detected over the entire pipe diameter. The pipe steel
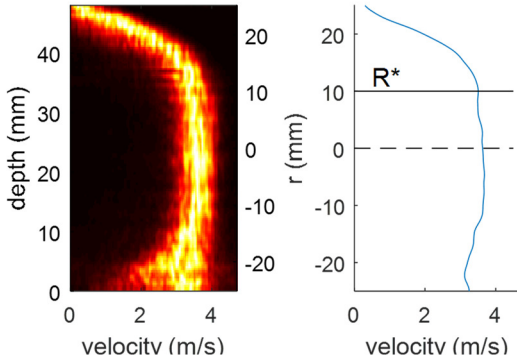
Fig. 10. Spectral matrix (left) and corresponding velocity (right) measured in a 48.6 mm pipe where an industrial suspension flowed at 360 L/min. Plug radius is shown by the line at r = 10.0 mm on the right panel.

Fig. 11. Top: shear rate along the nearer section of the pipe radius (-10 to 25 mm). Plug radius is shown by the line at r = 10mm. Bottom: rheology characterization of the fluid. Blue circles represent the measurements, the corresponding regression line is reported in red. The line crosses the vertical axis at the yield stress point τ_{0R} = 8.0 Pa.

produces an echo that is $30 - 40$ dB stronger than the signal reflected from the fluid particles. This produces a typical distortion that makes the profile apparently non-axisymmetric (the far end of the curve does not reach the expected 0 frequency at the distal wall position). The same phenomenon is produced by vessel walls in biomedical applications [23]. The flat shape of the central section of the profile (plug flow) reveals that the investigated fluid exhibits a yield stress. A plug radius of R^*=10.0 mm is measured from the profile (see horizontal line in Fig. 10, right) and the corresponding yield stress, calculated with (6), is τ_0= 8.0 Pa. The reference yield stress, measured in laboratory on the same fluid by a stress controlled rheometer, is τ_{0R}= 8.1 Pa, thus, in this example, the measurement error was −1.2%.

Fig.11 shows, on top, the shear rate calculated as the derivative of the velocity profile of Fig. 10. In the region where 10 mm $< r <$ 22 mm the shear rate ranges between 0 and 430 s^{-1} (this range is determined by the flow rate). The characterization of the fluid over this range is thus possible through a single measurement. The resulting rheogram, which reports how the shear stress is correlated to the shear rate (see (5)), is shown in the bottom graph. Blue circles are the experimental measurements, while the corresponding regression line is represented in red. The agreement with rotational rheometry data is within ± 5%.

VI. Discussion and Conclusion

Until now, no practical solution was commercially available for in-line monitoring of non-Newtonian and opaque industrial fluids flowing in process pipes. The PUV system, capable of acquiring data and calculating in real-time the velocity profile, represents an important step forward. The board produces profiles with high spatial and temporal resolution, which, correlated to pressure data, allow a complete rheological characterization of the monitored fluid for the whole range of shear rates present in the flow (see Secs. II. B and V. E).

The PUV system is connected to non-invasive ultrasound sensors, capable of transmitting and receiving the pulses through the stainless steel pipes. A particular coupling technique is employed to produce undistorted pressure field in the pipe lumen [22]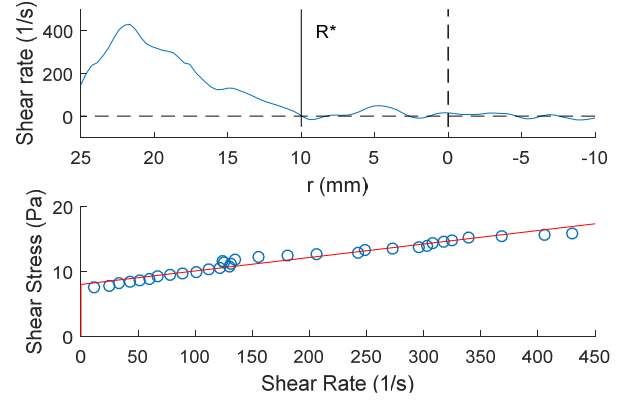. Moreover, since the internal pipe surface is untouched, the flow velocity profile is unaffected by the sensor installation. The PUV system can be used in food or pharmacological industries, where hygienic constraints require no contact between the sensors and the products to avoid contamination and to facilitate proper Cleaning In Place (CIP) method.

The complex propagation of the ultrasound wave in some suspensions can produce errors. Nevertheless, the PUV method was proven suitable for a wide range of industrial fluids [24], and, moreover, it allows accurate rheological characterization also in situations where conventional rheometers fail due to shear gap size restrictions [24].

The ultrasound wave is significantly attenuated when propagating across most of the industrial fluid of interest, (see, e.g. the 5 dB/cm attenuation of the sludge fluid in the test reported in Sec. V.E), and the received signal is often limited to few 10's of µV. The noise performance limits the kind of fluids that can be investigated and the maximum depth achievable, and thus has a large impact on the industrial usability of the instrument. For this reason, the proposed system includes a state-of-the-art LNA with a thermal noise near the theoretical limit (see Sec. V.A). The switching noise of the power suppliers is another important source of noise. Spread spectrum techniques, typically used to mitigate such a disturb [25], are ineffective in case of Doppler processing. The PUV electronics resynchronizes the switching frequency of the power suppliers with the start of each PRI, thus cancelling any phase difference of the noise among PRIs, like shown in Fig. 7. Moreover, by exploiting the FPGA flexibility, the mathematics involved in each of the processing steps was fine-tuned to the specific application. For example, CIC filters work at fixed-point 38 bit, FFT at 24 bit block-floating point, etc. Thanks to these features, the prototype can detect the velocity profile with an accuracy within ± 1% when the input SNR is higher than −5 dB. (see Sec. V.C and Fig.11).

The FPGA allows the maximum system compactness and efficiency by integrating in a single chip the data processing, the interface to other board devices like ADCs, DACs, PGA, and the state machines necessary for system managing.

The integrated ultrasound front-end, the real-time processing, the high input dynamics, the noise performance, the full programmability, etc., push the limit of the PUV system well beyond the simple acquisition boards currently used, in particular where the attenuation of ultrasound is a major concern. Further studies can aim to add the on-board capability of auto-tuning a part of the acquisition/processing parameters. This will further ease the installation and make the system adaptable to different conditions without user action.

The PUV board is installed, as an integral part of the Flow-Viz system, in pilot plants of international companies, where it is currently being validated for a wide range of industrial applications.

REFERENCES

[1] J. M. Dealy, K.F. Wissbrun, "*Melt Rheology and its Role in Plastics Processing: Theory and Applications*", New York, NY: Van Nostrand, 1990, ISBN: 978-0-7923-5886-2.

[2] R.A. Granger, "*Fluid Mechanics*". Mineola, NY: Dover, 1995.

[3] Y.L. Yeow and J.W. Taylor, "Obtaining the shear rate profile of steady laminar tube flow of Newtonian and non-Newtonian fluids from nuclear magnetic resonance imaging and laser Doppler velocimetry data", *J. Rheol.*, vol. 46, no.2, pp. 351–365, Mar. 2002.

[4] P.K. Chande and P.C. Sharma, "Ultrasonic Flow Velocity Sensor Based on Picosecond Timing System", *IEEE Trans. Ind. Electron.,* vol. 33, no. 2, pp. 162-165, May 1986.

[5] T.A. Kowalewski, "Velocity Profiles of suspensions flowing through a tube", *Archiv. Mech.*, vol. 32, pp. 857-865, 1980.

[6] J.J. Rodriguez-Andina, M.J. Moure, and M.D. Valdes, "Features, design tools, and application domains of FPGAs," *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 1810–1823, Aug. 2007.

[7] E. Monmasson, M.N. Cirstea, "FPGA Design Methodology for Industrial Control Systems—A Review", *IEEE Trans. Ind. Electron.,* vol. 54, no. 4, pp. 1824 - 1842, Aug. 2007.

[8] J. Weber, E. Oruklu, J. Saniie, "FPGA-Based Configurable Frequency-Diverse Ultrasonic Target-Detection System", *IEEE Trans. Ind. Electron.,* vol. 58, no. 3, pp. 871 - 879, Mar. 2011.

[9] M. Zamora, M.P. Henry, "An FPGA Implementation of a Digital Coriolis Mass Flow Metering Drive System", *IEEE Trans. Ind. Electron.,* vol. 55, no. 7, pp. 2820 - 2831, Jul. 2008.

[10] S. Ricci, L. Bassi, A. Dallai, E. Boni, P. Tortoli, "A Dual Transducer Ultrasound System for Quantitative Doppler Measurements", *IEEE International Symposium on Industrial Electronics* (ISIE 2007) *Proceed*, pp. 2718-2723, Vigo, Jun. 2007.

[11] S. Ricci, E. Boni, F. Guidi, T. Morganti, and P. Tortoli, "A programmable real-time system for development and test of new ultrasound investigation methods", *IEEE Trans. Ultrason. Ferroelect. Freq. Contr.*, vol. 53, no. 10, pp. 1813 - 1819, Oct. 2006.

[12] S. Ricci, M. Liard, B. Birkhofer, D. Lootens, A. Brühwiler, P.Tortoli, "Embedded Doppler System for Industrial in-Line Rheometry", *IEEE Trans. Ultrason. Ferroelect. Freq. Contr.*, vol. 59, no. 7, pp. 1395-1401, Jul. 2012.

[13] R. Kotzé, S. Ricci, B. Birkhofer, J. Wiklund, "Performance tests of a new non-invasive sensor unit and ultrasound electronics", *Flow Meas. Instrum.*, vol. 48, pp. 104 - 111, Apr. 2016.

[14] J.A. Jensen, "*Estimation of Blood Velocities Using Ultrasound: A Signal Processing Approach*", Cambridge University Press, Great Britain, 1996.

[15] E. Hogenauer, "An economical class of digital filters for decimation and interpolation", *IEEE Trans. on Acoustics, Speech, and Signal Process.*, vol. 29, no. 2, pp. 155-162, Apr. 1981.

[16] J. A. Jensen and N. B. Svendsen, "Calculation of pressure fields from arbitrarily shaped, apodized, and excited ultrasound transducers", *IEEE Trans. Ultrason. Ferroelect. Freq. Contr.*, vol. 39, no. 2, pp. 262–267, Feb. 1992.

[17] J.A. Jensen: "Field: A Program for Simulating Ultrasound Systems", *Med. & Biol. Engin. & Comp.*, vol. 34, no. 1, pp 351-353, 1996.

[18] M. Muller and P.O. Brunn and C. Harder, "New Rheometric Technique: The Gradient-Ultrasound Pulse Doppler Method", *Appl. Rheol*, vol. 7, no. 5, 204, Oct. 1997.

[19] B. Birkhofer, A. Debacker, S. Russo, S. Ricci, and D. Lootens, "In-Line Rheometry Based on Ultrasonic Velocity Profiles: Comparison of Data Processing Methods", *Appl. Rheol.* vol. 22, no. 4, 44701, Aug. 2012.

[20] J.A. Wiklund, B. Birkhofer, M.T. Stading, S.A.K. Jeelani, & E.W. Windhab, "In-line rheometry of particulate suspensions by pulsed ultrasound velocimetry combined with pressure difference method", *Appl. Rheol*, vol. 22, no. 4, 42232, Aug. 2012.

[21] Z. Hajduk, B. Trybus, and J. Sadolewski, "Architecture of FPGA Embedded Multiprocessor Programmable Controller", *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 2952-2961, May 2015.

[22] T.J. Shamu, R. Kotzé, J. Wiklund, "Characterization of Acoustic Beam Propagation Through High-Grade Stainless Steel Pipes for Improved Pulsed Ultrasound Velocimetry Measurements in Complex Industrial Fluids", *IEEE Sens. J.*, vol. 16, no. 14, pp. 5636 – 5647, Jul. 2016.

[23] R.S.C. Cobbold, "*Foundations of biomedical ultrasound*", New York: Oxford University Press; 2007, ISBN: 978-0195168310.

[24] J. Wiklund, M. Stading, "Application of in-line ultrasound Doppler-based UVP–PD rheometry method to concentrated model and industrial suspensions", *Flow Meas. Instrum.*, vol. 19, no.3-4, pp. 171-179, Jun. 2008.

[25] G.M. Dousoky, M. Shoyama, T. Ninomiya, "FPGA-Based Spread-Spectrum Schemes for Conducted-Noise Mitigation in DC–DC Power Converters: Design, Implementation, and Experimental Investigation", *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 429 - 435, Feb. 2011.

Stefano Ricci (M'07-SM'16) received the degree in Electronic Engineering in 1997, and the Ph.D. degree in Electronic Systems Engineering in 2001, from the University of Florence. Since 2006 he works as researcher at the Information Engineering Department of the University of Florence. His research activities are focused on the development of high performance ultrasonic systems and the development and test of new ultrasound methods for medical and industrial applications. He is author of more than 70 publications in international conferences and journals.

Valentino Meacci (S'16) was born in Empoli, Italy, in 1975. He received a Bachelor's degree in electronic engineering in 2011 and a Master's degree in electronic engineering in 2013 from the University of Florence, Italy. He is currently involved in the development of novel ultrasound systems, with focus on electronic system design and highly optimized FPGA firmware.

Beat Birkhofer received the degree in food engineering and the Ph.D. degree from the Swiss Federal Institute of Technology, Zurich, Switzerland. In 2008, he joined Sika Services AG, where he works in the Production Engineering department. His professional activities comprise industrial in-line process monitoring techniques such as Doppler ultrasound for rheometry. He is a member of the scientific committee of the International Symposium on Ultrasonic Doppler Methods for Fluid Mechanics and Fluid Engineering (ISUD).

Johan Wiklund received his M.Sc. in Chemical Engineering in 2002 from Chalmers University of Technology, Gothenburg, Sweden and the Ph.D. degree in Engineering in 2007 from Lund University of Technology, Lund, Sweden. Since 2007 he has been working for SP- Technical Research Institute of Sweden as Senior Research Scientist, Flow-Viz Project Manager and Area Leader Ultrasonic Technology, with special focus on the development of Doppler ultrasound technology for industrial in-line process monitoring and control applications. He is a member of the scientific committee of the International Symposium on Ultrasonic Doppler Methods for Fluid Mechanics and Fluid Engineering (ISUD).