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CLOCK AND CARRIER SYNCHRONIZATION IN FDMA/TDM USER-ORIENTED SATELLITE SYSTEMS

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Abstract

FDMA/TDM access, recently proposed for future mobile and business service satellite systems, requires a MultiCarrier Demodulator (MCD) on-board to recover the individual uplink SCPC modulating streams and build-up a unique downlink TDM carrier.

The complexity of such a MCD depends upon a number of factors (number of SCPCs and data rate, modulation format, type of employed technology, ...) among which a rather important role is played by the carrier/clock coherency of the different uplink signals at the satellite input.

The paper expands on some possible carrier/clock synchronization strategies, showing their impact on both user terminal and on-board MCD complexity.

A quantitative estimate of such an impact on the on-board (baseband digital) hardware is also given.

1. INTRODUCTION

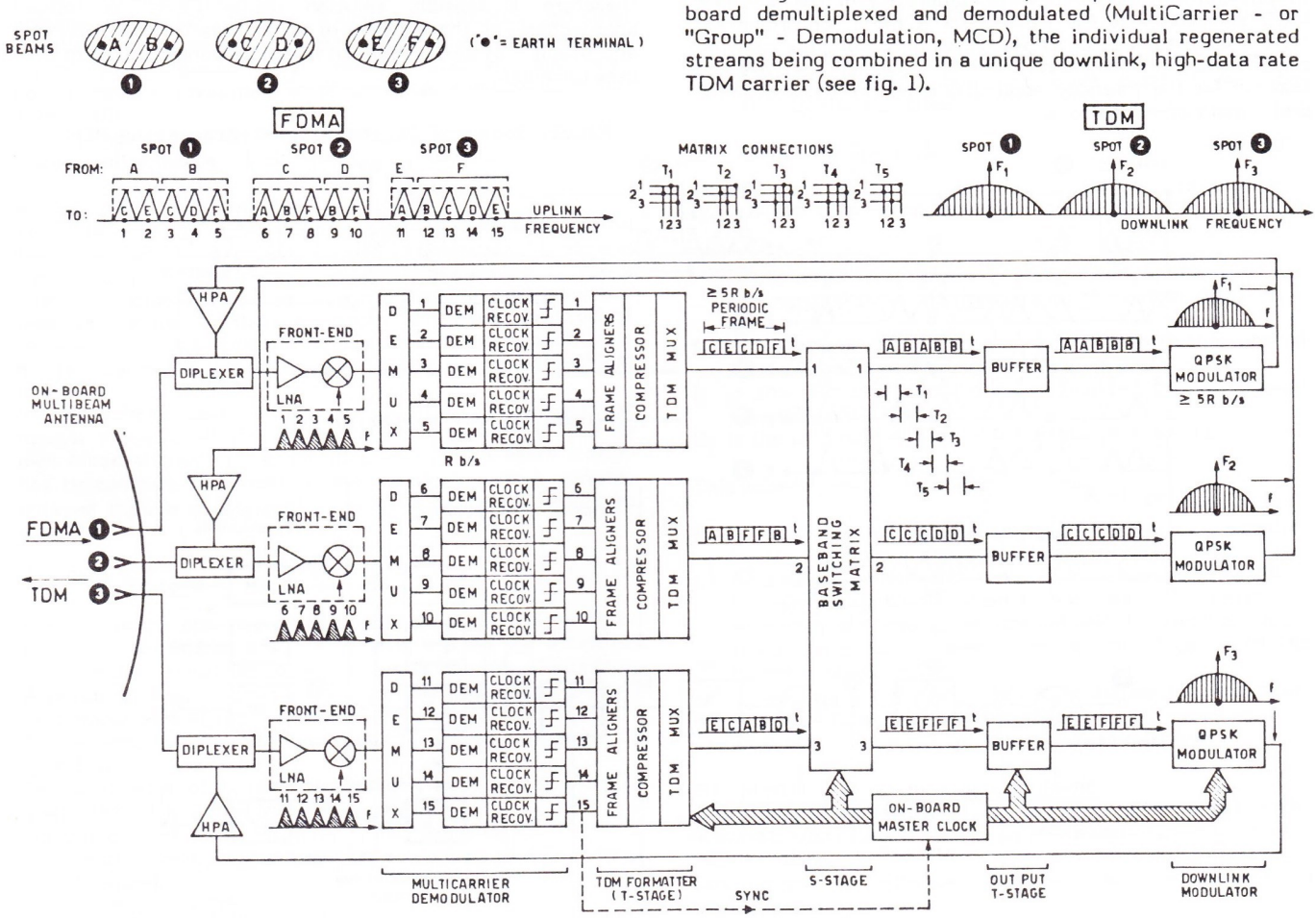
"User-oriented" satellite systems address the routing of low-to-medium data rate signals (Ref. 1), exchanged through Very Small Aperture Terminals (VSATs, antenna diameter 0.8-to-2.4 meters in general) located at the customer premises, which directly access the satellite differently from the "network-oriented" phylosophy.

Potential users of such systems are substantially mobile (land, maritime, aeronautical) services (from some hundred bps to some tens Kbps) and business services (from some tens Kbps to some Mbps), which are both expected to significantly grow up in the next decade.

Among the various access shemes which can be in principle considered, Single-Channel-Per-Carrier, Frequency Division Multiple Access (SCPC/FDMA, uplink) in conjunction with Time Division Multiplexing (TDM, downlink) has been recently proposed as a valid candidate (Refs. 1 through 8).

According to FDMA/TDM access, the uplink SCPCs are on-board demultiplexed and demodulated (MultiCarrier - or "Group" - Demodulation, MCD), the individual regenerated streams being combined in a unique downlink, high-data rate TDM carrier (see fig. 1).

FIG.1. FDMA/TDM On-Board Processing Payload.



This feature allows the efficient use of on-ground transmitted power - which must only be proportional to the user-required data rate using FDMA, and thus can be a cheap Solid-State Power Amplifier (SSPA) in most of the applications -and on-board TWTA as well, which can be saturated due to the single-carrier operation which prevents from intermodulation.
Moreover, the on-board regeneration enables baseband processing suitable to build-up the "switchboard-in-the-sky" concept (Ref. 9) based on the insertion of time-space-time (TST) stages on-board to provide full switching capabilities to the users, as well as some link budget advantages if up and downlink are nearly balanced.
A number of configurations have been reported to physically implement, with reduced size and power consumption, the MultiCarrier Demodulator, substantially utilizing BaseBand Digital Signal Processing (BBDSP), Surface Acoustic Wave (SAW) analog signal processing and Acousto-Optics.
The complexity of MCD, which is the most critical part of a FDMA/TDM regenerative payload, depends upon a number of factors such as number and data rate of SCPCs to be demultiplexed and demodulated, employed technology, modulation format(s), reconfigurability (variable center frequency and/or data rate) requirements, and so forth.
Indeed, focusing on BBDSP configurations as schematically depicted in fig. 2 (next sections 2 and 3, however, concern system considerations which are really independent of selected technology), most of the reported MCD implementations are primarily based on the assumption of unsynchronized user carrier and clock (symbol) frequencies, without any particular system constraint on the user terminals.
Other system configurations can be envisaged, where some kind of carrier and/or clock synchronization is present. As it is shown later in table 1, they have the advantage of simplifying the implementation complexity of the on-board MCD structures at the expense of a more "co-ordinated" system operation. In other words, a more complex network configuration is required, which, however, is deemed feasible for the intended applications on the basis of some preliminary investigations.

2. CARRIER FREQUENCY SYNCHRONIZATION

Due to the phase noise and instabilities of oscillators, precise carrier frequency synchronization is hardly feasible for satellite applications. However, schemes can be derived where some kind of control of the nominal value of the usable frequencies is implemented. Such schemes assure that the user frequency at the transponder input is at the nominal value with a very small uncertainty (residual frequency instability): this eliminates the requirement for frequency search by the on-board demodulator and greatly relaxes the filtering specifications of the on-board demultiplexer. As a consequence, the overall complexity of the on-board MCD is reduced.
As an example, recent studies on on-board MCD (e.g. Ref. 8) have assumed user frequency instabilities at the satellite input ranging from 10^{-7}-to-10^{-8} (with an on-board down converter stability of 10^{-6}).
These values of user frequency stability are hardly achievable with current low-cost crystal oscillators at the user terminals. However, relatively simple schemes can be utilized in order to obtain the desired frequency stability, as shown in fig. 3 (Ref. 4), where a possible Frequency Extraction and ReTransmission (FERT) scheme has been proposed. Using FERT, the user transmission frequency stability depends on the satellite reference frequency stability, even using low-cost crystal oscillators at the user terminal.
The implementation complexity of this scheme is relatively small: it requires the highly-stable satellite reference frequency f_R to be received by the earth terminals and each terminal to implement the FERT operation, which involves a very limited amount of additional hardware.
This kind of carrier synchronization (which decreases the transmitted carrier instability at the satellite input) appears therefore a feasible solution (using FERT or other approaches), at the expense of an increased - but however acceptable - system complexity, mainly concentrated in the user terminal.

FIG.2. Baseband Digital Signal Processing MCD.

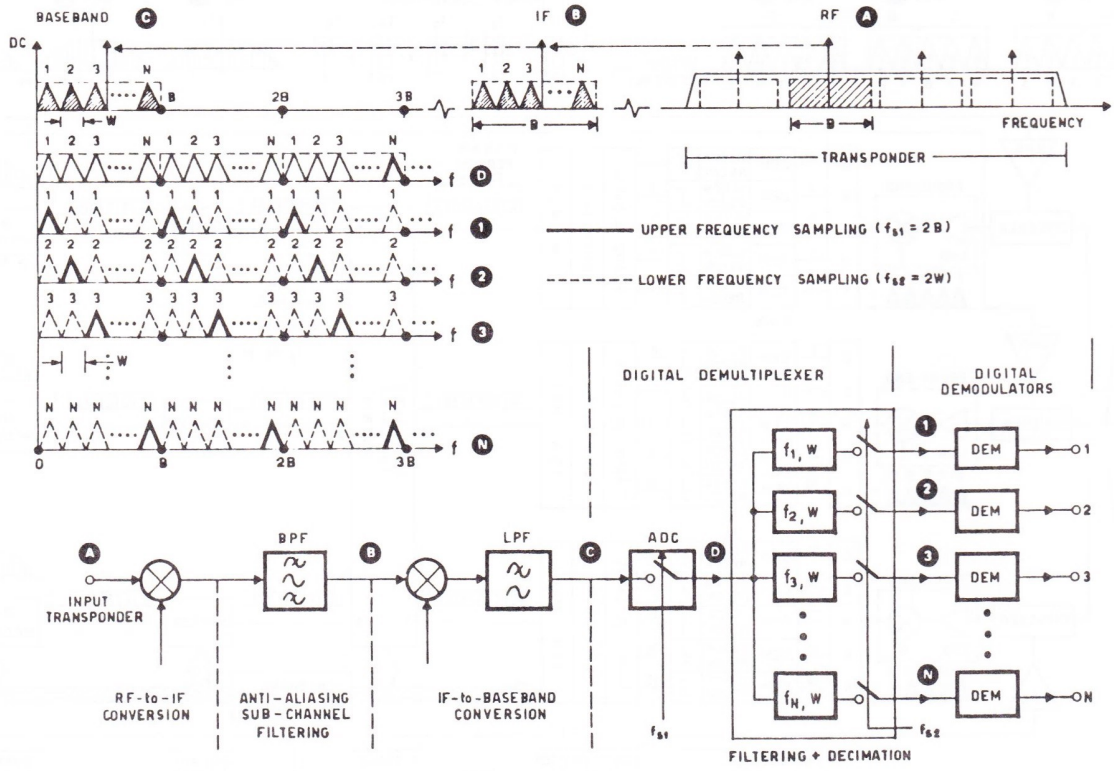
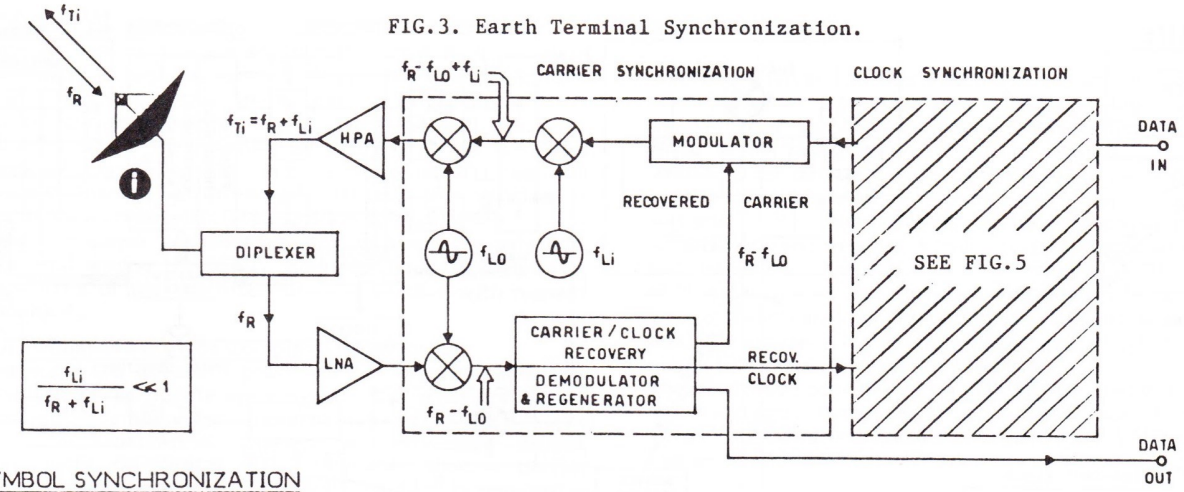


FIG.3. Earth Terminal Synchronization.



3. SYMBOL SYNCHRONIZATION

The possibility of assuming clock-synchronized SCPC signals at the satellite input directly impacts on the complexity and structure of the on-board demultiplexer and demodulators. It greatly simplifies the MCD structure and reduces its implementation complexity, as a MCD, under the assumption of symbol synchronization, may be a completely different equipment with respect to a MCD which does not assume symbol synchronization.
Based on some preliminary investigations, the following two schemes A and B seem to be suitable at present for symbol synchronization.
Both of them foresee the presence of a highly stable (10^{-9}-to-10^{-11}) "master" clock on-board the satellite.
It seems realistic to implement this function by a standard Voltage-Controlled Cristal Oscillator (VCXO, nominal stability of the order of 10^{-6}) synchronized by a control signal from ground (e.g. master station, but also communication terminals) as schematically indicated in fig. 4 (Ref. 10).
We will not expand on this subject, but only will assume a high-stability master clock on-board the satellite.

A) "Master-Slave" Open-Loop scheme
This scheme is the application to a satellite network of the "master-slave" approach of terrestrial digital communication networks for achieving clock synchronization. Of course, in a satellite network only one level in the master-slave hierarchy is present (instead of several levels of terrestrial digital networks), i.e. satellite = master, earth-stations = slaves (all at the same hierarchical level).
In this scheme (see Fig. 5), the satellite broadcasts the master clock to all the earth stations. In order to get its own clock aligned at the satellite input, each earth station has to compare the received master clock with a suitably delayed replica of its local clock. The delay t'_i should be equal to:

$$t'_i = 2t_i + t_p \qquad (1)$$

where t_i is the one-trip satellite-to-i-th earth station delay and t_p is the signal processing delay within the satellite. Once clock synchronization is achieved at the phase detector of Fig. 5, equation (1) assures clock (i.e. symbol) synchronization at the satellite.
This scheme requires the knowledge or accurate estimate of t_i and t_p.
The knowledge of t_p is not a problem, as it can be exactly evaluated for a digital MCD implementation.
On the contrary, the estimate of the one-trip delay t_i may be a rather complex problem in a number of cases (e.g. mobile users).
Therefore, at present, this scheme appears applicable mainly to fixed-satellite services.

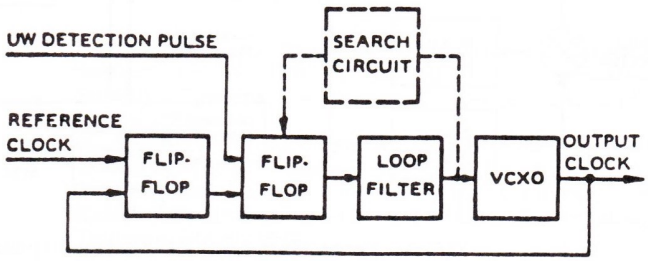


FIG.4. **Block diagram of the PLL for the on-board clock generation**

Master-slave network synchronization is known to be always stable.
Moreover, it can be shown that the steady-state time error between the master clock and slave clock i may be evaluated by the equation:

$$\Delta T_i = (f_M - f_i)/G_i + f_M \Delta t_i \qquad (2)$$

where:
ΔT_i is the time error between the master clock and clock i;
$\Delta t_i = \hat{t'_i} - (2t_i + t_p)$ is the error of the delay $\hat{t'_i}$ used in the local loop of the i-th earth station with respect to the actual delay $2t_i + t_p$;
f_M is the master clock frequency normalized to the nominal network frequency;
f_i is the i-th clock frequency normalized to the nominal network frequency;
G_i is the loop gain of the i-th earth station ($sec.^{-1}$).

This scheme has the following features:

i) it requires no processing capability on-board the satellite for the symbol synchronization operation;
ii) it requires a moderate amount of processing capability for symbol synchronization at each earth terminal (i.e. detection of phase difference between received and local clock and a control loop to adjust the clock, using the detected phase difference);
iii) it requires a sufficiently accurate estimate of the delay $t'_i = 2t_i + t_p$ at each earth terminal;
iv) each slave clock can be continuously controlled.

B) "Master-Slave" Closed-Loop scheme
The main disadvantage of the previous scheme (A) is the required knowledge or estimate of the delay $2t_i + t_p$ at each earth station.
An alternative scheme which avoids this problem is illustrated in Fig. 5(b) and (c).

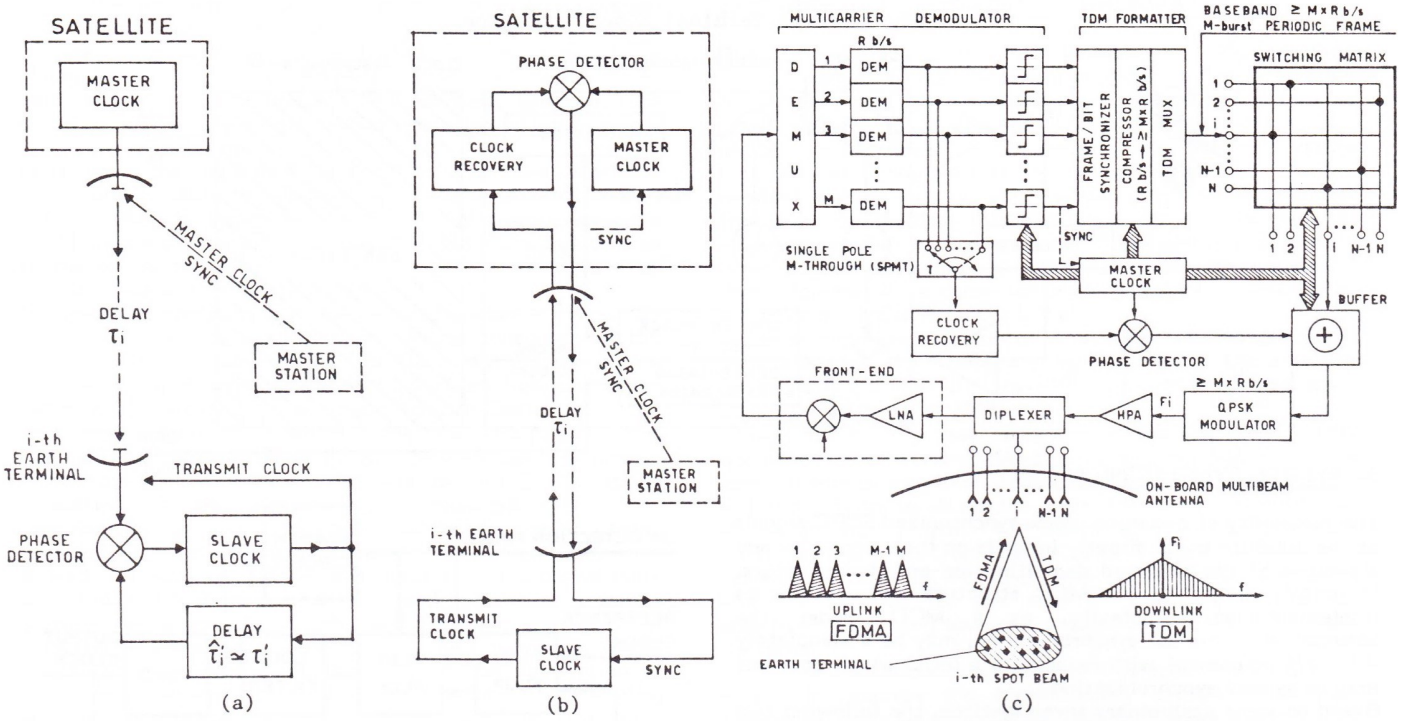


FIG.5. Earth Terminal Clock Synchronization: (a) Open Loop; (b) and (c) Closed Loop.

On-board the satellite, each SCPC recovered clock is cyclically compared with the on-board reference (master) clock, and the detected phase difference ΔT_i is transmitted to the corresponding earth station via a down-link TDM signal (which could be in principle directed to all the earth stations).

This system makes it possible to share a unique on-board clock recovery circuit among all the SCPC channels, and does not require any delay compensation at the earth stations, as this is automatically achieved by the closed-loop structure.

As any master-slave synchronization, this scheme would assure the stability, if each slave clock were continuously monitored on-board.

However, a previously said, an attractive feature of scheme B is the possibility of sharing the on-board circuit of clock recovery and phase-difference detection. It follows that, in this case, the on-board clock monitoring of each slave clock is periodically activated and interrupted, with the active period being much smaller than the non-active period, because of the large number of earth stations. Hence the system stability, in presence of a periodically interrupted on-board monitoring of the slave clocks, is not a-priori assured and should be carefully analyzed. For example, stability considerations could dictate a number of on-board clock monitoring circuits larger than one, in order to increase the "duty cycle" of the measurement/updating of each earth station clock.

Even for this scheme it is possible to evaluate an expression for the steady-state time error between the master clock and slave clock i; it can be shown that it is given by the expression:

$$\Delta T_i = (f_M - f_i)/2G_i + f_M \Delta t_i/2 \qquad (3)$$

where Δt_i is the difference between the up-link and down-link trip delays.

$\Delta t_i = 0$ in the case of continuous on-board clock monitoring, whilst in the case of periodically interrupted on-board clock monitoring or in the presence of mobile users, Δt_i can be different from zero, equating the difference of the up-link trip delay at the time of measurement of clock i and the present value of the down-link delay. The other quantities in eq. (3) have the same meaning as exposed in sub-section A).

The main features of this scheme are the following:

i) it requires a processing capability on-board the satellite for the symbol synchronization operation; however, a single on-board clock monitoring circuit can be time-shared, in principle, among all the SCPC channels;
ii) it requires no processing capability at the earth terminals; it only requires a local clock adjustable from the received time error information;
iii) it requires no knowledge or estimate of delay;
iv) each slave clock is periodically monitored and adjusted: this may influence the network synchronization stability, which is perhaps the main problem to be investigated for this scheme.

Assuming to have solved the stability problem for scheme B, the time error equations (2) and (3) indicate that, with the same values of the parameters, scheme A has a steady-state error twice that of scheme B.

Based on this consideration and on the features of each system, we can say that scheme B appears more advantageous at this early stage of investigation. However, the key point of network stability for scheme B must be analyzed very carefully.

4. ESTIMATE OF THE HARDWARE COMPLEXITY

4.1. Carrier Synchronization

The FERT scheme of carrier frequency synchronization does not require any specific equipment on-board the satellite; it does require some additional equipment at each earth station. However, the increased earth terminal complexity is deemed acceptable at a very low cost.

4.2. Symbol Synchronization

Scheme A does not require any specific equipment on-board the satellite; it requires some limited additional equipment at each earth station. Again, even in this case the additional terminal complexity is acceptable, at least for fixed users where the estimate of delay t'_i is not too hard; for mobile terminals, the increased complexity can be significant (hence, as previously stated, this scheme is primarily concerned with fixed-service applications).

Scheme B requires a phase detector on-board the satellite, time-shared among the SCPC channels; on the other hand, the structure of the earth terminals is simpler with respect to scheme A.

4.3. On-Board Processor Complexity Reduction

To estimate the on-board processor complexity reduction, we shall take as a reference system the on-board digital multicarrier demodulator in presence of a FERT-type carrier .synchronization. Indeed, as previously stated, current work on digital MCD indicates that a carrier frequency stability ranging from 10^{-7}-to-10^{-8} is required in order to guarantee acceptable system performance and complexity. Therefore, the MCD design with a carrier stability of 10^{-7}-to-10^{-8} and without symbol synchronization is taken as reference system (complexity = 1 or 100%) to evaluate the difference in complexity of schemes employing symbol synchronization.

Assuming symbol synchronization (either by scheme A or scheme B), the on-board MCD requires carrier phase recovery for a coherent detection (not required in presence of a differential detection, which however seems not recommendable due to the long required delay lines), whilst the clock recovery circuit is avoided.

Based upon preliminary results of current works (Ref. 8, 13) carried out for 9.6 Kb/s, 64 Kb/s and 2.048 Mb/s transmission rates, the on-board processor without the clock (symbol) recovery circuits can be estimated having a complexity 70%-to-85% with respect to the reference system (100%), depending on the transmission rate, number of channels, use of coherent or differential detection, etc. (see table 1).

However, better results can be obtained using the so-called "analytic signal method" which allows integrating the DEMUX and DEMOD operations, due to its "per-channel" structure (this integration is absolutely not conceivable for any "block" method). The demultiplexing and demodulation are jointly performed by a single component whose complexity is roughly 60%-to-70% with respect to the cascaded separate operations.

Hence, in symbol-synchronized systems, removing the carrier recovery circuits and employing the analytic signal approach can result in a on-board processor (MCD) complexity which is 50%-to-60% that one of the reference system, as summarized in Table 1.

TABLE 1. ESTIMATE OF FDMA/TDM ON-BOARD PROCESSOR (MCD) COMPLEXITY REDUCTION IN SYMBOL - SYNCHRONIZED SYSTEMS

REFERENCE SYSTEM (CARRIER SYNCHRONIZATION, NO SYMBOL SYNCHRONIZATION) COMPLEXITY			100
SYMBOL - SYNCHRONIZED SYSTEM COMPLEXITY	SEPARATE DEMULTIPLEXING AND DEMODULATION	COHERENT DETECTION	85
		DIFFERENTIAL DETECTION	70
	DEMUX+DEMOD INTEGRATION (Analytic Signal Method, Ref. 10)	COHERENT DETECTION	60
		DIFFERENTIAL DETECTION	50

5. CONCLUSIONS

We have analyzed in this paper the impact on the on-board MultiCarrier Demodulation (MCD) complexity of clock/carrier synchronization, at the satellite input, of the SCPC uplink signals in a FDMA/TDM system .

Carrier synchronization can be achieved, even with low-cost local oscillators at user (ground) terminal, by using some suitable FERT schemes (e.g. the one proposed in Ref. 4), whilst clock coherency is a more delicate topic which can be addressed, at present status of technology, with some kind of "master-slave" clock synchronisation. Little complication on the user terminal equipment is needed, whilst the on-board hardware complexity can be drastically reduced (up to about 50% the initial value).

The exposed considerations derive by some preliminary investigations done by the authors for International Telecommunications Satellite Organisation (INTELSAT) and European Space Agency (ESA).

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