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DIGITAL MULTICARRIER DEMODULATOR FOR ADVANCED COMMUNICATION SYSTEMS

Enrico DEL RE, Romano FANTACCI

Dipartimento di Ingegneria Elettronica, Università di Firenze
Via S. Marta 3, 50139 Firenze, Italy
Telex 580681/UNFING, Telefax +3955 460392

In this paper, a multicarrier demodulator (MCD) suitable for advanced satellite digital communications is presented. This system permits the direct on-board interface of FDMA and TDMA communication links by using digital signal processing techniques. Two main functions are implemented by a MCD: the demultiplexing (DEMUX) and the demodulation (DEMOD). We focus here only on a digital implementation of the MCD considering its advantages, flexibility, better performance and VLSI integrability.

1. INTRODUCTION

The development of space communications has required new digital communication systems using efficient modulation techniques, and satellites with on-board processing for a higher system efficiency. In particular, the on-board signal processing offers several advantages to satellite communication systems; an interesting feature is the separation of the uplinks and downlinks which permits their distinct and independent optimization. Regenerative satellites allow different modulation and multiple-access schemes to be employed in the uplinks and downlinks; for instance, uplink random access and downlink TDMA techniques can be envisaged [1]. Alternatively, for mobile communication services, the use of uplink FDMA techniques with the inherent low-cost earth stations, and downlink TDMA techniques that can fully exploit the satellite transponder output power without intermodulation, is a very interesting and attractive solution. However, the feasibility of this approach depends on efficient means to directly interface the two multiple access formats on-board the satellite. The on-board system implementation complexity (including the VLSI design) and power consumption are, of course, of primary concern. The on-board processing system receives an input FDMA signal and supplies an output to interface the TDMA or TDM links; therefore, it must accomplish the function of the separation of each individual radio channel and its demodulation. An appropriate name for the on-board processing system is the 'multicarrier demodulator' (MCD). Two main functions are implemented by a MCD: the demultiplexing (DEMUX) and the demodulation (DEMOD).

We focus here only on a digital implementation of the MCD because in perspective it offers several advantages such as flexibility, VLSI integrability, better efficiency. The operation of the DEMUX is to separate the individual input FDMA channels and to supply each of them to a demodulator input for the appropriate down-conversion to baseband. Therefore, in principle, its operation corresponds to a bank of band-pass filters followed by a down-converter. By digital means the down-conversion can be appropriately implemented by a decimation operation. On the other hand, the direct implementation of a bank of digital filters is not the most convenient solution. This paper describes an efficient approach to the digital implementation of the DEMUX, based on the analytic signal method [2]. This method fully exploits the properties of the analytic signal and employs the tools offered by the digital signal processing techniques to present a solution to the DEMUX that is modular, efficient, flexible, of relatively low complexity and suitable for VLSI integration. These characteristics can be achieved because the analytic signal approach directly leads to a per-channel and high modular structure, and is highly flexible allowing to vary on demand the bandwidth assigned to each channel, simply by switching to a suitable new set of system parameters. Moreover, this method relaxes the requirements on the input analog anti-aliasing filter. Further a certain degree of integration of the DEMUX and DEMOD functions is conceivable as will be shown later. A coherent demodulation is usually employed in satellite communications in order to achieve the required bit-error-rate (i.e. 10^{-6} to 10^{-9}) with an acceptable signal-to-noise ratio. The performance of a coherent demodulator depends rather critically on the design of the synchronization circuit employed to estimate the received carrier phase and bit synchronization reference from the received signal. The implementation structure of the MCD system considered herein is shown in Fig. 1. The digital architecture

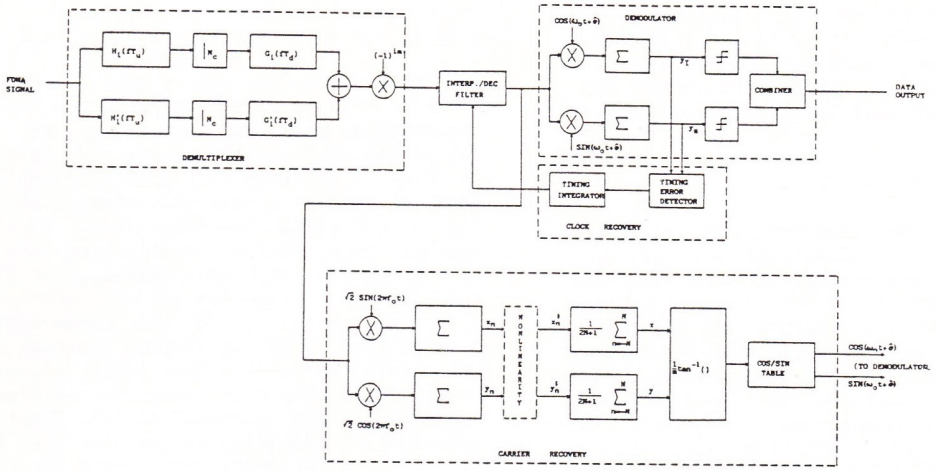

Fig. 1 - MCD structure.

of the proposed MCD can be adapted to different digital modulation techniques; therefore, we focus here only on the application for QPSK signals, owing to the interest of this modulation scheme in satellite digital communications. The carrier recovery circuit has been implemented according to the non-linear estimation method proposed by Viterbi [3]. This method has been selected because it achieves a good estimate accuracy, is less sensitive to a finite arithmetic implementation and requires a short and definite acquisition time. Moreover, it can be applied to continuous as well as burst mode carriers and a certain degree of integration of the demultiplexer implemeted according to the analytic signal method is conceivable (i.e. the separation of the in-phase and quadrature components of the received QPSK signal). The clock recovery circuit is assumed to be implemented by the clock estimation method proposed by Gardner [4]. This clock recovery method has been selected because its estimation operations are independent of carrier phase and some degree of integration of demultiplexer and clock recovery functions is possible: for instance, the required data filtering function (i.e. interpolator/decimation and pulse shaping) can be performed by the low-rate stage of the demultiplexer. In conclusion, the multicarrier demodulator described in this paper represents a complete solution for a processing system interfacing FDMA and TDM links. Its design has been carried out, in particular, aiming at its possible implementation by means of custom VLSI digital circuits.

2. DEMULTIPLEXER

The demultiplexing of a FDMA signal can be performed following two basic approaches: block methods and per-channel methods. We focus here on the analytic signal approach [2] which is a per-channel method that avoids any digital product modulator and has the specific feature to relax the filter specifications, thus achieving a lower implementation complexity with respect to other per-channel approaches. Further, the analytic signal approach directly leads to a per-channel and highly modular structure: this structure is directly matched to the per-channel implementation of the demodulators, and a certain degree of integration of the DEMUX and DEMOD functions is conceivable. The principle of operation of the analytic signal method has been reported in [2]. The structure of the DEMUX according to the analytic signal method is shown in Fig. 1 (Demultiplexer section) [2],[5],[6]. The FDMA input signal, after appropriate analog down-conversion of the received signal to a low frequency range, is sampled according to the sampling theorem [7] at the high-rate frequency $f_u=1/T_u$ and processed in order to obtain N_c baseband digital signals, each sampled at the low-rate frequency $f_d=1/T_d=f_u/N_c$, N_c being the number of FDMA multiplexed channels. In Fig. 1, $H_i(fT_u)$, $H_i^!(fT_u)$ represent the conjugate symmetric and antisymmetric parts, respectively, of the high-rate complex bandpass filter $H_i(fT_u)$ which can be regarded as a frequency translated version of a lowpass prototype $H(fT_u)$ such that [2]:

$$(1)\quad H_i(fT_u)=H_i(fT_u)+jH_i^!(fT_u)=H[2\pi(f-iW-W/2)T_u] \qquad i=1,2,\ldots N_c$$

where W is the channel spacing. In the same figure, $G_i(fT_d)$ and $G_i^!(fT_d)$ represent the conjugate symmetric and antisymmetric parts, respectively, of the complex low-rate filter $G_i(fT_d)$ which can be defined as [2]:

$$(2)\quad G_i(fT_d)=G_i(fT_d)+jG_i^!(fT_d)=G\{[f-(-1)^i W/2]T_d\} \qquad i=1,2,\ldots N_c$$

Thus, each filter $G_i(fT_d)$ is related, according to eq. (2), to a lowpass prototype $G(fT_d)$. It

can be noted from eq. (2) that the number of different filters $G_i(fT_d)$ is actually two: one for the odd channels and the other for the even channels. Taking into account eqs. (1) and (2), we have in the frequency domain [2],[5]:

$$(3)\quad X_i(fT_d) = S[(ft_d + i/2)/N_c]$$

according to the implementation structure shown in Fig. 1 (Demultiplexer section). The terms $S(fT_u)$ and $X_i(fT_d)$ in eq. 3 represent the spectrum of the input signal and the spectrum of the i-th output of the DEMUX, respectively. It must be noted that a decimation factor equal to the number N_c of multiplexed channels must be used and that only processing of real quantities is required. The overall number of multiplications required per input channel and per second M to implement the demultiplexer according to the analytic signal approach can be estimated as a function of the channel spacing W, the number of channels N_c and the filtering one-sided bandwidth B as [6]:

$$(4)\quad M=W^2[W(N_c+4)-2B(N_c+2)]/[(W-B)(W-2B)]\cdot \cdot \{-2[\mathrm{Log}\ 5\delta_1\delta_2]/3\}$$

where the terms δ_1 and δ_2 denote the overall acceptable in-band and the out-of-band ripples, respectively, derived according to given system specifications; for example, a filter design procedure is reported in [6]. It results from eq. (4) that for specified values of B and N_c an optimum value for the channel spacing W_o can be found in order to achieve the lowest M. However, taking into account that for the subsequent demodulation operation an integer number of samples per symbol is convenient a suboptimum value of W closest to W_o is generally used which guarantees this condition. Thus, a suitable choice of the DEMUX output sampling frequency 2W turned out to be equal to 3 samples/symbol.

3. DEMODULATOR

In this section, the digital coherent demodulator for QPSK signals is considered. A digital coherent demodulator is comprised of three parts: i) the carrier recovery circuit; ii) the clock recovery circuit and iii) the data-decision circuit. The carrier recovery circuit is assumed to be implemented by the non-linear estimation method proposed in [3]. Fig.1 shows the general structure of the phase estimator considered herein (carrier recovery section), where in the dotted box we suppose to insert the two dimensional (complex) non-linear functions:

$$(5)\quad x'_n + y'_n = \rho_n^2\ e^{j4\Phi_n}$$

with $\rho_n = \sqrt{x_n^2 + y_n^2}$ $\Phi_n = \tan^{-1}(y_n/x_n)$

In other words, for each symbol a rectangular-to-polar transformation is performed, multiplying phase Φ_n by 4, and squaring ρ_n. We avoid describing the non-linearity in this manner in Fig. 1, because in a practical implementation it becomes a read-only-memory, transforming a quantized two-dimensional vector into another such vector. Multiplying the phase by 4 along with the final operation of dividing the $\tan^{-1}$ function by 4, gives rise to a $\pi/2$ ambiguity in the phase estimates. A practical QPSK modulation systems adjusts for this by coding the data transitions, rather than the data themselves (differential encoding), and performing the function of differential decoding at the receiver. Suppose we wish to estimate the phase at the midpoint of the estimation interval T_E, which encompasses (2N+1) QPSK symbols (each T long), the implementation complexity of the proposed carrier phase estimator can be derived as:

$$(6)\quad M_v = 3\ R\ \text{mults/sec.}\quad A_v = (2N+1)\ R\ \text{adds/sec.}$$

being R the transmission rate, and 2 samples per symbol have been assumed. These two samples per symbol can be derived through an interpolator (by a factor 2) and decimator (by a factor 3) digital filter as shown in Fig. 1. The implementation complexity of this interpolator/decimator digital filter can be evaluated as 13 R mults/sec. and 12 R adds/sec. The clock recovery circuit is assumed to be implemented by the clock estimation method proposed in [4]. The general structure of the clock recovery circuit is shown in Fig. 1 (clock recovery section). The timing error detector operates upon samples and generates an error sample u(k) for each symbol. The detector algorithm is the following:

$$(7)\quad u(r) = y_I(r-\tfrac{1}{2})[y_I(r)-y_I(r-1)]+y_Q(r-\tfrac{1}{2})\cdot \cdot [y_Q(r)-y_Q(r-1)]$$

where the index r is used to designate the symbol sample number. The terms $y_I(m)$, $y_Q(m)$ denote the strobe values of the m-th symbol, i.e. the samples on which the symbol decision is made, and $y_I(m-\frac{1}{2})$, $y_Q(m-\frac{1}{2})$ represent the samples lying midway between the (m-1)-th and the m-th strobe sample. Thus, it can be pointed out that the proposed detector algorithm required only two samples per symbol and it can be shown that it is independent of carrier phase [4], so that timing lock can be achieved without depending upon prior carrier phase acquisition. The timing integration shown in Fig. 1 performs a timing error updating through the following equation:

$$(8)\quad w(r) = w(r-1) + u(r)$$

The implementation complexity of the clock recovery circuit can be derived through eqs. (7), (8), taking into account the implementation complexity required to split the received QPSK signal into its in-phase and quadrature components, as:

(9) M_C = 3 R mults/sec. A_C = 3 R adds/sec.

where, as for the carrier phase recovery, two samples per symbol have been assumed. The data decision is performed after splitting the received QPSK signal in its in-phase and quadrature components as shown in Fig. 1 (demodulator section), and it can be implemented by a threshold detector. The overall implementation complexity of the coherent demodulator can thus be derived as:

(10) M_V = 19 R mults/sec./ch.

M_A = 2(N+8) R adds/sec./ch.

4. SYSTEM DESIGN AND PERFORMANCE

In this section, the design of a MCD system is considered for different SCPC-FDMA channel numbers. The number of channels processed by the MCD influences the input sampling frequency and consequently the processing rate and the complexity of the first stage of the demultiplexer. In this paper, the number of channels N_C to be processed by the MCD has been selected taking into account the possibility of a variation of the transmission rate R in the range R to 32 R (with R = 137 kb/sec.). Thus, the number of channels N_C should allow to vary the transmission rate with the lowest possible impact on the overall MCD structure. In particular, a feasible constraint is to require that the input A/D converter sampling frequency (clock) should be held constant at its maximum possible value. Starting from these considerations, as the design goal, we have selected N_C = 96 at R = 137 kb/sec.; however, in the following, the cases N_C = 32 and 48 will be considered, since in this way it is possible to reduce the input sampling frequency and the complexity of the demultiplexer, thus achieving a sufficient flexibility for applications with higher bit rates. In the following, a QPSK modulation technique with occupied signal bandwidth (i.e. filtering one-sided bandwidth B) equal to 41 KHz at R = 137 kb/sec., is assumed to be used for data transmission. The demultiplexer design is first presented. The high-rate and low-rate lowpass prototypes have been designed as a FIR linear phase filter by using the equiripple method [8]. The required filtering specifications are reported in Tab. 1 for the considered values of N_C. In the same table, the number of coefficients required for the high-rate lowpass prototype $H(fT_u)$ and low-rate lowpass prototype $G(fT_d)$ in order to satisfy the corresponding filtering specifications is also reported. The demultiplexer finite precision design has been carried out in order to introduce at each demultiplexer output a degradation, with respect to an input signal-to-noise ratio SNR_i equal to 7.6 dB, less than 0.1 dB. The finite arithmetic wordlengths are reported in Tab. 2, and they actually introduce a degradation of 0.05 dB (at SNR_i = 7.6 dB). In Tab.4 the over-

Tab. 1 - Filtering specifications for the analytic signal approach.

	N_c	δ_1	δ_2	N° of coeff.
High-rate filter H	32	$1.41 \cdot 10^{-2}$	$1.41 \cdot 10^{-2}$	96
	48	$1.15 \cdot 10^{-2}$	$1.15 \cdot 10^{-2}$	156
	96	$8.11 \cdot 10^{-3}$	$8.11 \cdot 10^{-3}$	340
Low-rate filter G	32	$1.41 \cdot 10^{-2}$	$1.41 \cdot 10^{-2}$	18
	48	$1.15 \cdot 10^{-2}$	$1.15 \cdot 10^{-2}$	20
	96	$8.11 \cdot 10^{-3}$	$8.11 \cdot 10^{-3}$	22

Tab. 2 - MCD Finite Arithmetic Wordlengths.

A/D Converter	DEMUX						DEMOD
	High-Rate Filters			Low-Rate Filters			
b_q	b_c	b_m	b_a	b_c	b_m	b_a	b_e
8	8	11	8	8	10	8	6

b_q = input signal quantization wordlength

b_c = filter coefficient wordlength

b_m = filter arithmetic wordlength

b_a = filter output wordlength

b_e = carrier and clock recovery wordlength

Tab. 3 - Implementation complexity of the MCD shown in Fig. 1

N_C	DEMUX xR (mlt/s/ch)	DEMOD xR (mlt/s/ch)	OVERALL xR (mlt/s/ch)
32	99	19	118
48	145.5	19	164.5
96	288	19	307

Tab. 4 - MCD Loss Evaluation.

N° of channels N_C	Demud loss (dB)	Demod loss (dB)	Overall loss (dB)
32	0.2	0.4	0.6
48	0.2	0.4	0.6
96	0.2	0.4	0.6

all demultiplexer loss is reported for the considered values of N_C. These degradations have been derived following the procedure outlined in [6]; they are due essentially to the effects of the required decimation process and of a finite precision implementation of the demultiplexer [6]. The coherent demodulator has been implemented according to the structure presented in Sect. 3. The demodulator implementation complexity can be derived through eq. (10) and the values obtained for different N_C are reported in Tab. 3. In the same table the overall MCD implementation complexity is also reported and it can be noted that it approximatively increases with N_C. In order to derive the degradations introduced by the coherent demodulator we have evaluated first the degradations due to the phase jitter introduced by the carrier phase estimate and to a symbol timing offset introduced by the symbol timing estimate, by assuming them as two independent noise contributions. The loss due to a phase jitter can be derived through the following equation [9]:

$$(11)\quad \text{Loss(dB)} = 4.34\,(1+2\Gamma)[1+(1+2\Gamma)/2\beta]/\beta$$

where Γ is equal to SNR_i (=7.6 dB) and β for moderate and high signal-to-noise ratios can be assumed equal to $1/\sigma_\theta^2$ with σ_θ the root-mean-square (r.m.s.) value of the phase error: for the considered non-linear estimate method, in the steady state condition, it results less than 4° at SNR_i = 7.6 dB. It follows from eq. (11) a demod loss of 0.27 dB. The degradation due to the symbol timing offset has been derived according to a worst case analysis. The maximum symbol timing offset in a steady-state condition is equal to half the sampling interval normalized to the symbol time, i.e. 1/12 in our case. At this maximum time offset the actual degradation of a QPSK modulation can be estimated equal to 0.05 dB. In order to derive the overall degradation introduced by the coherent demodulator the effect of a finite precision implementation must be taken into account. By assuming to implement the coherent demodulator through the use of the finite arithmetic wordlength reported in Tab. 2, a degradation equal to 0.08 dB is obtained. The overall demodulator loss, including the degradation due to a finite precision implementation is reported in Tab. 4. In the same table the overall MCD degradation (demod loss plus demux loss) is also reported for the considered values of N_C. In conclusion, the multicarrier demodulator described in this paper represents an attractive solution for processing systems interfacing directly FDMA and TDMA links. It achieves a good performance with an acceptable on-board system implementation complexity. A further reduction in the overall implementation complexity can be achieved by integrating some demodulator and demultiplexer functions.

5. CONCLUSIONS

IN this paper, a multicarrier demodulator (MCD) suitable for advanced satellite digital communications has been presented. The proposed MCD has two parts: the demultiplexer (DEMUX) and the coherent demodulator (DEMOD). In particular, the DEMUX has been implemented according to the analytic signal approach leading to a per-channel structure that avoids any digital product modulator and any block processor. It has the specific feature to relax the filter specifications, thus achieving a lower implementation complexity with respect to other per-channel approaches. Further, the analytic signal approach is directly matched to the per-channel implementation of the demodulators; therefore, a certain degree of integration of the DEMUX and DEMOD functions can be obtained, thus lowering the overall system complexity. Another advantage of the analytic signal approach is its high flexibility: differently from other methods, in the case that some specific applications should benefit from the unequal channel bandwidth, the analytic signal structure could vary on demand the bandwidth assigned to each channel, simply by switching to a suitable new set of DEMUX parameters. In conclusion, the digital MCD system described herein represents an appropriate solution for advanced digital communication systems interfacing FDMA and TDMA links and, in particular, it has been carried out aiming at its possible implementation by custom or semicustom VLSI digital circuits.

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