Analytical Model of Power MOSFET Switching Losses due to Parasitic Components

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Abstract— **In this paper the effect of parasitic elements on the MOSFETs switching transient through a linear and time-varying electrical model is presented. In particular, the effect of non-linear junction capacitances and the stray inductances have been studied and compared in terms of switching loss and waveform overshoot and ringing. The results obtained with the proposed model are validated by comparison between the model implemented in Matlab/Simulink and LTspice simulations. Considerations about the impact of stray inductances and switching energy losses are conducted and some observations to reduce energy losses are proposed.**

Keywords — Power MOSFET; Switching Losses; Stray Inductance; Junction Capacitance; Parasitic Elements.

I. INTRODUCTION

Power density of electronic switching devices is continuously increasing thanks to the introduction of components able to work at higher switching frequency. Thanks to the introduction of wide bandgap (WBG) semiconductor power converters are nowadays able to work at higher voltages, temperatures and frequency than conventional semiconductor material. In particular, the possibility to work at higher operating frequency allows higher power density and therefore save space, material and therefore reduce costs. Thus, if working at higher frequency brings several benefits, more attention must be placed during the design step. Predicting the power MOSFET losses is of primary importance for an optimum thermal design of the heatsink or cooling system, a fundamental aspect in many different high power sector such as automotive, railway and avionics [1]-[6]. Switching power converter are commonly based on PWM DC-DC converters which are simple, require a low number of components, and are widely investigated [7]-[11]. However the operations of these circuits is largely affected by parasitic components introduced by actual devices utilized in assembly the converter circuits [14]-[19]. When these parameters are takin into account the analysis of the circuit become cumbersome and require computer aided techniques [20]-[27]. In literature several studies were made to estimate the power losses with different degrees of approximation. In [19], a simple method to get a first and fast estimation of power losses is shown. This approach can be useful to get a rough estimation, but it does not consider the parasitic components.

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In [28] the impact of nonlinear junction capacitance on switching transient and its modeling for Silicon Carbide (SiC) MOSFET is shown. Experiments show that without full consideration of nonlinear junction capacitances, some significant deviations between simulated and measured results will emerge in the switching waveforms.

In [29] a detailed study of SiC MOSFET switching characteristics is shown. The switching performance of SiC MOSFETs are evaluated, in terms of turn on and turn off voltage and current in relation to gate driver maximum current, gate resistance, common source inductance and parasitic switching loop inductance. In [30][31] useful parameter extraction sequence of a SiC MOSFET is presented. The procedure makes possible to find several characteristics parameters starting from electrical tests and datasheets information. In [32] a circuit-level analytical model is shown. In particular, this model takes MOSFET parasitic capacitances and inductances, circuit stray inductances, and reverse current of the freewheeling diode into consideration is given to evaluate the MOSFET switching characteristics.

In this paper, starting from the information in [6]-[33] a state-space linear and time varying MOSFET model able to consider the non-linear junction capacitance and the stray inductance is proposed. This model is implemented in Matlab/Simulink. The results obtained are validated on LTspice using an accurate model of SiC MOSFET provided from the manufacturer. Since junction capacitances are characteristic of the MOSFET more attention is focused to the effect of the stray inductances and how they interact with the capacitances. The results show how each inductance affect the turn-on and turn off transient in terms overshoot, ringing and power losses. Some designing good practice observation to reduce the stray inductance are proposed.

II. MOSFETS SWITCHING TRASIENT DESCRIPTION

Fig. 1 shows the current, voltage and power waveforms during turn-on and turn off transient of a power MOSFET as derived in [32] where a linear time-variant model of the device has been introduced to estimate the power losses starting from the characteristics reported in the datasheet. Both turn-on and turn-off can be divided in four main stages by considering the drain-to-source current I_{DS}, the drain-to-source voltage V_{DS}, the gate-to-source voltage V_{GS} and the gate current I_G. These

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waveforms are useful to estimate the power losses due to both conduction and switching.

Starting from [32], non-linear models of the parasitic capacitances of the MOSFET have been included in the switching model.

III. Analytical Model of the Switching Transient

Every stage can be modelled by a state-space representation. Being a time-variant model, some continuity conditions are necessary when a transition from a stage to another one occurs.

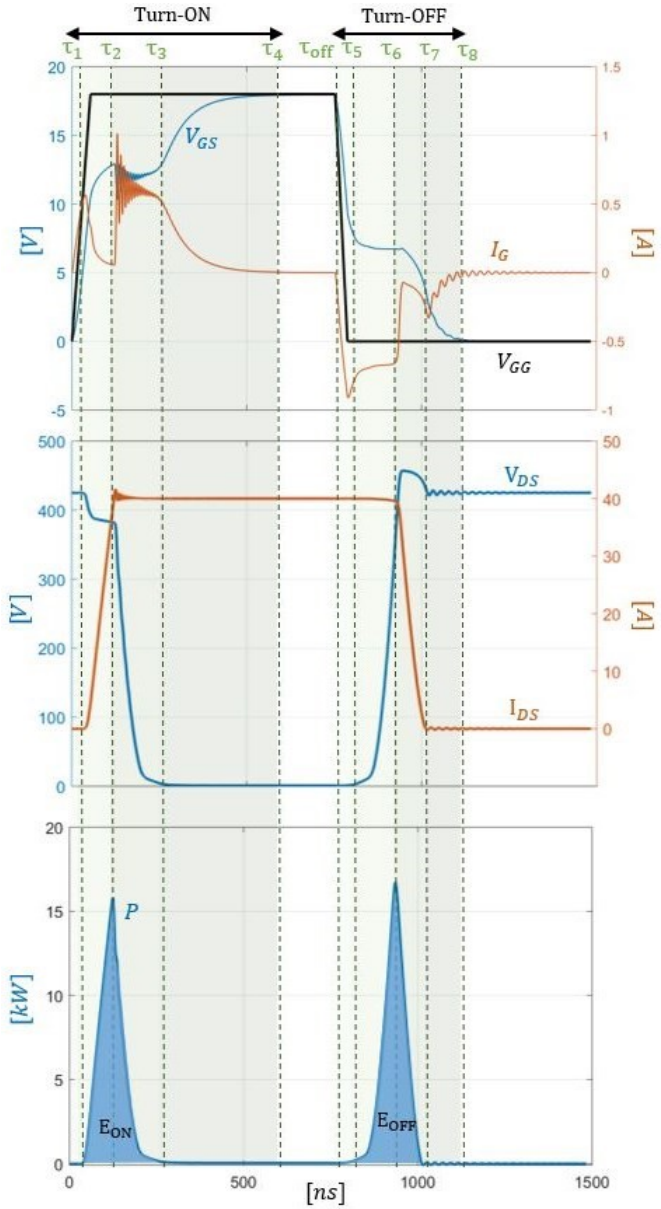

Fig. 1 Stages during turn-on and turn-off switching transient.

The general representation of the *i*-stage can be written as the following time-discrete Linear Time-Varying (LTV) dynamic system.

$$x_{k+1} = A_i k_k + B_i u_k \tag{1}$$

Where x_k and u_k are respectively the state and the input of the dynamic system at the instant time kT, for the integer index $k \in \mathbb{N}$ and the sample time T. The state matrix is A_i and the input-to-state matrix is B_i.

The State variable used in this paper is a five element vector $x = [V_{GS}, V_{DS}, V_{AK}, I_{DS}, I_G]$ where V_{GS} is the internal gate-to-source voltage, V_{DS} is the internal drain-to-source voltage, V_{AK} is the voltage of a diode placed between the drain and the main alimentation, I_{DS} is the drain-to-source current and I_G is the gate current. The input variable is $u=[V_{TH}, V_{TH,1}, V_{DD}, I_{DD}, V_{GG}]$, where V_{TH} $V_{TH,1}$ are the MOSFET threshold voltage [32], V_{DD} is the voltage supply, I_{DD} is the steady output current and V_{GG} is the driver voltage.

IV. Improved Cds and Cgd Non-Linear Model

The proposed model is time-varying since the parasitic capacitances are dependent from the applied voltage. These dependences can be found from the MOSFET datasheet and it is shown in Fig. 2. From the input capacitance C_{ISS}, the output capacitance C_{OSS} and the reverse transfer capacitance C_{RSS} can be found the gate-to-drain capacitance $C_{GD}=C_{RSS}$, the drain-to-source capacitance $C_{DS}=C_{OSS}-C_{RSS}$ and the gate-to-source capacitance $C_{GS}= C_{ISS}-C_{RSS}$. In [28] are modelled the effect of the non-linear capacitances on the transient characteristics of the switching process. The effect of the nonlinearity of C_{GS} can be neglected, therefore it is assumed constant [32]. On the other hand, if C_{DS} is assumed simply constant, there will be a serious deviation between the simulation and experimental results in switching transient. The factor that made the C_{DS} changes are substantially two: the drain-to-source voltage V_{DS} and the gate-to-drain voltage V_{GD}. In fact, as a junction capacitance, C_{DS} decreases significantly with the increase of V_{DS} since the depletion width changes with bias voltage. However, when MOSFET is turned ON or in the switching transient, C_{DS} will be impacted by the conductive channel and the non-uniform distribution of electrons caused by the gate-to-drain voltage V_{GD}, which is the second factor mentioned above. As shown in [28], the C_{DS} can be view as a linear combination of two parameters, $C_{DS,vds}$, a hyperbolic function of V_{DS}, and δ, which is a function of V_{GS}.

$$C_{DS} = C_{DS,vds} \cdot \delta_{ds} \tag{2}$$

where

$$C_{DS,vds} = \frac{C_O}{\sqrt{1+\frac{V_{DS}}{V_{bi}}}} \tag{3}$$

and

$$\delta_{ds} = \begin{cases} 1 & V_{GS} < V_{TH} \\ (1-\delta_{ds0})\, e^{-\alpha(V_{TH}-V_{GS})} + \delta_{ds0} & V_{GS} > V_{TH} \end{cases} \tag{4}$$

While δ_{ds0} can be approximately regarded as the attenuation ratio of C_{DS} on the condition that MOSFET is fully turned-ON, α is an adjustable parameter. Unfortunately, the actual value of C_{DS} in ON-state is difficult to measure as it is almost bypassed by the ON-state resistance. Thus, the two undetermined parameters δ_{ds0} and α, probably only can be obtained by finite-element analysis or experience at present.

Regarding the gate-to-drain modelling, its non-linearity is faced up in [30] where, in transient equations section of table 1, the value of the capacity is related directly to the drain-gate voltage.

$$C_{GD} = \begin{cases} C_{oxd} & V_{DS} < V_{GS} - V_{Td} \\ \dfrac{C_{oxd} \cdot C_{gdj}}{C_{oxd} + C_{gdj}} & V_{DS} > V_{GS} - V_{Td} \end{cases} \quad (5)$$

Where C_{oxd} is the Gate-drain overlap oxide capacitance and C_{gdj} is the gate-drain depletion capacitance and V_{Td} is the gate-drain overlap depletion threshold.

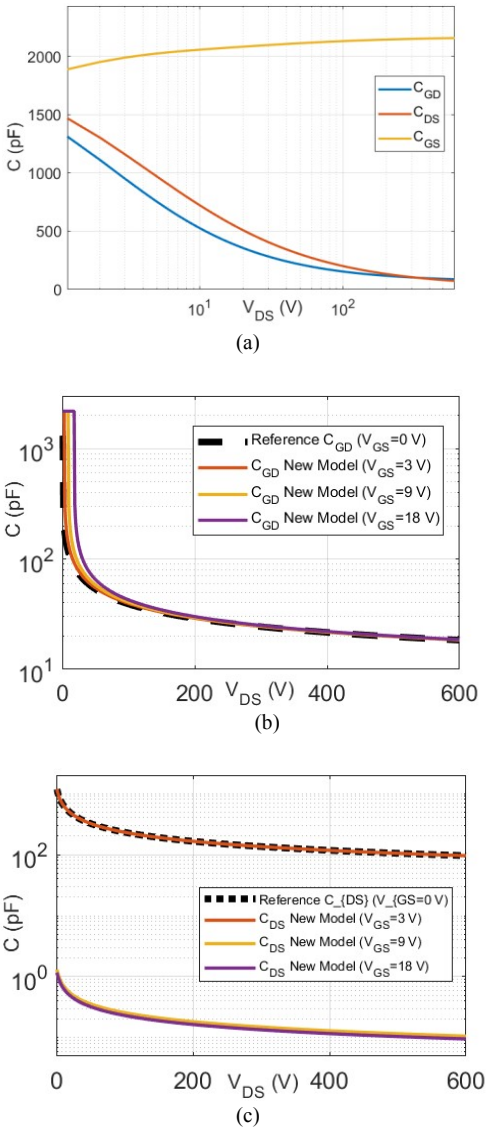

Fig. 2 Non-linear capacitances (a) Non-linear capacitances varying drain-to source voltage. Gate-to-drain capacitance C_{GD}, the drain-to-source capacitance C_{DS} and the gate-to-source. (b) Dependence of C_{GD} from gate to source voltage. (c) Difference between classical model presented in [2] and the new proposed model dependent from the Gate-to-Source voltage.

The C_{gdj} can be expressed as:

$$C_{gdj} = \frac{A_{gd} \cdot \varepsilon_{semi}}{W_{gdj}} \quad (6)$$

where A_{gd} is the Gate-drain overlap area, ε_{semi} is the semiconductor dielectric constant and W_{gdj} is the gate to drain depletion width body junction and can be calculates as

$$W_{gdj} = \sqrt{\frac{2\varepsilon_{semi}\left(V_{ds} + V_{Td}\right)}{qN_b}} \quad (7)$$

With q fundamental electronic charge and N_b base dopant density.

V. Model Validation

The analytical model of Power MOSFET mentioned in Section II-III-IV was implemented in Matlab-Simulink software. To validate the results obtained with the analytical model, several simulations were performed on LTspice. The chosen component is the SiC power MOSFET SCT3022AL since the manufacturer provide an accurate LTspice Model. This MOSFET has a conduction resistance r_{DS}=22mΩ, a drain-source breakdown voltage V_{DSS}=650V and a continuous drain current I_{DD}=93A. The MOSFET behaviour is analysed in a typical double pulse test system as shown in Fig. 3. Compared to the circuit presented in [32], the body diode of an SCT3022AL is used instead of a Schottky diode (C4D10120D). When the component is connected to the PCB, some parasitic inductances are created at the electric terminations. In this paper, it is assumed as nominal value L_S=9 nH, L_D=5 nH and L_G=15 nH. The comparison between the analytical model assuming V_{DD}=420V and I_{DD}=40A and the LTspice simulations are shown in Fig. 4. It's noticeable that the analytical model implemented in Matlab/Simulink is validated by the comparison between output MOSFET current, voltage and power delivered.

VI. Parasitic Inductances Effect on MOSFET Transient

After validating the model, a study on how the parasitic inductances affect the turn-on and turn-off transient is carried out. In the following analysis a single inductance is changed maintaining constant the other two to the nominal values.

A. Effect of the Parasitic Gate Inductance L_G

The waveforms for three values of gate inductance L_G are shown in Fig. 5, while the energy dissipated during a turn-ON and turn-OFF transient are summarized in Table I. This inductance tends to resonate with the MOSFET input capacitance, causing oscillations in the gate-to-source voltage V_{GS}.

TABLE I. Switching Energy Dissipation for Different Gate Inductance

Switching Energy	**L_G = 15 nH**	**L_G = 150 nH**	**L_G = 500 nH**
Turn-ON	149 µJ	176 µJ	159 µJ
Turn-OFF	145 µJ	98 µJ	87 µJ

For this reason, it is recommended to minimize L_G placing the gate driver as close as possible to the power device, ensuring the correct gating of the device and avoiding its spurious operation leading to undesirable faults. Apart from this recommendation, the influence of L_G on the V_{DS} and I_{DS} is limited if compared to the effect of the other two inductances.

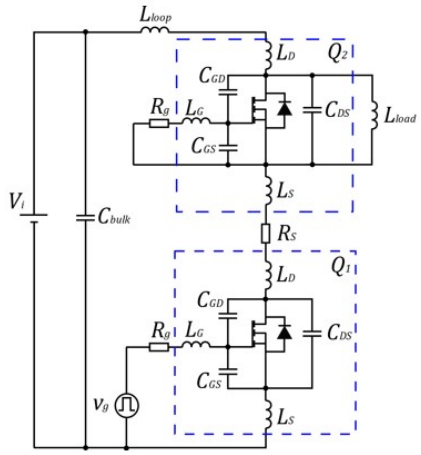

Fig. 3. Test circuit used to estimate the power losses.

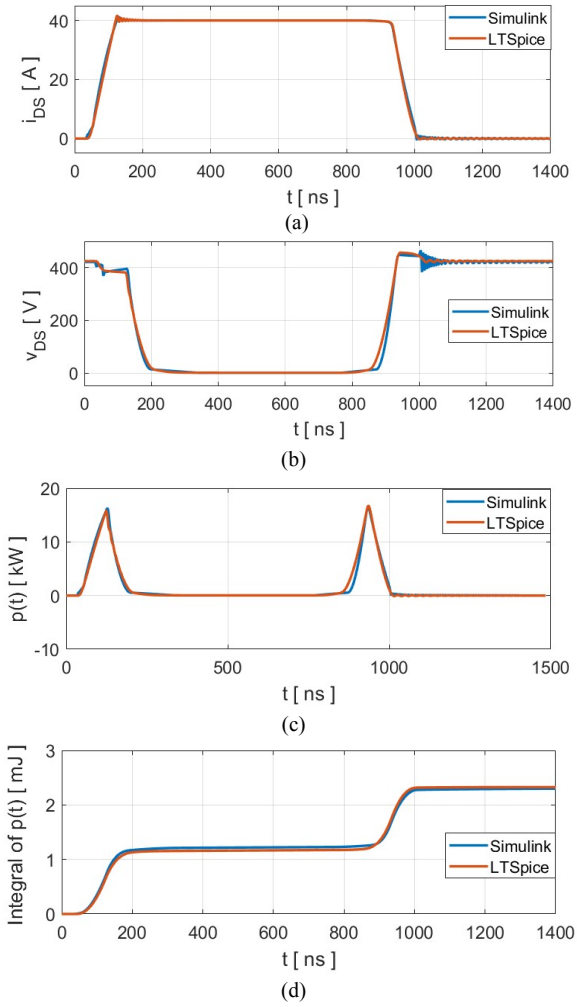

Fig. 4. Comparison between analytical model and LTspice simulations. (a) Drain-to-Source current I_{DS}. (b) Drain-to-Source voltage V_{DS}. (c) Istant power losses dissipation p. (d) Energy losses during the switching.

B. Effect of the Parasitic Drain Inductance L_D

The drain capacitance L_D, also called in literature switching loop capacitance, resonates with the MOSFET output capacitance and the diode junction capacitance during the switching transient. The oscillation produced are then coupled into the gate loop through the gate-to-drain capacitance C_{GD}. Thus, increasing L_D, ringing are introduced in V_{GS}, V_{DS}, and I_{DS}, as shown in Fig. 6.

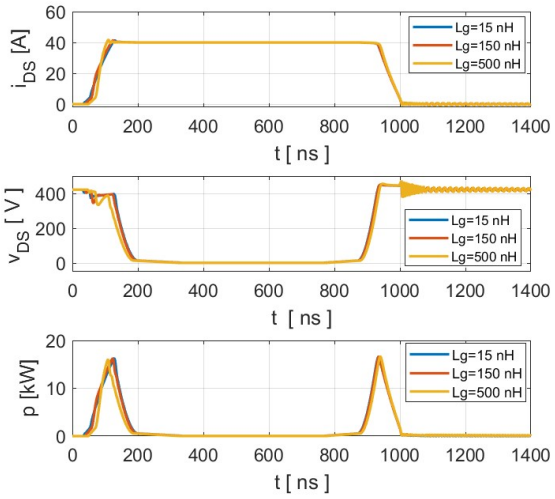

Fig. 5. Effect of gate inductance L_G. (top) Drain to source current I_{DS}. (middle) Drain to source voltage V_{DS}. (bottom) Istant Power p.

TABLE II. SWITCHING ENERGY DISSIPATION FOR DIFFERENT DRAIN INDUCTANCE

Switching Energy	L_D **= 5 nH**	L_D **= 50 nH**	L_D **= 100 nH**
Turn-ON	151 µJ	133 µJ	115 µJ
Turn-OFF	141 µJ	154 µJ	166 µJ

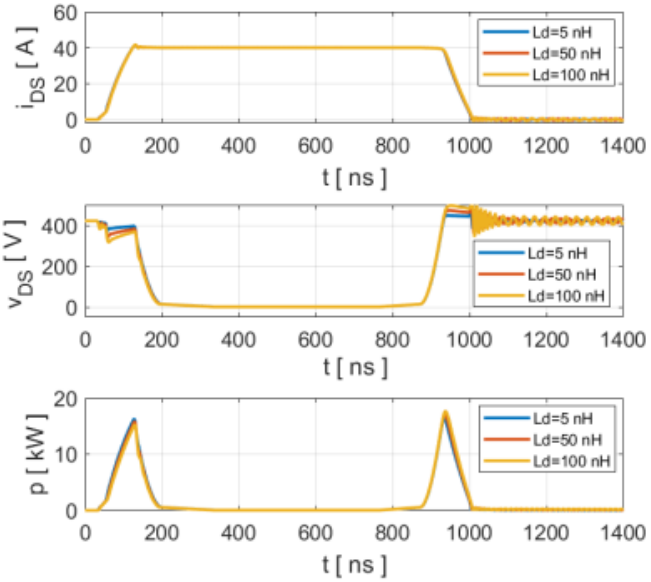

Fig. 6. Effect of gate inductance L_D. (top) Drain to source current I_{DS}. (middle) Drain to source voltage V_{DS}. (bottom) Istant Power p.

This inductance affects the switching transient more significantly than the gate inductance, causing even worse oscillations and stresses on the device. The voltage overshoot of V_{DS} increase by increasing L_D. For this reason, is recommended to reduce the drain loop inductance to ensure the safety of the MOSFET. Moreover, another effect of L_D is the current slew rate reduction leading to higher switching losses. The energy dissipated during a turn-ON and turn-OFF transient are summarized in Table II, varying L_D.

C. Effect of the Parasitic Source Inductance LS

The source inductance L_S creates a negative feedback from the switching loop to the gate loop. When the drain

current I_{DS} changes during the switching, the voltage across L_S counteracts the change of the gate voltage slowing down slew rate of the current I_{DS}. This behavior can be seen in Fig. 7 (a). On the other hand, these inductance does not affect the slew rate of the voltage V_{DS}. In addition, increasing L_S, the ringing across V_{DS} are reduced but higher switching losses occurs due to slew rate reduction. The energy dissipated during a turn-ON and turn-OFF transient are summarized in Table III, varying L_S.

TABLE III. SWITCHING ENERGY DISSIPATION FOR DIFFERENT SOURCE INDUCTANCE

Switching Energy	L_S **= 3.5 nH**	L_S **= 9 nH**	L_S **= 18 nH**
Turn-ON	102 µJ	151 µJ	241 µJ
Turn-OFF	110 µJ	142 µJ	217 µJ

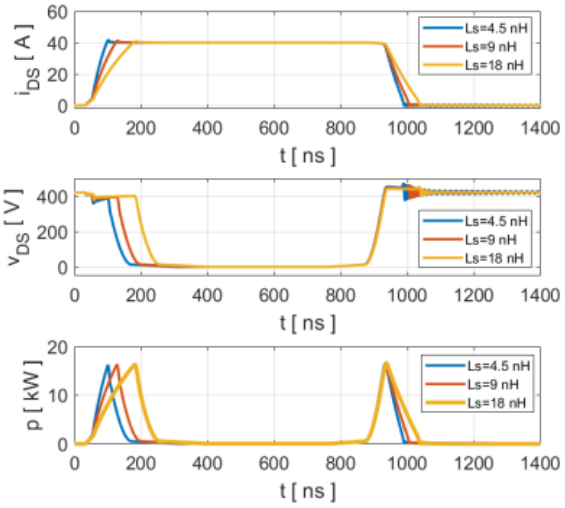

Fig. 7. Effect of gate inductance L_S. (top) Drain to source current I_{DS}. (middle) Drain to source voltage V_{DS}. (bottom) Istant Power p.

VII. Comparison and Summary

To have a complete overview of the stray inductances effects in SiC MOSFET, the energy losses in turn-ON and turn-OFF phases are calculated separately, varying the inductances L_G, L_D, L_S. The range of the stray inductances is appropriately assessed, referring to [31] and Table I, II, III. Fig. 8 shows that in both the transient phases, the variation of the gate stray inductance L_G contributes very few to the switching losses of the Sic MOSFET, while, the variation of the source stray inductance L_S highly affects the switching losses, especially for the turn-ON phase, as shown also in the Fig. 7. Despite the energy losses values during the turn-OFF is [1.0 – 1.4] µJ, while during the turn-ON higher [0.4 – 1.5] µJ. Therefore, it is important in the design to take care of on the connection of the source pin.

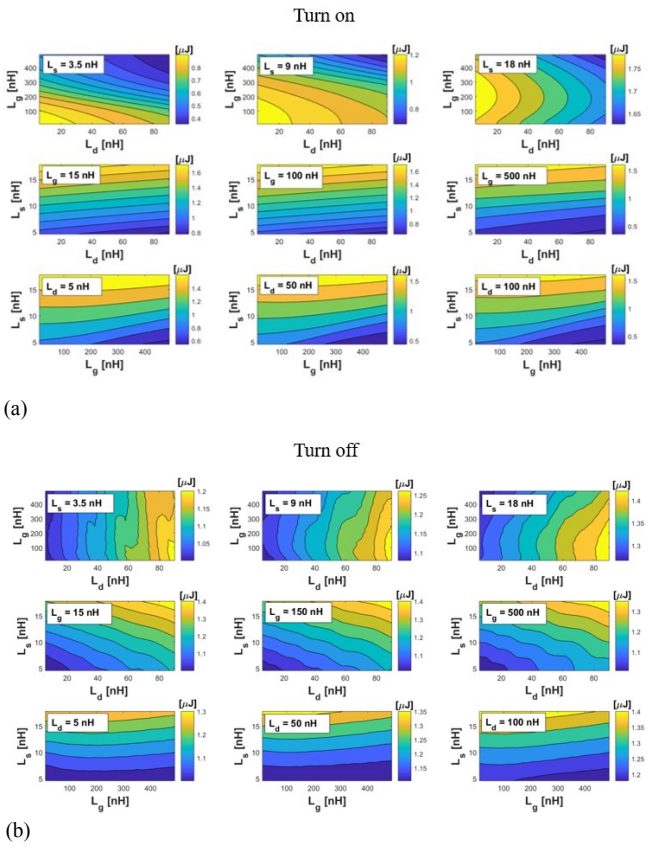

Fig. 8. Energy dissipated in analytical model of Sic MOSFET during the single Turn-ON transient (a) and Turn-OFF (b) transient, depending on stray inductance L_S, L_G, L_D.

Conclusions

The effect of stray inductances has been analytically analyzed considering the MOSFET non-linear junction capacitance. The results obtained are in good agreement with the LTspice model provided from the manufacturer. The results show that the source capacitance L_S affect the switching transient more than the others inductances: even small values produce significant negative effects. For this reason, during the design phase, the source connection is crucial to reduce the switching losses. On the other hand, the drain inductance L_D affect less than the waveforms, but it is the first responsible of the overshoot on V_{DS}. Therefore L_S, must be kept low to avoid that V_{DS} let reach values higher that the breakdown voltage. Finally, the gate voltage L_G affect less than all the turn-on and turn-off transient, but it is recommended to maintain low value to ensure the correct gating of the device and avoid its spurious operation leading to undesirable faults.

As future works the model will be improved coupling this electrical model with a thermal model. Indeed, in real applications, all the parameters of the model are temperature dependent. The coupling of an electric model and a thermal model can be useful to better understand the system performance and know the junction temperature of each switching device.

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