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A. Cidronali, G. Collodi, G. Vannini and A. Santarelli

A distributed modelling approach for micro- and millimetre-wave FETs is presented. Model identification is directly carried out on the bases of S-parameter measurements and electromagnetic analysis of the device layout, without requiring cumbersome optimisation techniques. Experimental results confirm that the model is consistent with device scaling.

Introduction: The development of high performance monolithic microwave integrated circuits (MMICs) requires global design procedures where not only the values of passive components, but also the active device geometry (e.g. number of fingers and gate width) represent available design parameters. In this context, robust scaling procedures for FET models are of key importance.

In this Letter, a new approach to FET model scaling for MMIC design is proposed which is based on an empirical distributed modelling approach [1 - 3]. In particular, model identification is carried out by means of accurate electromagnetic (EM) simulation and scattering parameters measured for a limited number of FET structures. On this basis, a characterisation of the 'active area' of the device is obtained which is consistent with simple scaling rules.
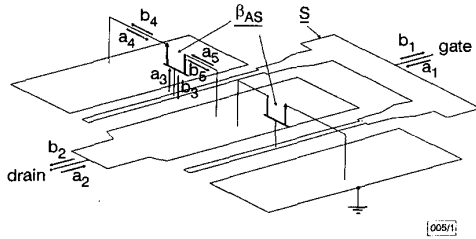

Fig. 1 *Structure of distributed model*

Empirical distributed model: The electron device is assumed to consist of an 'extrinsic passive structure' connected with a finite, suitable number of elementary 'intrinsic active slices' as shown in Fig. 1 for a two-finger FET where a single active slice per finger has been considered. As far as model identification is concerned, the extrinsic structure is characterised through its scattering matrix S (see Fig. 1) computed by means of EM simulation. This kind of analysis enables device geometry and material characteristics to be taken into account, for any given device structure and size, by means of a multiport S-matrix 'distributed' description. Thus, since electromagnetic propagation and coupling effects are accounted for by the passive structure, all the intrinsic devices are described by the same scattering matrix β_{AS} which can be identified once the scattering matrix α of the electron device has been measured. This identification procedure is well justified by the experimental results provided in the following.

The identification of the 3×3 matrix β_{AS}, which characterises the active slice, will be described for a two-finger FET where a single active slice per finger is considered as shown in Fig. 1. This choice, which does not limit the validity of the approach, has the advantage of simplifying the mathematical development and has been found suitable for FET modelling up to 50GHz. In particular, by denoting with $\tilde{S}$ the 5×5 matrix obtained from the 8×8 scattering matrix $\underline{S}$ of the extrinsic part, after the application of symmetry conditions deriving from the FET structure, it can be shown that

$$\underline{\beta}_{AS} = \left[\underline{\tilde{S}}_1 \cdot \left[\frac{(\underline{\alpha} - \underline{\delta})^{-1} \cdot \underline{\gamma}}{\underline{I}} \right]^{-1} \right]^{-1} \tag{1}$$

with

$$\underline{\tilde{S}}_{1_{i=1,\ldots,3;j=1,\ldots,5}} = \underline{\tilde{S}}_{i=3,\ldots,5;j=1,\ldots,5}$$

$$\underline{\delta}_{i=1,2;j=1,2} = \underline{\tilde{S}}_{i=1,2;j=1,2}$$

$$\underline{\gamma}_{i=1,2;j=1,\ldots,3} = \underline{\tilde{S}}_{i=1,2;j=3,\ldots,5}$$

where the port indexes are defined according to Fig. 1. In eqn. 1, $\underline{I}$ is the 3×3 identity matrix while $\underline{\alpha}$ is the 2×2 measured scattering matrix of the electron device. It is worth noting that model identi-

fication does not require either parameter optimisation or complex measurements.

Scaling rules for active slices: Experimental results show that the FET static currents and differential conductances deviate from a simple proportional relationship with device width. As an example, the saturated drain current and the static transconductance are plotted in Fig. 2 as functions of the total gate width for different GEC-Marconi MESFETs of the same wafer die (so that process dispersion is practically negligible). It is evident that although linear behaviour with gate width can be reasonably assumed, this is not purely proportional, as the linear regression does not pass through zero. A possible explanation could be related to the fact that the FET structure is not 'geometrically homogeneous' along the finger width, due to the gate feed and termination structures. These 'border' effects, which become more relevant at high frequencies, must be accounted for in the scaling rules. This can be done by introducing, under the reasonable assumption that border effects are independent of gate width, a correction term in the value of all the static and dynamic parameters. In particular, an equivalent admittance matrix Y_{AS} associated to the active slice width W_{AS} can be defined according to the following scaling rule

$$Y_{AS_{ij}}(\omega, W_{AS}) = \hat{Y}_{ij}(\omega) \cdot W_{AS} + C_{ij}(\omega) \qquad i,j = 1, \ldots, 3 \tag{2}$$

$C(\omega)$ being a width-independent fraction of the equivalent admittance matrix, which accounts for non-ideal, border-like effects.
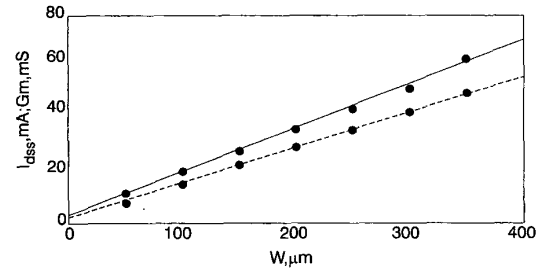

Fig. 2 *Linear regressions of measured I_{dss} and static transconductance Gm against total gate periphery*

———— I_{dss}
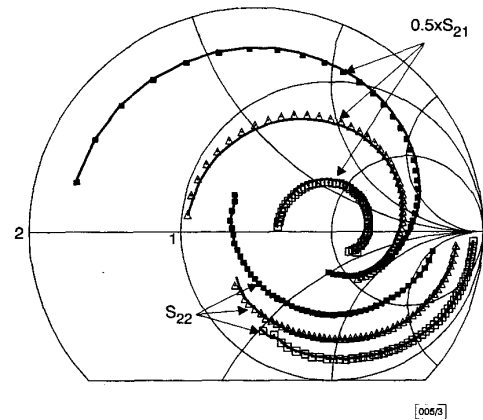— ·· — · — Gm

Fig. 3 *Measured and simulated S_{21} and S_{22} for three different FETs*

■ $2 \times 150\mu m$
△ $2 \times 75\mu m$
□ $2 \times 25\mu m$

Experimental results: Different GEC-Marconi MESFET structures were measured and simulated to validate the proposed approach. More precisely, the S matrices of the extrinsic passive structures were computed, on the basis of foundry process parameters and device GDSII files, using the em™ Sonnet electromagnetic simulator. The scattering parameters of the electron devices were measured directly on-wafer up to a frequency of 50GHz using an

HP8510C network analyser. Moreover, the model was implemented in the HP-MDS program for microwave circuit design.
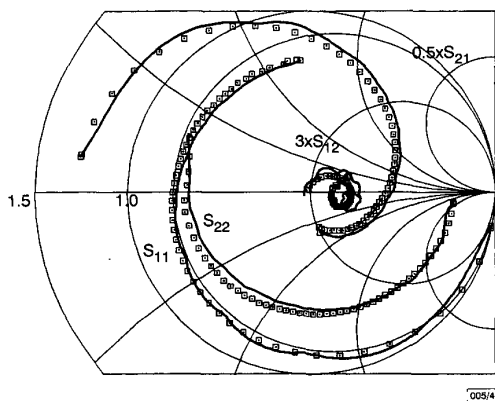

Fig. 4 *Measured and simulated S-parameters for 4 × 50µm FET*

☐ measured
—— simulated

On the basis of the identification procedures proposed and using the scaling rule of eqn. 2, the knowledge of the admittance matrices $Y_{AS}(\omega)$ associated with two FETs having different gate widths is sufficient to identify the matrices $\hat{Y}(\omega)$ and $C(\omega)$. In practice, since eqn. 2 is in any case an approximation, better prediction capabilities are obtained by evaluating the matrices $\hat{Y}(\omega)$ and $C(\omega)$ on the basis of a linear regression applied to device structures covering a wide range of gate widths. In particular, model identification was carried out using three MESFET structures: a 2 × 25µm, a 2 × 75µm and a 2 × 150µm device. Fig. 3 shows the comparison between the measured and simulated S_{22} and S_{21} parameters for these GaAs MESFETs. The good agreement confirms the accuracy of the proposed approach even when simple linear regression is adopted for model scaling.

To test the actual predictive capabilities of the proposed approach, the model was used to predict, on the basis of the active slice characterisation previously obtained, the electrical behaviour of a 4 × 50µm device (a structure significantly different from the structures used in the identification phase). Fig. 4 shows the measured and predicted S parameters for the 4 × 50µm GaAs MESFET, in the bias point $V_{ds} = 3V$, $I_D = I_{DSS}$. Similar good agreement has been found for other bias conditions.

A. Cidronali and G. Collodi (*Department of Electrical Engineering, University of Firenze, Via S. Marta 3, 50139 Firenze, Italy*)

G. Vannini (*Department of Engineering, University of Ferrara, Via Saragat 1, 44100 Ferrara, Italy*)

A. Santarelli (*CSITE, Italian National Research Council, Viale Risorgimento 2, 40136 Bologna, Italy*)

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Analytical model for output-buffered Banyan networks

K.S. Chan, S. Chan and K.T. Ko

A new model for evaluating the performance of output-buffered Banyan networks is proposed. Not only the number of packets stored in a buffer, but also the state of the buffer's head of line (HOL) packet ('new' or 'blocked'), are considered. Simulations are used to verify the accuracy of the model. The analytical result shows that, when the buffer size is large enough, say 10, the maximum throughput is close to saturation.

Introduction: Output-buffered Banyan networks use 2 × 2 knockout switches [2] and the buffer is placed at the output port of each switch element, as shown in Fig. 1. The simulation results in [2] show that the maximum throughput of a six-stage output-buffered Banyan with buffer size 4 is > 0.7. This is a significant improvement over input-buffered Banyan networks, making this configuration more suitable for asynchronous transfer mode (ATM) switches. The authors in [2] proposed an analytical model for output-buffered Banyan networks. The model only considers the number of packets stored in the buffer. The simulation and analytical results of this model do not match well, especially for small buffer size and heavy input traffic. This is because this model does not differentiate between the 'new' and 'blocked' head of line (HOL) packets.
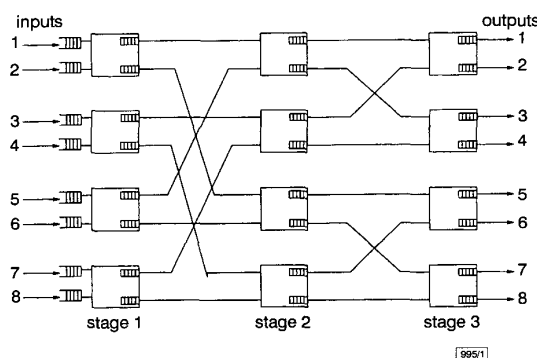

Fig. 1 *Architecture of 8 × 8 output-buffered Banyan network*

In [1], we proposed a more accurate analytical model for multiple input-buffered Banyan networks. In that model, we consider both the number of packets in the buffer of each stage and the state of the HOL packet in the buffer. In deriving the state transition probability, we have taken into account the influence of the HOL packet of the other buffer in the same switch element. Here, we modify that model for output-buffered Banyan networks. The results show that the model is more accurate than that in [2].

Analytical model: We consider an internal output-buffered Banyan network, with stage number m and buffer size B. Each switch element is a knockout switch, so if B is larger than 1, it is possible for the buffer to receive two packets simultaneously. Each buffer can only send the HOL packet during an operation cycle. Consider the input buffer as a buffer stage; a packet will go through m + 1 stages of buffers before leaving the switch. We label the buffers at the input stage as stage 0 buffers, the buffers at the output port of the first stage switch as stage 1 buffers, and so on. The buffers at the last stage are thus the stage m buffers. We consider the HOL packet in three states:

(i) state 'e': no packet in the buffer
(ii) state 'n': the HOL packet is different from that at the beginning of the previous operation cycle
(iii) state 'b': the HOL packet is the same as that at the beginning of the previous operation cycle

So, at the beginning of an operation cycle, a stage k buffer, $0 \le k < m$, may be in one of the $(2B + 1)$ possible states: $(0, e)$, $(1, n)$, $(1, b)$, ..., $(B-1, n)$, $(B-1, b)$, (B, n), (B, b). Here, we use (i,j) to identify a buffer's state, where i is the number of packets in the buffer, j is the state of the buffer's HOL packet, where $j \in \{e, n, b\}$. For a stage m buffer, because the HOL packet cannot be in state 'b', it