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MMIC Application of Heterostructure Interband Tunneling Diodes / A. CIDRONALI; V. NAIR; G. COLLODI; J. LEWIS; M. CAMPRINI; G. MANES; H. GORONKIN. - In: IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES. - ISSN 0018-9480. - STAMPA. - 51:(2003), pp. 1351-1367.

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02 May 2026

MMIC Applications of Heterostructure Interband Tunnel Devices

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***Abstract*—This paper deals with recent achievements in the field of an emerging technology termed the quantum monolithic microwave integrated circuit (QMMIC). QMMIC consists of a heterojunction interband tunneling diode and a high electron-mobility transistor monolithically integrated to obtain a new functional device. This technology enables the realization of low-voltage, high-density, and high-functionality circuits. A detailed description of the design and analysis techniques for several circuits such as an amplifier, an oscillator, and a mixer, along with the analytical treatment of the principle of operation are given in this paper. A number of prototypes implemented in InP technology constitute the proof-of-concept of the unique features of QMMIC circuit blocks for low-power wireless systems.**

***Index Terms*—Linear mixer, low power, monolithic microwave integrated circuit (MMIC), quantum-well devices, RF identification (RF ID), voltage-controlled oscillator (VCO).**

I. Introduction

IT IS WELL known that the development of new applications for information communication technology (ICT) is enabled by the introduction of new electronic systems. The ability in developing such a systems is directly related to the availability of new high-performance technologies both in digital and analog fields. Until now, in the digital circuit area, the increase in logic gate and bit density has followed Moore's law, which predicts a reduction by a factor of two in the minimum feature size every year. A similar trend has been observed in analog systems for features such as cutoff frequency, output power density, and low-power supply. In field-effect transistors, the reduction of the supply voltage and dynamic performance improvement has been obtained by reducing the gate length to a dimension of 100 nm. A natural and realistic question on dimension scaling is whether this trend will continue indefinitely. There are a number of technological challenges to be solved to allow conventional silicon and III–V compound semiconductors to reach nanometer dimension, as predicted by the SIA roadmap [1]. As operation frequencies and data transmission rates increase, these devices will reach an ultimate limit beyond which the conventional scaling approach will not be adequate. A change in paradigm is being sought in the electron-device concept to enable new systems and circuit functionalities using unconventional devices. A few emerging technologies are the outcome of this effort. Among others, single-electron FETs [2], molecular electronics [3], and resonant tunneling devices [4] have received a lot of attention by research institutes and industries. In particular, resonant tunneling devices appear to be a technology closer to introduction into commercial products.

Tunnel diodes (TDs) have been used to demonstrate numerous applications and potential market opportunities, including digital-to-analog converters, clock quantizers, shift registers, and ultra low-power SRAMs [5]. All these applications derive benefit from the inherent bi-stable behavior of the TD and utilize the negative differential resistance (NDR) to increase the transition speed between the two stable states. In the microwave realm, although TDs in theory promise medium-noise amplifiers, low-noise converters, and low-cost oscillators, these circuits have never achieved the high volume of usage, which one would have expected on the basis of the claims being made [6]. This is due primarily to the technological and design issues, which still have to be solved.

Enhancement in semiconductor growth techniques, in particular molecular beam epitaxy (MBE), has lead to an improvement in device quality and performances, and has introduced new families of tunneling devices. One of them is the family of the heterojunction resonant interband tunneling diodes (HITDs or RITDs), which makes use of resonant interband tunneling through potential barriers. These devices are interesting because of their high peak-to-valley current ratio (PVCR) and the large voltage span of the NDR region. A recent advancement in this class of devices is the monolithic integration of the TD into the structure of a three-terminal device, resulting in a novel NDR device. One of these new three-terminal device is called the heterojunction interband tunneling FET (HITFET) and its third terminal can be used as a gate control [7].

A number of significant applications of tunnel-diode-based monolithic microwave integrated circuits (MMICs) has demonstrated the potential for high-speed low-power consumption operation. The main applications already implemented are mixers [8], frequency multipliers [9], and oscillators [10]. The TD has also been used to provide a proof-of-concept of new circuits, such as the monolithically integrated bidirectional amplifier [11], which reduces the circuit complexity and increases the performances of RF identifications (RF IDs). Some applications are enabled by HITD and HITFET technology, but many of the results presented in the research are valid for all the technologies able to implement two- and three-terminal tunneling devices.

Manuscript received August 8, 2002.

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Digital Object Identifier 10.1109/TMTT.2003.809175

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TABLE I
SEMICONDUCTOR STRUCTURE OF AN InP

Layer	Semiconductor	Thickness	Doping		
Top Contact (Anode)	$In_{0.53}Ga_{0.47}As$	100 nm	p^{++}	C	1.3535×10^{20}
Barrier	$In_{0.52}Al_{0.48}As$	2 nm	nid	-	-
Well	$In_{0.53}Ga_{0.47}As$	4 nm	nid	-	-
Ohmic contact	$In_{0.52}Al_{0.48}As$	50 nm	n^{++}	Si	2.0×10^{19}
Bottom Contact (Cathode)	$In_{0.53}Ga_{0.47}As$	-	n^{++}	Si	2.0×0^{19}
Substrate	InP	-	nid	-	-

TABLE II
SEMICONDUCTOR STRUCTURE OF AN SiGe TD

Layer	Semiconductor		Thickness.	Doping		
Cap	Si	Stressed	4 nm	n^+	As	3×10^{18}
Emitter	$Si_{0.8}Ge_{0.2}$	Relaxed	50 nm	n^+	As	3×10^{18}
Spacer	Si	Stressed	10 nm	nid	-	-
Barrier	$Si_{0.4}Ge_{0.6}$	Stressed	2 nm	nid	-	-
Well	Si	Stressed	3 nm	nid	-	-
Barrier	$Si_{0.4}Ge_{0.6}$	Stressed	2 nm	nid	-	-
Spacer	Si	Stressed	10 nm	nid	-	-
Buffer	$Si_{0.8}Ge_{0.2}$	Relaxed	10 nm	nid	-	-
Collector	$Si_{0.8}Ge_{0.2}$	Relaxed	900 nm	n^+	As	3×10^{18}
Buffer	$Si \rightarrow Si_{0.8}Ge_{0.2}$	Relaxed	3000 nm	nid	-	-
Substrate	Si (100)	Relaxed	-	n	As	-

The paper is structured as follows. In Section II, the most common semiconductor structures for resonant tunneling diodes (RTDs) and RITDs are reviewed and a brief description of the physical models is given. Also presented is a modeling method suitable for both small- and large-signal applications. In Section III, a description of the microwave signal sources based on the HITFET along with a detailed treatment of design issues and constrains is given. Applications to active antenna are briefly discussed. Section IV discusses the design of a bidirectional amplifier and describes its exploitation in an RF-ID system. Finally, in Section V, a frequency converter and its inherent linearity are shown. The exploitation of the frequency-conversion properties for applications in envelope detectors and radiometry is also discussed in this section. All the applications are supported by a complete set of experimental data, which aid in the assessment of the strengths and weakness of quantum monolithic-microwave integrated-circuit (QMMIC) technology.

II. DESCRIPTION AND MODELING OF TUNNELING DIODES

A. Semiconductor Structures

The semiconductor structures of TDs used for practical high-speed or microwave applications are mainly based on heterostructure materials, which are either Si or III–V based. In Tables I and II, the semiconductor structures of state-of-the-art TDs implemented in InP and Si technologies are reported. In the case of Si, the semiconductor structure is based on the relaxed SiGe buffer that is commonly referred to as a virtual substrate.

In the case of the structure delineated in Table I, an optimization of the geometrical and doping parameters is required to reach the best tradeoff between peak current and the PVCR. The physical mechanism behind the dependence of the PVCR from the well thickness and barrier composition can be described only qualitatively by *ab-initio* models. For example, see the coherent model for interband tunneling based on the two-band equation system developed by Kane [14] and the kinetic model for intraband tunneling which makes use of the Wigner function [15]–[18]. As a consequence, experimental determination of device characteristics have to done to optimize the performance. Fig. 1(a) reports the experimental results of this optimization. This figure shows the sensitivity of peak current density and PVCR with respect to quantum-well width. From the comparison of the two curves, an optimum value for the well thickness was determined to be 4 nm. Fig. 1(b) reports a further example of the TD's I–V characteristic optimization, namely, the dependence of current density on the barrier composition and doping of the p-type semiconductor. It is observed that the peak current density is two times higher for InP, which has a lattice-matched barrier layer like InAlAs, compared to InP, which has a wider barrier layer like AlAs, which is not lattice matched. A similar optimization for the RF performance is not feasible due to complexity of physical processes involved. However, from a circuit design point-of-view, a set of characteristic figures-of-merit based on the conventional equivalent circuit of TDs can be introduced as follows to select the proper device structure.

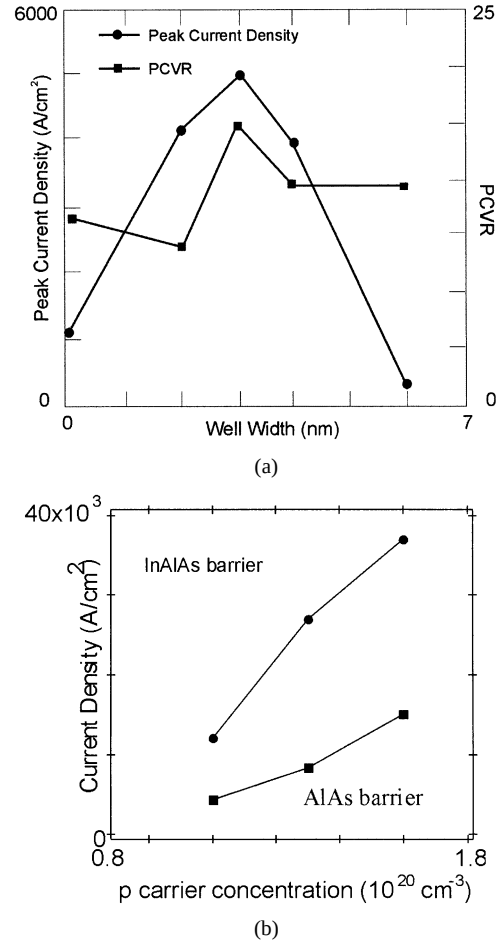


Fig. 1. (a) Peak current and PVCR as a function of the well width for the TD of Table I. (b) Peak current as a function of the doping for the TD of Table I in the case of the AlAs and InAlAs barriers.

- Current sensitivity:

$$\beta = \beta_o + \frac{1}{1 + \omega^2 C_{jv}^2 R_s R_j} \tag{1}$$

where β_0 represents the ratio of power to dc current at zero bias, C_{jv} and R_j are the junction capacitance and resistance at the operation bias voltage, respectively, and R_s is the series parasitic resistance.

- Noise figure:

$$\mathrm{NF} = 1 + \frac{e}{2KT}\left|R_j I_o\right| \tag{2}$$

where I_0 is the bias current. The main contribution to the device noise is shot noise, which is proportional to the current flowing through the junction.

- Negative-resistance cutoff frequency:

$$f_{ro} = \frac{1}{2\pi R_o C_{jv}}\sqrt{\frac{R_o}{R_s} - 1} \tag{3}$$

where R_o is the maximum magnitude of the NDR.

- Self-resonant frequency:

$$f_{xo} = \frac{1}{2\pi}\sqrt{\frac{1}{L_s C_{jv}} - \frac{1}{\left(R_o C_{jv}\right)^2}} \tag{4}$$

where L_s is the series parasitic inductor.

- Speed index:

$$\tau = \frac{Ip}{C_{jv}} \tag{5}$$

where Ip is the peak current.

- Maximum oscillator power:

$$P_{om} = \frac{3}{16}\left(V_v - V_p\right)\left(I_p - I_v\right) \tag{6}$$

where the indexes "v" and "p" denote the valley and peak values for currents and/or voltages.

In terms of the above-mentioned figures-of-merit, the main differences between Si- and III–V-based diodes lie in the inherent higher PVCR obtained in the III–V semiconductor structures. Even though an absolute maximum ratio of 144 has been reported [12] for III–V-based materials, values in the range of 30-50 are more typical for III–V interband semiconductor structures [4]. On the other hand, silicon devices hardly reach the value of four for interband structures and even worse for the intraband TDs. The higher PVCR of III–V TDs results in higher output power and higher frequencies of operation. The point of strength for Si TDs is the compatibility with the standard CMOS processes and the adaptability for mixed-signal circuits. Applications in this area are expected to emerge in the next few years.

As seen in (2), noise figure is proportional to the factor RjI_0, which is material related. Common values for that parameter are 2.4 for GaAs and 3 for Si, while a value of 1.36 can be achieved for refrigerated InAs [13]. The bias sensitivity parameter β_0 is slightly higher for GaAs than Si. Typical values of 10 and 8 V^{-1} were reported for GaAs and Si, respectively [13].

B. Comprehensive DC and RF TD Model

A general model to describe TDs implemented using different technologies will be introduced in this section. All TDs show strong nonlinearity in the dc current–voltage (I–V) characteristics, as well as frequency dependence of the impedance at different voltage biases. Figs. 2 and 3 illustrate these behaviors for an HITD. The real part of the impedance is negative at lower frequencies when the diode is biased in the NDR regime (from 0.05 to 0.65 V). This impedance is obtained from two-port S-parameter measurements of the diode.

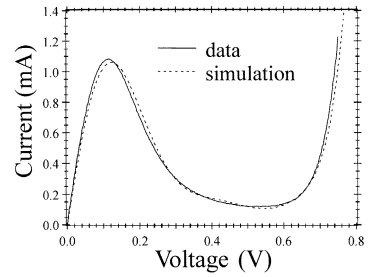


Fig. 2. DC current–voltage characteristics of a TD showing the NDR region. The solid line is experimental data and the dotted line is simulation.

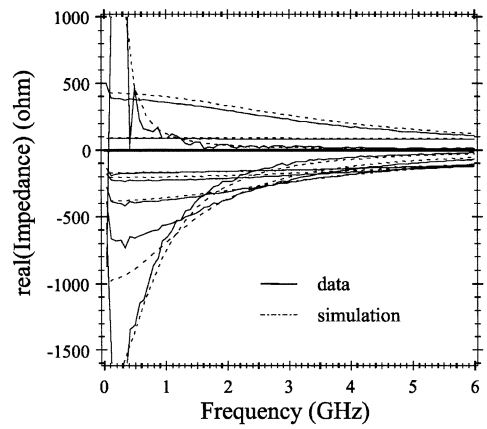


Fig. 3. RF characteristics of the TD of Fig. 1 showing the real part of the impedance as a function of frequency when biased at different voltages (from 0.05 to 0.65 V). The solid lines are experimental data and the dotted lines are simulation results from the new model (Section II).

A simple circuit, as shown in Fig. 4(a), allows modeling of the small-signal behavior of the device for a given bias. The resistance R_d, called the dynamic resistance, is negative when the diode is biased in the NDR region and is positive otherwise. C_d is the capacitance of the diode and R_s is a parasitic series resistance. This model is not adequate when TDs are coupled with other semiconductor devices to perform three terminal functions. This family of devices, such as HITFET, requires simulation of the dc and RF characteristics simultaneously. The RF properties of three terminal devices depend upon the distribution of dc voltage drops across the two terminals of the diode and the three terminals of the transistor. In order to overcome these limitations, a comprehensive dc/RF model for TDs that uses a voltage-controlled current source (VCCS) to model the diode properties has been developed [19]. This model is more than just a data-based large-signal RF model of a TD, as it is compatible with dc simulations. Significant physical insight into TD operation in analog circuits has been provided using this model. The basic idea behind the model, the use of a dependent current source, has been presented by Mizutz and Tanoue for digital applications [20]. Mizutz *et al.* describes a piecewise

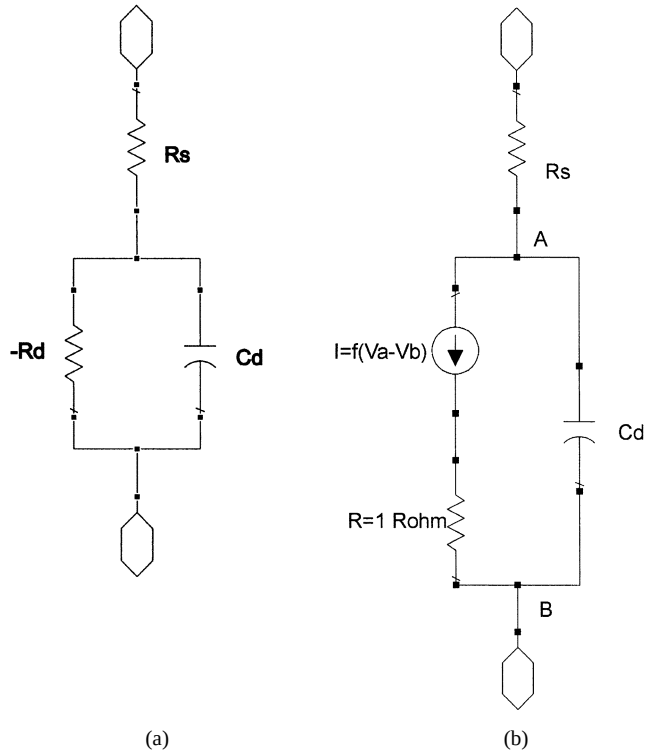


Fig. 4. (a) Small-signal RF model of a TD. (b) Comprehensive dc/RF model of a TD.

linear model for the current source that completely ignores the bias dependence of the RF properties within the NDR region. This model may be sufficient for digital applications where the TD switches across the NDR region rather than being biased in it. It is, however, not suitable for analog applications where the diode is biased within the NDR and, hence, the details of the NDR region are important. The new model developed in [19] is designed for analog RF and microwave applications. This model has been implemented in the Agilent Advanced Design System (ADS) simulation tool to facilitate the simulation of QMMIC circuits.

Fig. 4(b) shows the dc/RF model implemented in ADS formalism. The current I is a function of the voltage difference between the nodes a and b. This voltage is equal to the voltage drop across the 1-Ω resistance for any external applied bias, thus giving a self-consistent solution for the current. A polynomial fit to the dc current–voltage characteristics is used as the function $f(V_a–V_b)$. R_s and C_d have the same physical meaning as in the small-signal model (Fig. 3) and are determined from a small-signal measurement at a single bias in the NDR region. This model represents both the dc and RF properties of the diode with a high degree of accuracy. For dc simulation, the function $f(V_a–V_b)$ is a good representation of the IV characteristics since it is obtained from a fit to the dc data. The actual simulated current, however, is slightly different due to the presence of R_s in the model circuit. However, if $R_s \ll R_d$, which is typically the case, then the model is accurate for dc simulation. Fig. 2 shows excellent agreement between the dc IV data and the results of the model simulation. For the diode considered, R_s is 2.5 □ and is much smaller than R_d at any bias.

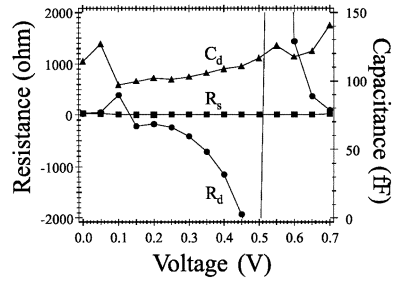


Fig. 5. Bias dependence of R_d, R_s, and C_d for the TD of Fig. 1.

During RF simulation R_s, C_d, and the VCCS combine to produce the appropriate diode impedance. The dynamic resistance R_d of the small-signal model is replaced by the VCCS. This substitution is possible and is successful because of the experimental observation of an excellent agreement between the resistances R_d obtained from RF measurements and the same derivative from the dc IV characteristics. Fig. 3 shows the comparison between the experimental data and the simulation results of the RF impedance-frequency characteristics of the TD of Fig. 2. The simulation and experimental data agree quite well over the entire bias range of the TD, in the NDR region, as well as out of it, and involving a wide change in the impedance values.

It has to be highlighted that the comprehensive dc/RF model does not account for the bias dependence of R_s and C_d. The variations in these parameters, in HITD, are much smaller than those in R_d, as seen in Fig. 5. The capacitance varies by approximately 15% over the bias range of interest. The model can be improved by introducing a bias-dependent capacitance to take this into account. The model also requires that R_s be at least ten times smaller than R_d. Typically, for diodes that show good performance, this requirement is easily met. If that is not the case, then it will be possible to obtain the correct dc behavior by fitting the VCCS function to a set of data deembedded from the effects of the Rs. Another limitation of the model is the necessity of obtaining an accurate curve fit to the dc IV data. The smoother the measured dc IV characteristics, the better the curve fit. This is not always possible because the NDR region of the TD is often unstable.

C. DC/RF Model Applications

As stated previously, the HITFET device is created by integrating TDs and FETs. The TD can be either connected to the drain, source, or gate terminal of the FET creating different types of HITFETs. To simulate the HITFET, the dc/RF model of the TD is used in conjunction with FET model. This simulation approach is used to investigate the relative advantages of the HITFET compared to the FET alone. The broad conclusions of this analysis are valid irrespective of the exact transconductance, gain, threshold voltage, or other properties of the underlying FET. The dc/RF model also allows the investigation of the optimum FET and diode characteristics that produce the best HITFET, as well as the matching requirements between the two devices.

In a source-HITFET, the TD is connected from the source terminal of the FET to the ground. As previously underlined, not

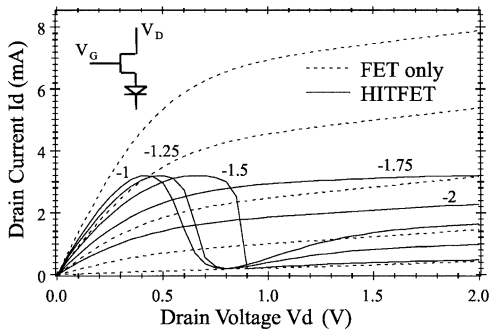


Fig. 6. Simulation of dc drain current versus drain voltage of a source HITFET at different gate biases as shown. Also shown are characteristics of the FET alone (dashed lines) at gate biases from -1.5 (top curve) to -2.5 V in equal intervals.

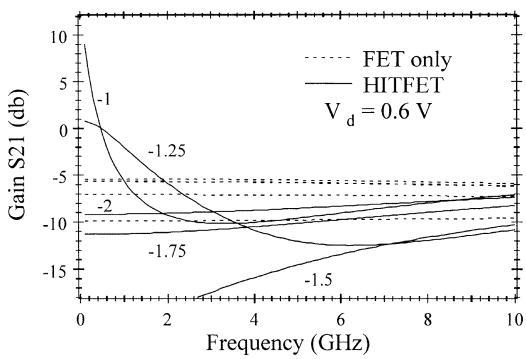


Fig. 7. Simulated gain S_{21} of a source HITFET and FET versus frequency for different gate biases.

only the s-parameters, the gain, and other RF characteristics of the HITFET depend upon the exact biases across the diode and the FET, but also the IV characteristic of the global device is affected by the interaction among them. Fig. 6 shows the simulated dc drain current versus drain bias characteristics of the source HITFET at different gate biases. Due to the presence of a TD in the source, the HITFET exhibits NDR characteristics (as seen for gate biases from -1 to -2 V). At lower gate biases (-1.75 and -2 V), the FET drain current is smaller than the peak current of the diode. At these gate biases, the TD acts as a simple resistor, there is no NDR, and the HITFET acts as an FET. The simulation shows that a proper matching of the FET saturation current and the diode peak current is required for the HITFET to show NDR. Fig. 6 also shows the characteristics of the FET alone. The effective gate–source voltage in a source HITFET is different from the voltage at the gate terminal due the presence of the diode between the source and ground. Hence, the FET only characteristics are shown for slightly lower gate biases (from -1.5 to -2.5 V). Fig. 6 shows that the HITFET exhibits NDR around the drain bias of 0.6 V. At these biases, the FET is in its linear regime. Fig. 7 shows the simulated gain S_{21} of the same source HITFET and FET at different gate biases where the drain bias is 0.6 V. At specific gate and drain biases, the HITFET displays a substantially higher gain than the FET alone. This higher gain, however, is very bias dependent (gate and drain) and has a very narrow voltage range in which it is high. This suggests that the source HITFET is more suitable for applications like oscillator rather than amplifiers where a flat gain profile is required to prevent distortion of the signal.

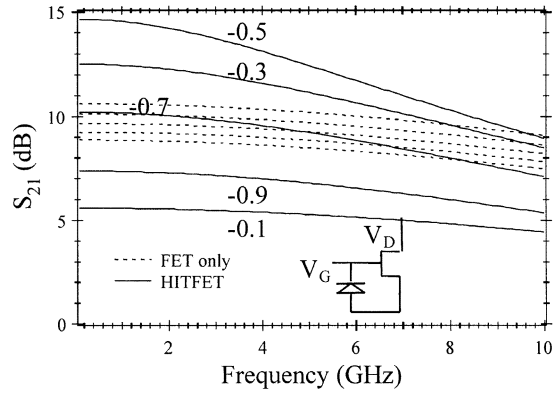


Fig. 8. Simulation of the gain $S21$ of a gate HITFET and an FET alone at different gate biases. The gate biases of the HITFET are clearly marked. The FET only characteristics are also simulated at the same gate biases; the lowest curve is at -0.9 V and the highest is at -0.1 V. The drain bias is 2 V.

In conventional FET amplifier circuits, the devices are biased in their saturation regime. The analysis shows that, if the FET is in the saturation regime ($V_d > 1$ V), then the TD is out of its NDR region (Fig. 6) and acts simply as a resistor pulling down the gain. The simulation of S_{21} at a drain bias of 2 V (figure not shown) shows that the source HITFET has lower gain than the FET alone at all gate biases. It can be concluded from simulation that the source HITFET thus has limited flexibility and advantages compared to the underlying HFET alone.

A second embodiment is a gate HITFET in which the TD is connected from the gate to the source of the FET (see inset of Fig. 8). The same terminal is used to bias the TD as well as the gate of the FET. The simulation (not shown) showed that the HITFET drain current versus drain voltage characteristic is almost identical to that of the FET only. This is expected because the diode voltage does not alter the voltage at the gate, drain, or source of the FET. The RF characteristics of the gate HITFET, however, do exhibit the effect of the NDR of the TD. Fig. 8 shows the gain S_{21} of the gate HITFET and the FET alone at different gate biases. The drain bias is 2 V and the FET is in its saturation regime. The gate HITFET exhibits a higher gain than the FET alone for gate biases when the diode is in its NDR regime. The S_{11} of the gate HITFET is also high (figure not shown). This enhancement is attributed to a resonance in the gate–source loop of the HITFET due to the negative impedance of the TD. This device is an ideal candidate for applications such as oscillators and mixers. Other MMIC circuits, such as amplifiers, using gate HITFETs have also been designed by having suitable matching circuits to stabilize the device while still benefiting from the higher gain.

In the following sections, detailed discussion of RF applications of the HITD and HITFET, including the drain HITFET, are presented.

III. HITD AND HITFET MICROWAVE SIGNAL SOURCES

A. Design Considerations Quantum Voltage-Controlled Oscillator (QVCO)

The InP HITFET allows implementation of efficient and ultra low-power QVCO. The key property of such a device is the tuning of the NDR by the gate voltage, which acts as a

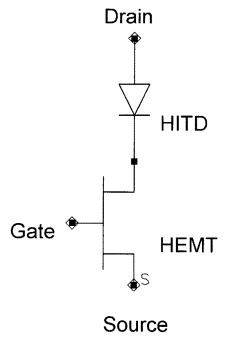


Fig. 9. Drain–HITFET schematic.

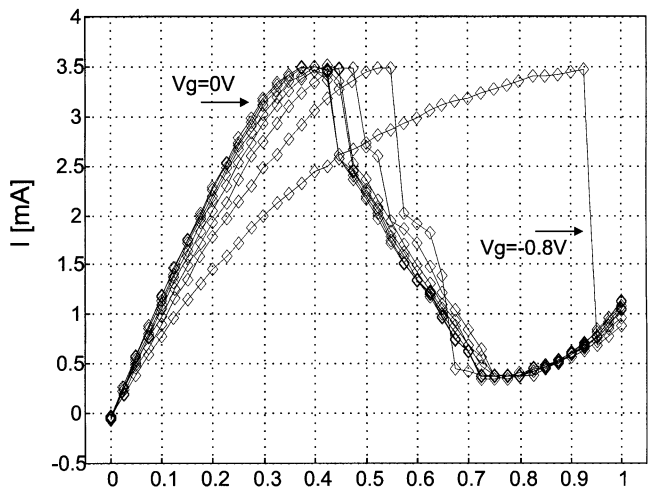


Fig. 10. $I\backslash V$ characteristic of the HITFET for $Vg = 0$, -0.8-V step 100 mV.

control voltage. As discussed in Section II, the interconnection between the HFET and HITD can be obtained through any of the three terminals of the HFET, but the most suitable configuration for the present application is with the HITD placed on the top of the drain electrode, namely, a drain HITFET (Fig. 9). Some technological solutions integrate a tunnel device directly on the drain n+ contact of the HFET obtaining a vertical monolithically integrated transistor [19]. In this study, a more conventional approach has been followed so the two devices are interconnected as different elements of the same circuit. In particular, the HITFET consist of a 2 $\times$ 25 μm high electron-mobility transistor (HEMT), while the HITD is a 2.5 $\times$ 2.5 μm^2. The employed HITDs show very high current densities (50–60 kA/cm^2), peak-to-valley current ratios between 10–15, and a maximum frequency of oscillation around 60 GHz (for the 2.5 $\times$ 2.5 μm^2 diode size) [22]. The IV characteristics of the HITFET are shown in Fig. 10.

The bias voltages span in the range from 0 to 1 V for the drain and from 0 to -0.8 V for the gate. The NDR region shifts toward higher drain-bias voltage as gate-bias magnitude decreases. For gate voltage close to 0 V, an increase in the magnitude of the NDR region is also observed. On the other hand, when the gate bias is set to -0.8 V, the characteristic becomes strongly discontinuous and the NDR region vanishes completely. This is due to the increasing value of the HEMTs equivalent channel resistance which, being in series to the HITD, shifts the HITFET

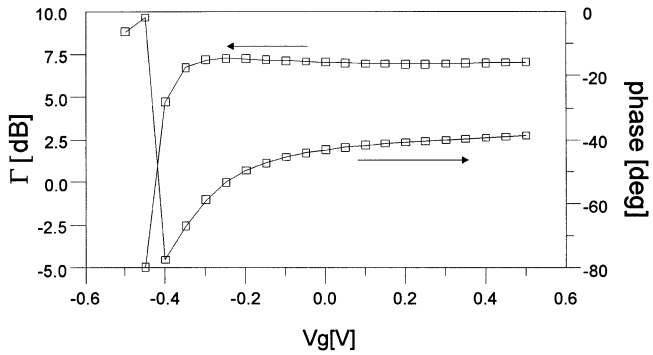


Fig. 11. Drain–HITFETs reflection coefficient (as seen from the source terminal) as a function of the gate control voltages (frequency $= 6.2$ GHz, $Vd = 500$ mV).

peak and valley voltages to higher values. The overall effect is a reduction in the peak-to-valley voltage until the HITFET is no longer functional. The HEMT also introduces a reactive component that modifies the self-resonant frequency slightly. The microwave characteristics (i.e., the dependence of the HITFET in terms of reflection coefficient Γ) seen by the source terminal as a function of different voltage biases are shown in Fig. 11. The measured Γ is higher then zero due to the NDR associated to the diode.

In general, it is possible to tailor the size of the HITD or, equivalently, increase the peak current in order to reduce the NDR in absolute value. This action should produce a higher value of Γ at the expense of an increased parasitic junction capacitor and a reduction of the cutoff frequency. A proper selection of the NDR is advisable to meet the requirement of high-frequency operation and a Γ value that ensures a proper magnitude margin in the oscillation condition.

The main contribution to the phase swing of Γ is due to the variation of the drain–source to channel capacitances, which are an order of magnitude higher than the HITD junction capacitor.

One of the main tasks in the design of HITFET-based circuits is the analysis of the HITFET short-circuit stability. A basic tool for such a study is a small-signal linear model of the HITFET. The model has been derived under the assumption that the HFET within the HITFET is biased at a drain–source voltage of a few tens of millivolts. This makes the transconductance negligible with respect to the HFET output conductance. The equivalent circuit is shown in Fig. 12. The active region of the diode is represented as a negative resistance $-R_d$ in parallel with a capacitance C_d. The drain-to-gate capacitance and the source-to-gate capacitance of the HEMT are neglected and, therefore, the drain-to-source impedance of the FET is the parallel connection of the channel resistance $R_{\rm ds}$ and the channel capacitance $C_{\rm ds}$. The parasitic effects are taken into account by adding a series resistance R_s and a series inductance L_s (Fig. 12).

A device is short-circuit stable if no current can flow in the circuit when no input voltage is applied. It is clear that, if the HITFET is short-circuit unstable, it can oscillate when the bias network (represented by an ideal or real voltage source) is connected to the drain. The stability may be evaluated applying the method described in [23]–[25] to the impedance $Z(s)$ of the low-frequency equivalent circuit shown in Fig. 12. $Z(s)$

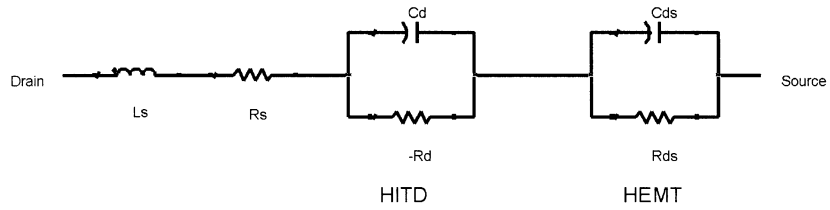


Fig. 12. HITFET equivalent circuit.

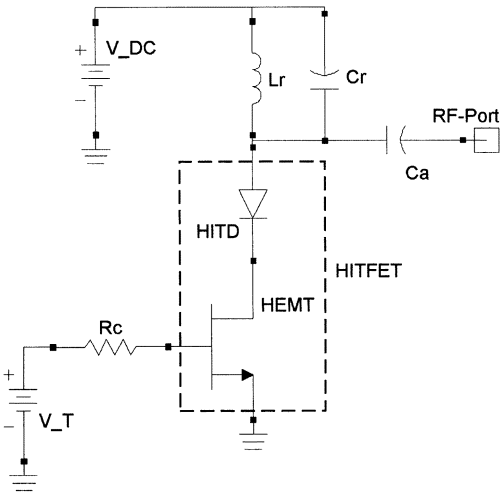


Fig. 13. HITFET-based VCO circuit schematic.

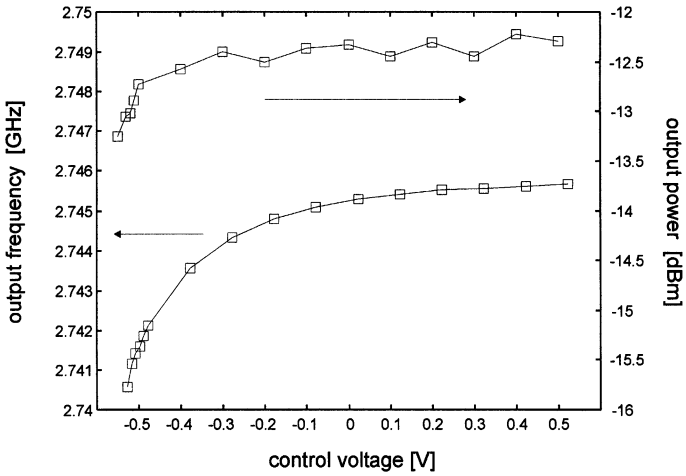


Fig. 14. VCO's output frequency and power as a function of the tuning voltage.

must have no zeros in the right-hand-side half of the S plane as follows:

$$Z(s) = (sL_s + R_s) + \left(\frac{1}{-R_d} + sC_d\right)^{-1} + \left(\frac{1}{R_{\rm ds}} + sC_{\rm ds}\right)^{-1}. \tag{7}$$

This method is also useful to investigate the effects of a variation in the parameters of the equivalent circuit due to a modification of the physical structure of the device or, equivalently, due to the connection of an external lumped element (see the Appendix).

B. QVCO Prototypes and Experimental Results

The experimental results for a voltage-controlled oscillator (VCO) based on the consideration described in the Appendix will be illustrated below. The operation frequency is in the 2.7-GHz band. The topology of the prototype is represented in Fig. 13. It is composed of the HITFET in a common source configuration and a simple off-chip *LC* resonator (Lr, Cr) to achieve the selected frequency. The circuit is controlled by an external tuning voltage V_T. The design method adopted here is the one commonly used in reflection oscillators: the HITFET is considered as the negative resistance element, which must resonate with a proper load to obtain the oscillation. The chip is biased at 500 mV thorough the HITD's anode while the tuning potential is applied to the HEMT's gate through a 1-kΩ resistor.

The tuning characteristic of a free-running VCO for a wide range of tuning voltages is reported in Fig. 14. A frequency swing in the 2.741–2.745-GHz range with a nearly constant power level has been observed. The graph shows a range from -0.5 to -0.1 V in which the frequency changes quickly, which is due to the parabolic shape in the reflection-coefficient phase associated with an almost constant value of the magnitude. For a higher level of tuning voltage, the reflection coefficient has a linear behavior in magnitude and phase.

The power level is approximately -12 dBm, which leads to an efficiency of around 9%. Roughly constant value of the output power is a direct consequence of the IV characteristic of the HITFET. Since the diode bias point is approximately constant during the tuning, the voltage and current dynamics are determined by the IV shape, which governs the saturation mechanism. The power level of the VCO is constant since the reflection coefficient is positive and the oscillation condition is satisfied.

The phase-noise performance of the oscillator has been estimated by use of a spectrum analyzer (see Fig. 15). At 100-kHz offset frequency, a single-sideband noise-to-carrier ratio (SSCR) of -104 dBc/Hz has been obtained. The current drawn by the circuit for a tuning voltage ranging from -0.5 to 0.5 V was between 1.7–1.85 mA. The dc power consumption was approximately 850 μW. This value, to the best of our knowledge, is the lowest dc power consumption for a MMIC VCO operating in this frequency range. This feature enables applications in the area of RF-ID tag for identification or distributed remote sensor networks, where the low-power consumption and the low data rate are common required features. Moreover, the extremely low-power supply makes this technology interesting for batteryless solar-cell-powered equipments.

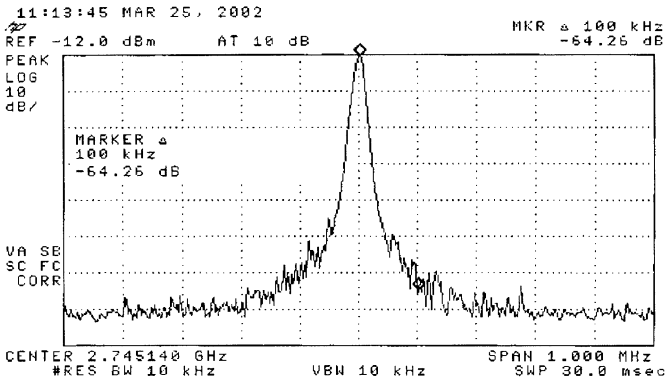


Fig. 15. Output spectrum of the VCO.

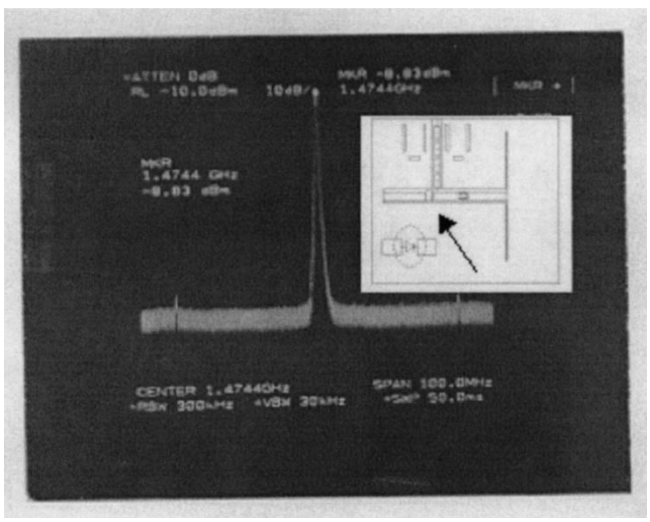


Fig. 16. Frequency spectrum of an active antenna using a $5 \times 5\ \mu m^2$ diode. Bias voltage is 0.37 V and current 2.11 mA. The antenna oscillates at 1.4744 GHz with a power output of -8.83 dBm giving 16.7% dc to RF conversion efficiency.

C. Active Antennas

Active antennas represent an important application of TDs as signal sources. The intrinsic property of TDs to exhibit NDR and RF negative resistance when biased appropriately could be used to improve the performance of such an antenna. TDs have higher operating frequencies and better noise performance compared to Gunn and IMPATT diodes. In addition, tunnels diodes can be operated with very low power consumption. These features make these devices very attractive for active antenna application (see Fig. 16). In particular, HITDs simplify the implementation of such antenna for low-power output applications such as collision-avoiding radar or wireless tag. The principle of operation of this category of antennas is directly related with the inherently oscillating behavior of the TD due to the RF NDR. The RF NDR is employed for signal generation using the antenna like an element of the resonant circuit. A detailed discussion of applications of TDs in active antennas can be found in [26].

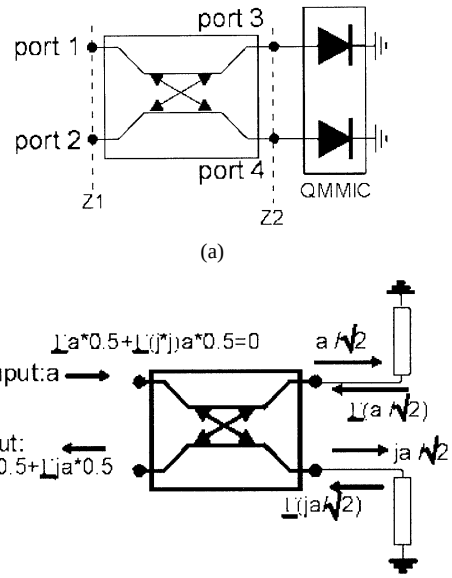


Fig. 17. BDA topology. (a) Simplified schematic. (b) Basic operation principles.

IV. Bidirectional Amplifier (BDA) for RF-Tagging System

A. Circuit Topology and Features

The first proposal for an amplifier, possibly unilateral, based on an NDR device was made by Van der Ziel [27] at the beginning of the 1980's and was mainly oriented to low noise applications. At that time, the unavailability of suitable devices in an integrated circuit (IC) process prevented the exploitation of this proposal in a MMIC. Only in the late 1990s, thanks to the availability of such a device, was it possible to develop this basic idea. In particular, Ando and Cappy [28], making use of three-terminal NDR compound devices, developed this concept to a useful topology configuration by integrating RTDs with FETs.

This section is dedicated to the implementation technique of an innovative amplifier topology called a BDA and its possible application in a tagging system. MMIC circuits based on this topology have been built and the principle of operation has been demonstrated [11]. It makes use of a lumped-element directional coupler with arbitrary impedance terminations, as shown in Fig. 17.

The use of the TDs in the BDA differs from previously proposed amplifiers that also use TDs. It should be noted that the BDA combines the negative resistance characteristics exhibited by an HITD biased in the NDR region, with a directional coupler, in order to obtain a symmetrical and reciprocal system. The two main features of the BDA are symmetry and reciprocity of the associated scattering matrix and gain at extremely low dc power consumption. These features make the BDA an enabling electronic function for an RF-ID tag.

The principle of operation is sketched in Fig. 17(a) and (b), where the HITDs are represented by their equivalent impedance with a negative real part. Defining Z_2 as the directional-coupler

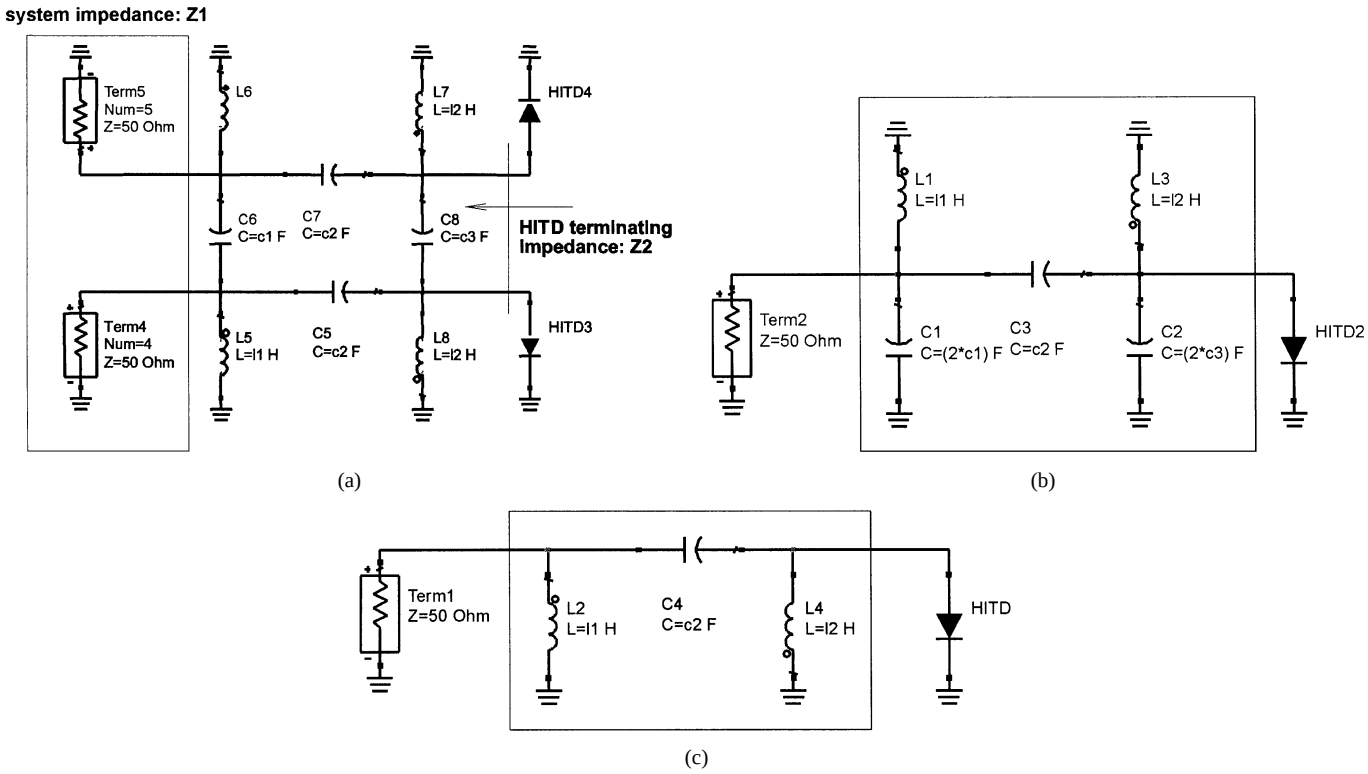


Fig. 18. (a) BDA schematics. (b) Odd-mode equivalent circuit. (c) Even-mode equivalent circuit.

impedance seen by the HITD and R_D as the diode negative dynamic resistance, a simple calculation shows that the BDA gain is

$$\text{gain} = \Gamma e^{j(\pi/2)} \tag{8}$$

where Γ is the reflection coefficient seen by the diode toward the directional coupler.

Equation (8) shows that the amplifier gain depends on the matching between the system impedance and the diode negative resistance R_D. The value can be selected by adjusting either the diode characteristic or the directional coupler characteristic [30]. This allows designers to use the characteristics impedance as a design parameter. A main issue regarding the BDA is its stability. Any negative-resistance-based circuit may present unwanted oscillations [13], [24]. Due to the fact that not all values of gain may be implemented in a stable operation mode, the design method has to take into account the study of the circuit stability.

The circuit analysis theory shows that any stable network must have an equivalent-circuit admittance with no zeros in the right-hand-side half of the complex plane $s = \alpha + j\omega$. The problem of evaluation of the BDA's stability then reduces to determining the roots of the associated input admittance, following the well-known Nyquist's criterion [13]. This criterion relates the number of times the locus of the input impedance of a network encircles the origin to the number of poles (P) minus the number of zero (N) with $\alpha > 0$. To this end, it is necessary to verify the stability of the network for the designed $Z2$ and, consequently, gain. Analysis can be done on the base of a complete lumped-element directional coupler circuit [see Fig. 18(a)] whose design formulas are reported in [30]. To investigate the stability of this circuit, the even- and odd-mode analysis approach for a symmetrical network and associated equivalent circuits can be followed. Fig. 18(b) and (c) shows the circuits for the odd- and even-mode excitation, respectively.

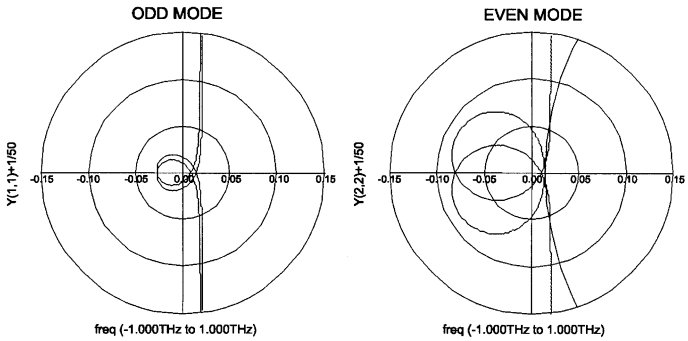
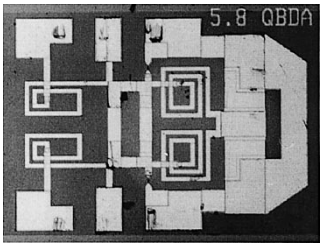
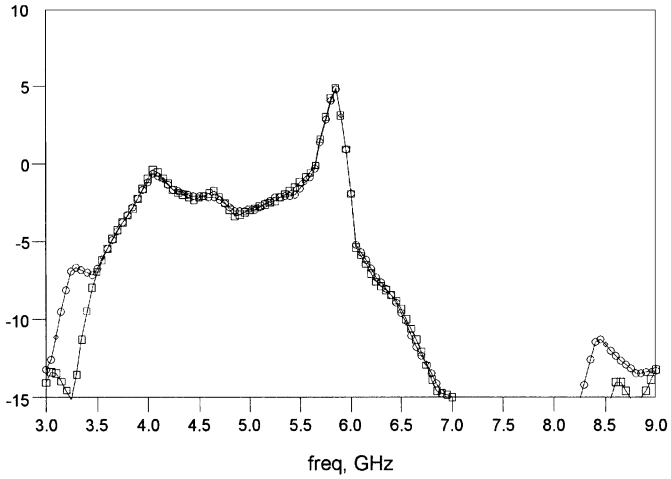


Fig. 19. Polar plots for the odd- and even-mode circuits. The number of counterclockwise encirclement gives the stability condition of the circuit.

The design proceeds by analyzing the input impedance for both even and odd circuits, and selecting the value of $Z2$, which ensure gain and stability. The results of such an analysis for $Z1 = 50\,\Omega$ and $Z2 = 90\,\Omega$ are reported in Fig. 19. In this case, the theoretical small-signal analysis shows a gain of 6 dB at the center frequency of 5.8 GHz. The number of encirclements is two for both the modes, and it may be shown that this is a condition for which $N = 0$, where N is the number of zeros with a positive real part. Thus, this analysis shows that the BDA is stable. The prototype is realized in coplanar technology [see Fig. 20(a)]. The entire design has been carried out using the Momentum tool within the Agilent ADS package. This approach allows careful design of the dimensions of any element, and en-



(a)



(b)

Fig. 20. (a) BDA circuit. (b) Measured $S12$ (circles) and $S21$ (squares) of the BDA.

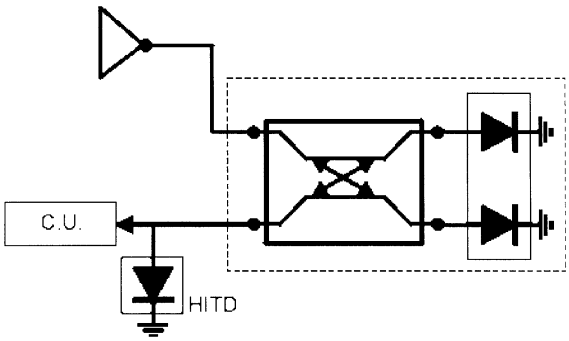


Fig. 21. Schematic representation of the RF ID based on the BDA.

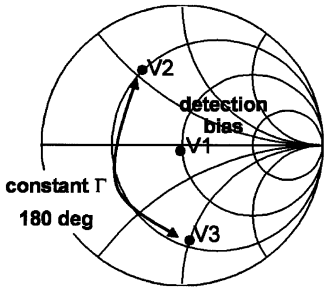


Fig. 22. Reflection coefficients exhibited by the TD in different bias voltages.

ables the consideration of any electromagnetic (EM) coupling between different parts of the circuit, giving a further compact arrangement [30], [31].

The measurement of both $S12$ and $S21$ are also reported in Fig. 20(b). The measurement shows a gain approaching 5 dB, which is slightly lower than the target value due to the loss in the passive part, which were underestimated during the design stage. However, the good bandpass behavior and the reciprocity demonstrate the validity of the approach. The amplifier is biased at 400 mV and drain 1 mA of dc current.

B. RF-ID Application

As highlighted above, the BDA is an enabling electronic function for the RF-ID tag. The proposed tagging system is a particular kind of short-range microwave link (SRML), arranged on the basis of a picocell on the order of a few square meters. Each cell is equipped with an RF antenna, usually mounted in the center of the cell in a convenient location, which allows interference and obstacle fading strength. Each antenna is connected to a "reader," which controls the communications between the tag mounted on the host and the antenna in the middle of the cell. This equipment is usually referred to as a transceiver (TX–RX). The reader sends out a signal (via the antenna) to the tag, which lets the tag know that it should begin communication. The tag returns a unique ID number, which is used to identify the host. In the case of read/write tags or smart tags, additional information may be transmitted by the tag (e.g., any ambient-related information) and the reader may send back updated information to be encoded on the tag/smart card.

The proposed solution considers the reflective scheme (Fig. 21) composed of a RX–TX patch antenna, the BDA and a high sensitivity detector, and a control unit. It is possible to identify the two operation modes. In the receiving mode, the circuit acts as a direct conversion receiver. In this mode, the incoming signal is first filtered to proper bandwidth using a bandpass filter network (not shown) to reduce the interference and then amplified by the BDA.

The BDA works in the transmit direction as antenna detector and its gain can be adjusted to the desired coverage range. The detector may be implemented by a TD thanks to its inherent low-level sensitivity, low $1/f$ noise, and the low impedance (typically 10–100 Ω) at zero bias ($V1$ in Fig. 22). The control unit verifies the detected baseband signal and, upon positive identification, the circuit switches to its second state, the backscattering mode. In the receiving mode, the absorbed dc power is almost all due to the BDA (if the power consumption of the control unit is neglected). At typical power consumption of 0.1 mW for a 6-dB gain circuit, the tag can provide one year of continuous operation if the system is powered by a 1-Ah battery. A channel study, carried out for an indoor communication system using the above-mentioned data, predicted a diode sensitivity of -52 dBm for a 7-m range of coverage at 5.8 GHz.

In the backscattered mode, the BDA is terminated at the antenna at one port and to the TD at the other port. The circuit schematic is the same as that in Fig. 21. In this mode, the diode is driven by a two-state signal $V2$ and $V3$ in Fig. 21. In these two states, the diode assumes different impedance values so that the reflection-coefficient amplitude is constant and the phase difference swing is 180°. This allows a variable backscattered gain independent of the diode states and a superimposed phase modulation on the transmitted signal [11].

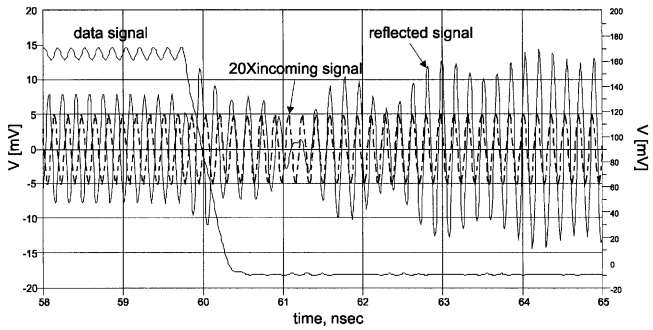


Fig. 23. Simulated data signal (right-hand-side axis), incoming signal (left-hand-side axis) and reflected signal (left-hand-side axis) for an RF-ID tag data link in the backscattered mode.

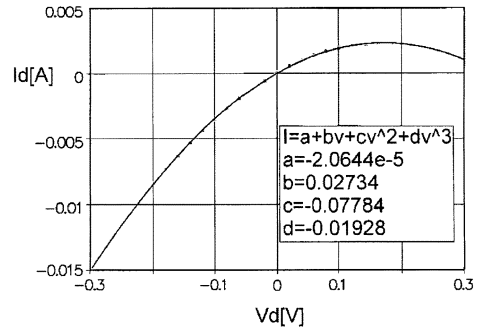


Fig. 24. Approximation by a third-degree polynomial of the intrinsic diode I/V characteristic around zero bias. The fitting standard error is $3.18e-5$. Symbols: data; continuous curve: fitting.

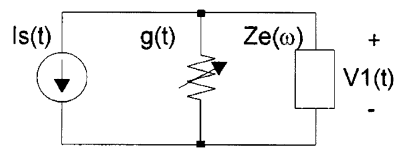


Fig. 25. Time-varying nonlinear equivalent mixer circuit.

Fig. 23 reports the simulated time-domain representation of the proposed RF-ID tag's meaningful signals, in the backscattering mode, for an operation at 5.8 GHz and for a data rate of 100 MHz. The data signal consists of the voltage applied to the HITD in order to obtain different load conditions and, in turn, different phase reflection. The incoming signal is the one received by the antenna connected to a port of the BDA and acts as the carrier for the data link. The reflected signal is the voltage waveform scattered by the same antenna. This is amplified twice by the BDA; moreover, an almost 180° phase shift is applied depending on the state of the terminating diode. For the sake of comparison, in Fig. 22, the incoming signal is magnified 20 times in order to reach a level comparable with the reflected signal. In the "high" state, the two waveforms are almost in-phase, while in the "low" state, they are 180° out-of-phase, resulting in an elementary binary phase-shift keying (BPSK) modulation. The reflected signal envelope is constant after a transient of 3-4 ns, which is in compliance with most applications in the range of 100 Mb/s.

V. Frequency Converter

A. HITD-Based Mixer

Frequency conversion is another electronic function that takes advantage of HITD technology. Some interesting applications of the HITDs in the field of frequency conversion are subharmonic mixers [32] and frequency multipliers [9]. In this section, the main focus is on the linearity of the mixer implemented using TDs and other important application such as envelope detectors for microwave imaging and atmospheric radiometry. In particular, the HITD can be considered as an enabling device for these electronic function due to the quasi-square-law behavior of the IV characteristic around $V = 0$ V.

It is well known that mixing circuits base their functionality on the nonlinear behavior of the devices. It is also well known that a nonlinearity of the nth degree generates nth-order mixing products. As a consequence, electron devices showing nonlinearity of the nth degree generate nth-order mixing products [33]. This relationship between the order of the nonlinearity and order of the mixing products is an important factor in the mixer design. In particular, the use of devices having approximately second-degree nonlinearity allow inherently good performances in terms of third-order intermodulation (IM3).

The linear behavior of a mixer can be well explained by describing the conversion mechanism of an HITD-based mixer and using the large-signal–small-signal analysis together with the conversion matrices. The basic assumption is the following: the HITD is driven by the local oscillator (LO) signal without involving the negative dynamic region. The intrinsic IV characteristic of the HITD is calculated using a procedure based on the assumption that diodes having different cross sections should have the same peak voltage Vp.

The intrinsic IV characteristic around zero, obtained from the measured extrinsic device data after the extraction of the series parasitic resistance Rs, is approximated through a minimum square-curve-fitting procedure using a polynomial equation up to the third degree in a symmetric range with respect to $V = 0$ V (see Fig. 24) as follows:

$$I(V) = a + bV + cV^2 + dV^3. \tag{9}$$

The fitting shows a factor 4 difference between the second- and third-order coefficients, as expected for a quasi-square-law IV.

A further assumption is that the nonlinear capacitance variation of the HITD with respect to input voltage can be neglected based on the experimental observation that the main contribution is related to the geometrical capacitance [34], [35]. The mixing operation is analyzed by using the equivalent circuit shown in Fig. 25, where the impedance $Ze\ (\omega)$ represents the embedding network and includes the series parasitic resistor Rs. The equivalent two-tone excitation and the LO signal Is and V_{LO}, respectively, are given as

$$\begin{aligned} I_S\,(t) &= I_S\left[\sin\left(\omega_P + \omega_1\right)t + \sin\left(\omega_P + \omega_2\right)t\right] \\ V_{\mathrm{LO}}\,(t) &= V_P \cos\left(\omega_P t\right). \end{aligned} \tag{10}$$

The qualitative description of the power of the IM3 component and the conversion loss requires the calculation of the conversion matrix Yj [33]

$$\mathbf{Y}_J = \begin{vmatrix} b + \frac{3}{2}\,dV_P^2 & cV_P & \frac{3}{4}\,dV_P^2 \\ cV_P & b + \frac{3}{2}\,dV_P^2 & cV_P \\ \frac{3}{4}\,dV_P^2 & cV_P & b + \frac{3}{2}\,dV_P^2 \end{vmatrix}. \tag{11}$$

The calculation of the IM3 component requires the evaluation of the third- and second-order components of the current source generator $\mathbf{I}_S$. Once these current components are determined, the linear conversion matrix analysis can be used to find the voltage across and the current in the embedding impedance at the IM3 frequency. The third-order current in $Ze\,(\omega)$ is

$$\mathbf{I}_{E,3} = -\left[\mathbf{1} + \mathbf{Y}_j \mathbf{Z}_{E,3}\right]^{-1} \mathbf{I}_{S,3} \tag{12}$$

where $Z_{E,3}$ is the diagonal matrix of the embedding impedance at the third-order mixing frequency. The power dissipated in the embedding impedance at the IM3 component is

$$P_{-1,3} = 0.5\,|I_{E;-1,3}|^2\,\mathrm{Re}\left\{Z_{E;-1,3}\right\}. \tag{13}$$

The power content at IM3 depends upon the I/V characteristics of the diode. In other words, a low degree of nonlinearity results in a small conversion matrix. Hence, there are few contributions to the dissipated power in the embedding impedance that is directly dominated by the third-order nonlinearity. A minimization of this parameter is possible, in principle, by adjusting the V_{PEAK}, I_{PEAK} pair through semiconductor bandgap engineering during the HITD development. It is also possible to observe that a reduction of the embedding impedance is required to minimize the IM3 component. IM3 also depends on the embedding impedance.

In the particular case of an HITD-based single balanced mixer, the ports of the quadrature directional coupler, which are connected to the diodes; could be designed for a selected system impedance (not necessarily equal to 50 Ω) able to reduce the intermodulation (IM) product. The same consideration allows an estimation of the transducer conversion loss (G_C) for the HITD-based mixer. From the conversion matrix (11) it is possible to obtain

$$G_C = \frac{1}{4\left|Y_{j_{1,0}}\right|^2 \mathrm{Re}\left\{Z_E\left(\omega_{\mathrm{RF}}\right)\right\} \mathrm{Re}\left\{Z_E\left(\omega_{\mathrm{IF}}\right)\right\}}. \tag{14}$$

G_C only depends on the second-degree nonlinearity and increases as $Ze\,(\omega)$ reduces. A tradeoff between IM3 and G_C is required.

A lumped-element directional coupler (LEDC) implemented using discrete inductors and capacitors is the preferred configuration for RF frequency applications [30], [36]. As a consequence, the LEDC circuit is designed considering that the characteristic impedance for two out of the four LEDC ports has a value that arises from the tradeoff between the IM3 level, conversion loss, and RF/LO isolation. In particular, the diode's impedance at the bias point depends on the parasitic resistance, reactive component, and characteristic around zero. The RF and LO ports maintain the 50-Ω characteristic impedance of the system.

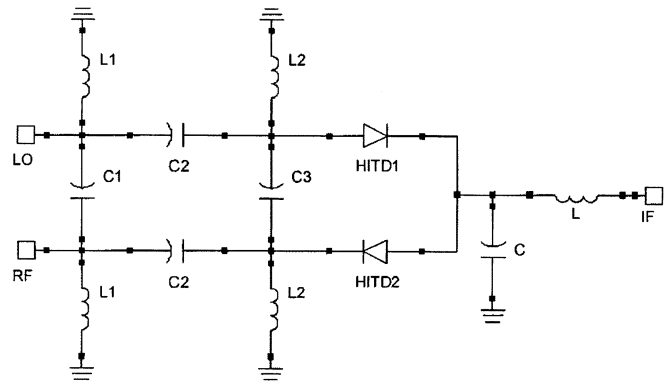


Fig. 26. Single balanced mixer circuit topology.

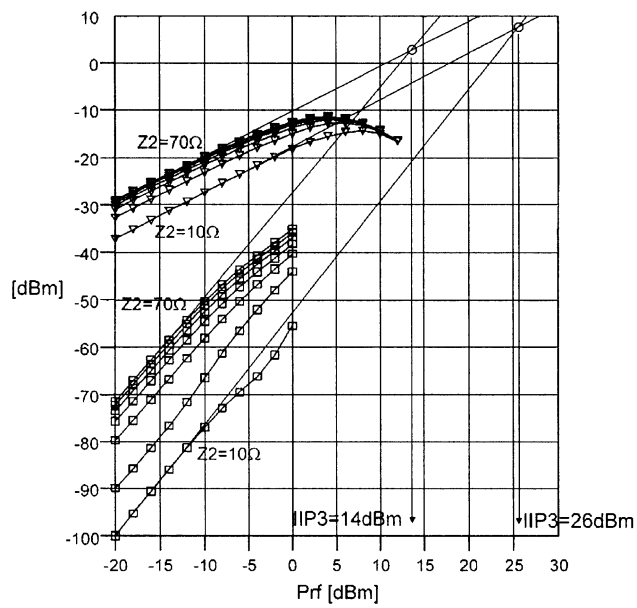


Fig. 27. HITD-based balanced mixer output power. IM3 (square) and IF (triangle) for $\mathrm{LO} = 1.8$ GHz, $\mathrm{RF1} = 1.825$ GHz, $\mathrm{RF2} = 1.835$ GHz, $\mathrm{IF} = 25$ MHz, $\mathrm{IM3} = 15$ MHz, $P = 5$ dBm, as a function of $Z2$, ranging from 10 to 70, step 10.

The LEDC design follows the formulas introduced in [30]. Let Z_1 be the characteristic impedances at the RF and LO ports and Z_2 be the characteristic impedance at the diode ports. The matching problems between the LEDC and nonlinear elements are solved considering a value of Z_2 close to the real part of the impedance of the diode biased at $V = 0$ V. The inductor $L2$ in the LEDC absorbs the residual capacitive part of the diode's impedance. As highlighted in the above discussions, the terminating impedance Z_2 significantly affects the mixer performance.

The nonlinear analysis of the single balanced mixer shown in Fig. 26, with Z_2 as simulation parameter, has been carried out in order to show the effects of Z_2 on performance. The HITD balanced mixer was simulated using the dc/RF diode model discussed in Section II. The simulations (Fig. 27) confirm the theoretical behavior, showing a significant reduction of the IM3 level with reduction of Z_2. A weaker reduction is observed for G_C. Moreover, the simulations highlight the dependence

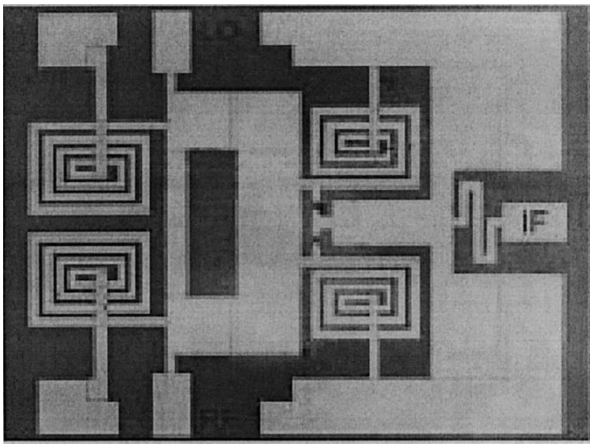


Fig. 28. Prototype chip photograph of the single balanced mixer prototype implemented by LEDC and HITD.

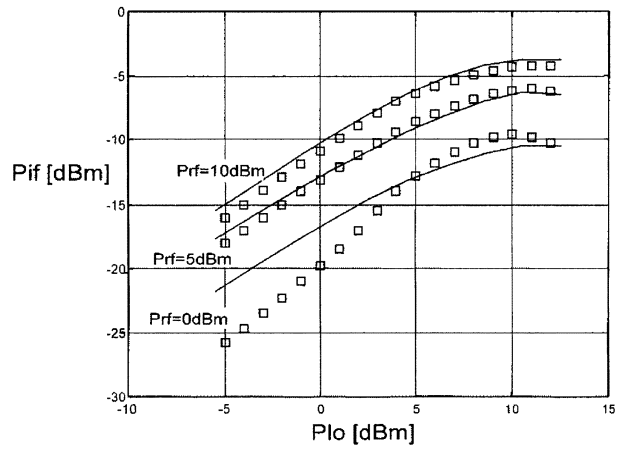


Fig. 29. IF power as a function of LO power at different RF power levels. Squares: measured data, continuous curves: simulations.

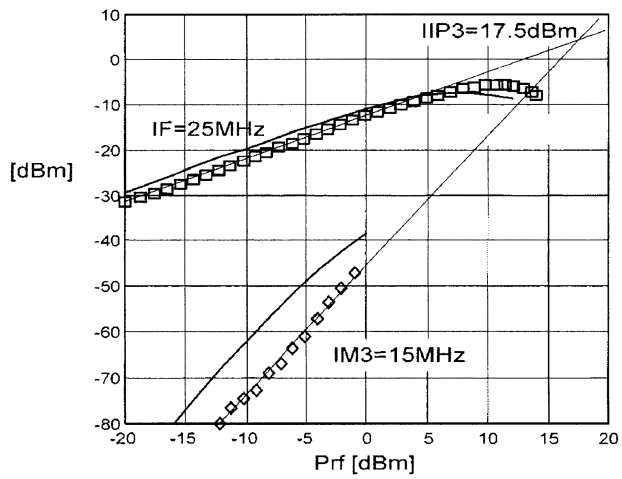


Fig. 30. IF and IM3 output power for $\mathrm{RF1} = 1.825$ GHz, $\mathrm{RF2} = 1.835$ GHz, $\mathrm{LO} = 1.8$ GHz, 5 dBm. The calculated IIP3 is 17.5 dBm. Squares: measured data, continuous curves: simulations.

of the conversion loss on the diode peak current. For different LO levels and at a fixed Z_2, the curves exhibit maximums, which move slightly toward higher current values, as the peak current increases. An increase in the peak current corresponds to a proportional increase of the second-degree nonlinearity. This results in a reduction of the conversion loss [32]. A further increase results in a mismatch between the LEDC and HITD pair, which leads to the reduction of the LO and RF power dissipated in the diode.

This explains qualitatively the origin of an optimum value of the peak current for a given LO level. The unavoidable loss in the LEDC circuit increases the conversion loss, while the reduction of the diodes' series parasitics contributes significantly to a conversion-loss reduction. In the prototypes design, the values of the LEDC circuit element have been calculated using $Z1 = 50$ and $Z2 = 35$. The diodes used in the circuit realization have shown very high current densities (50–60 kA/cm) and peak–valley ratios between 10–15. The selected peak current is 1.8 mA and the LO level is 5 dBm. The entire design, which makes use of the coplanar technology, has been carried out using the Momentum tool available within the Agilent ADS package.

This approach allows careful design of the dimensions of any element, and enables the consideration of any EM coupling between different parts of the circuit, making further compact arrangement possible (Fig. 28). A close investigation of the mixer operation illustrates that the optimization of the linearity performance by adjusting Z_2 may lead to a mismatch between the LEDC and HITD pair. This results in a signal reflection that reaches the input ports, reducing the LO to RF isolation. This can be improved by implementing a 180° coupler. The large-signal performance of the prototype has been tested using an LO frequency of 1.8 GHz and an RF frequency of 1.83 GHz with different levels of LO and RF power. Fig. 29 shows the mixer performance in terms of IF output power with respect to the LO level depending upon different RF power. A value of 5 dBm is an acceptable tradeoff between the IF power, linearity, and LO level. The comparison with simulation shows a fairly good match between curves for $P_{\mathrm{RF}} = 5$ and 10 dBm, while the accuracy of the simulation reduces for 0 dBm, particularly for a low LO level.

The set of harmonic-balance simulations uses the small-signal EM simulation for the LEDC description in conjunction with the HITD nonlinear model. The linear response, which is the main characteristic of the proposed mixer, results in a high value for both the 1-dB compression point and input third-order intermodulation product (IIP3) parameters. Fig. 30 reports the IF level as a function of the RF power for a 5-dBm LO. The 1-dB input power compression point of the mixer was 7 dBm.

The IIP3 has been evaluated using two RF signals at 1.825 and 1.835 GHz, respectively, and results in 17.5 dBm under the LO level of 5 dBm (Fig. 30). This is a value typically obtained in double balanced diode mixers. The same graph also reports the simulated data; which show an evaluation of the IIP3 less than the actual value. This lack of accuracy could be an effect of the inaccurate description of the odd-order nonlinearity due to the differences in the HITD prototypes and to a series resistance underestimation.

In Fig. 31, second-order spurious rejection behavior of the mixer for $2\mathrm{RF} + 2\mathrm{LO}$ with $\mathrm{RF} = 1.83$ GHz and $\mathrm{LO} = 1.8$ GHz is reported as a function of the LO power for different RF levels. They appear to be more than 20 dB below the IF output level,

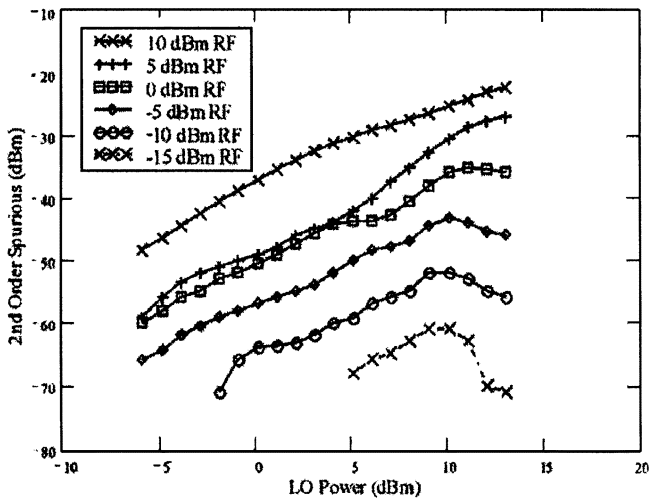


Fig. 31. Spurious response $(2;2)$ as a function of LO power at different RF power levels. $\mathrm{RF} = 1.83$ GHz, $\mathrm{LO} = 1.8$ GHz.

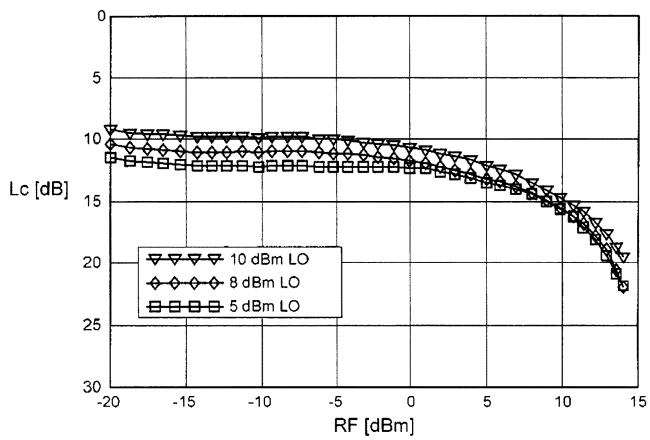


Fig. 32. Conversion loss as a function of the RF power at different LO power levels. $\mathrm{RF} = 1.83$ GHz, $\mathrm{LO} = 1.8$ GHz.

at the same conditions for the LO and RF input powers, particularly in the case of the 5-dBm LO and 15-dBm RF; this spurious contribution is 40 dB lower than the respective IF level. Finally, the mixer conversion loss, shown in Fig. 32, is around 11 dB in the linear range. This performance, which is slightly higher than the conversion loss of typical Schottky diode mixers, constitutes the main drawback of the proposed mixer and is due to the low degree of nonlinearity presented by the HITDs.

B. HITD-Based Mixer Envelope Detector

Another important applications of the HITDs in the field of the frequency conversion are the passive envelope detector for atmospheric radiometry and millimeter-wave imaging illustrated in [38].

At the beginning of this section, HITDs have been referred to as enabling devices for such a system. Desired objectives like low power consumption, high sensitivity, low noise performance, low circuit complexity, high bandwidth, large dynamic range, and highly linear conversion from power to dc have been reached thanks to the features of the HITDs. In particular, the envelope detectors are based on the quasi-square law showed by the heterostructure single barrier tunneling (not resonant) diode

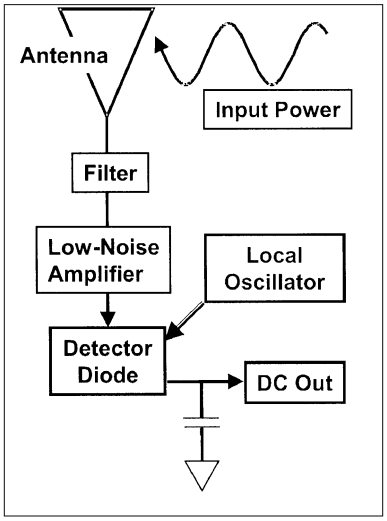


Fig. 33. Schematic block diagram of a simple radiometer system.

in the power-to-dc-voltage conversion that is directly related to the behavior of the HITD's IV characteristic around $V = 0$ V. In general, a passive envelope detector can also be implemented using nontunneling diodes (e.g., a low-voltage Schottky diode). In this case, the performance of the system decreases, while the complexity of the circuits increases. The block diagram in Fig. 33 illustrates the simple architecture of such detectors implemented using the HITD. The RF power is collected by an antenna, filtered by a narrow- or wide-band filter, amplified by a low-noise amplifier (LNA), and mixed with an LO in order to obtain the requested dc output.

VI. Conclusions

The development of TD-based devices for microwave applications is fueled by the need for higher performance devices that can enable new circuit functionalities. The QMMIC is not conceived as a competing technology with respect to capable and well-established GaAs HBTs and FETs, but a complementary technology able to increase their performance. The possibility to implement all the functions that are normally required in a microwave transceiver using only HITDs is not envisioned. In this paper, the methodology for the analysis and design of a number of building blocks like the frequency converter and free-running oscillators has been described. These circuits have features that make them unique. The presented single balanced mixer provides high linearity by using zero-bias TD devices. This is of great importance in order to reduce the flicker noise and the IM in low-IF system receivers. To the best of the authors' knowledge, the VCOs reported in this paper have the lowest reported power supply and fairly good phase noise. This solution allows their integration in all systems where the static energy is provided to the system using unconventional ways such as a rect-antenna or solar cell. The efficiency and overall features are also very attractive for low-power portable systems.

Some challenges and limitation still face the research groups working in this area. First of all, it may not be possible to implement all the standard building blocks involved in a transceiver using QMMIC technology. For example LNAs, power amplifiers (PAs), and switches are hard to replace.

However, it is important to note that QMMIC technology can be used in conjunction with conventional MMIC building blocks. With the addition of a single epi stack and one mask level, the wafer fabrication process for both QMMIC and MMIC circuits can be simultaneously realized. It is possible to monolithically integrate QMMIC and MMIC circuits on the same wafer. Therefore, from an RF design point-of-view, a choice between QMMIC and MMIC technology does not have to be made. Designers can choose the technology (MMIC or QMMIC) best suited for a given building block and seamlessly integrate it with other circuit blocks to realize highly integrated ICs.

The QMMIC building blocks can be used either for improving the cost/effectiveness of conventional architectures, following the so-called optimization approach, or for realizing alternative and more effective architectures. This opens the door to a completely new approach: the "enabling technology approach." This approach improves the effectiveness of the systems taking advantage of the unique features of QMMIC technology, by introducing appropriate architectures whose application is enabled by the features of that technology. An example of this is given in Section III; where a completely new ultra-low power RF-ID system architecture is enabled by the use of a BDA. This is a new-concept circuit, which cannot be easily implemented by conventional technology, improves the operative range of RF-ID tags, and allows a drastic reduction of the component's count and, consequently, the cost.

Although a considerable research effort in this area is still required to describe more circuit functionalities, to increase the reliability, and to decrease the fabrication cost, it is believed that the QMMIC is an emerging technology that can be exploited to realize low-power communication products.

APPENDIX

Here, the effects on the short-circuit stability of an HITFET due to the connection of an external lumped element to an HITFET are reported. Starting from the impedance $Z(s)$ of the low-frequency equivalent circuit

$$Z(s) = (sL_s + R_s) + \left(\frac{1}{-R_d} + sC_d\right)^{-1} + \left(\frac{1}{R_{\rm ds}} + sC_{\rm ds}\right)^{-1}. \tag{A1}$$

The following four different cases have to be analyzed.

Case 1) *Inductor L_s in series with the drain or the source.*

If we assume that the following conditions:

$$R_d C_d - R_{\rm ds} C_{\rm ds} > 0 \quad R_d - (R_s + R_{\rm ds}) > 0 \tag{A2}$$

are satisfied, assuming the zeros of (A1) have a positive real part, we obtain that there is a maximum value L_C for the series inductor L_S to ensure the stability.

Case 2) *Resistance R_s in series with the drain or source.*

Let us consider resistor Rs in the circuit. If the first of condition (A2) is satisfied, the circuit is stable as long as the second condition of (A2) is also true. Let Rc be the critical value of Rs that satisfies (A2). In this case, however, the circuit does not oscillate since the solution for the current I is given by growing exponential functions. It can also be demonstrated that, if we include both a series resistance and a series inductor L_s, the circuit is stable for higher values of L_c than those obtained when only the inductance is added. However, when the circuit becomes unstable, the oscillation frequency is not affected by the values of resistance.

Case 3) *Capacitance C in parallel with the HITD.*

If we add a capacitance in parallel with the tunneling diode, we obtain a new equivalent circuit with

$$C_d^* = C_d + C. \tag{A3}$$

If the HITFET itself is stable (i.e., conditions (A2) are verified for $C = 0$)), it can be demonstrated that stability conditions are not changed by the added capacitance C.

Case 4) *Capacitance C in parallel with the HFET.*

In this case, we have

$$C_{\rm ds}^* = C_{\rm ds} + C. \tag{A4}$$

Depending on the value of the circuit parameters, the following three different cases have to be investigated.

Case 1)

$$R_d < \left\{ L_s / \left[C_d \left(R_{\rm ds} + R_s \right) \right] \right\}. \tag{A5}$$

The circuit is nearly always unstable (see [23] for more details).

Case 2)

$$\left\{ L_s / \left[C_d \left(R_{\rm ds} + R_s \right) \right] \right\} < R_d < \left[L_s / \left(C_d R_s \right) \right]. \tag{A6}$$

The circuit is stable if C is not increased beyond a critical value (see [23]).

Case 3)

$$\left[L_s / \left(C_d R_s \right) \left(C_d R_s \right) \right] < R_d. \tag{A7}$$

The circuit is always stable.

ACKNOWLEDGMENT

The authors wish to acknowledge the assistance and the support of the Wafer Fabrication Team, Physical Sciences Research Laboratories, Motorola Laboratories, Tempe, AZ.

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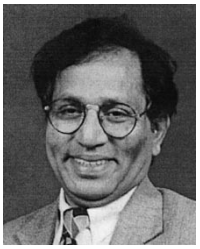

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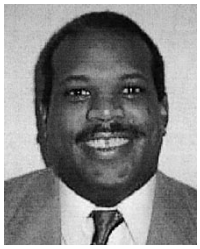

Jonathan H. Lewis (M'99) received the B.S. degree in electrical engineering from North Carolina Agricultural and Technical State University, Greensboro, in 1988, and the Ph.D. degree in electrical engineering from Howard University, Washington, DC, in 1991. His doctoral dissertation concerned molecular-beam epitaxy (MBE) growth of strained superlattice and their electrical transport properties.

He is currently with Motorola Laboratories, Tempe, AZ, where he is involved with epitaxial growth of quantum functional devices (TDs) and their applications to RF millimeter-wave circuits. This work focuses on device fabricated in the III–V material systems and specifically InP.

Matteo Camprini was born in Florence, Italy, in 1973. He received the Laurea degree in electronic engineering from the University of Florence, Florence, Italy, in 2000, and is currently working toward the Ph.D. degree at the University of Florence.

He is currently with the Microelectronics Laboratory, Department of Electronics and Telecommunications, University of Florence. His research activities concern the study and characterization of tunneling effects in quantum NDR devices and the application of such class of devices to the design of QMMIC circuits.

Gianfranco Manes (SM'02) was born in Florence, Italy, on November 16, 1944.

He became an Associate Professor in 1980 and a Full Professor in 1985 with the University of Florence, Florence, Italy. He has contributed, since the early stages, to the field of surface-acoustic-wave (SAW) technology for radar signal processing and electronic-countermeasure applications. His major contributions include the introduction of novel finite-impulse response (FIR) synthesis techniques, fast analog spectrum analysis configurations, and frequency-hopping waveform synthesis. Since the early 1980s, he has been active in the field of microwave modeling and design. In the early 1990s, he founded and is currently leading the Microelectronics Laboratory, University of Florence, where he is committed to research in the field of microwave devices. In 1982, he was committed to starting a facility for the design and production of surface acoustic wave (SAW) and microwave integrated circuit (MIC)/MMIC devices, as a subsidiary of the Florence radar company SMA Spa. In 1984, this facility became the standalone privately owned microwave company Micrel SpA, operating in the field of defence electronics and space communications. From 1996 to 2000, he was involved in IV framework projects, in the field of information technology applied to cultural heritage and was invited to orientation meetings and advisory panels for the Commission. His current research interest is in the field of RITD devices for microwave applications in a scientific collaboration with the Group at the Physical Science Research Laboratories, Motorola Laboratories, Tempe, AZ. He was founder and is currently President of MIDRA, a research consortium between the University of Florence and Motorola. He is Director of the Italian Ph.D. School in Electronics. In November 2000, he was appointed Deputy Rector for the Information System, University of Florence. He has authored over 100 scientific papers in learned society journals and presentations at international conferences.

Dr. Manes is member of the Board of Italian Electronics Society.

Herb Goronkin (M'75–SM'83–F'89) received the B.A., M.A., and Ph.D. degrees in physics from Temple University, Philadelphia, PA.

He is Vice President and Director of the Physical Research Laboratories, Motorola Laboratories, Tempe, AZ. Following research assignments in the areas of compound semiconductors, silicon ICs, optical sensors, and microwave semiconductor devices, he joined Motorola in 1977 to build their GaAs electronics program. His laboratory developed Motorola's early versions of heterostructure transistors and circuits for low-power low-noise wireless applications and high-efficiency power transistors for cellular telephones. More recently, his laboratory developed DNA biochips for analysis of genetic defects and spun the effort into a newly formed division in 1998. The laboratory continues development of microfluidic chips for biological sample preparation and analysis. The Physical Research Laboratories are developing quantum and molecular devices for future logic, wireless, and biosensor applications. The Physical Research Laboratories recently transferred its world leadership MRAM technology to the Semiconductor Products Sector, which continues its development for product introduction. Motorola's MRAM is based on tunnel junction magnetic devices for universal nonvolatile memory (MRAM) applications. Meanwhile, he and his staff continue the investigation of radical scaling of MRAM memory elements, as well as new device applications of spin-dependent structures and materials. The Physical Research Laboratories are rapidly approaching world parity in the area of molecular electronics, which will be used in future ICs, as well as sensing and analysis of biological molecules. He has served on numerous conference committees and professional organizations. He has over 65 patents and numerous publications.

Dr. Goronkin is a member of the American Physical Society and Sigma Xi. He is a member of Motorola's Science Advisory Board Associates. He is a Motorola Dan Noble Fellow. He was the recipient of the 1992 Motorola Distinguished Innovator Award and the 1995 Master Innovator Award. He was selected as Senior Engineer of the Year in 1993 by the Phoenix Section of the IEEE.