Analog+digital phase and frequency detector for phase locking of diode lasers

Analog+digital phase and frequency detector for phase locking of diode lasers

L. Cacciapuoti
ESA Research and Scientific Support Department, ESTEC, Keplerlaan 1-P.O. Box 299, 2200 AG Noordwijk ZH, The Netherlands

M. de Angelis
Istituto di Cibernetica, C.N.R., 80078 Pozzuoli (NA), Italy

M. Fattori,[a] G. Lamporesi, and T. Petelski
Dipartimento di Fisica, Università di Firenze and INFN, Sezione di Firenze, 50019 Sesto Fiorentino (FI), Italy

M. Prevedelli[b]
Dipartimento di Chimica Fisica e Inorganica, Università di Bologna, 40136 Bologna, Italy

J. Stuhler
Physikalisches Institut, Universität Stuttgart, 70550 Stuttgart, Germany

G. M. Tino
Dipartimento di Fisica, Università di Firenze and INFN, Sezione di Firenze, 50019 Sesto Fiorentino (FI), Italy

(Received 19 February 2005; accepted 24 March 2005; published online 2 May 2005)

We describe a type of phase and frequency detector employing both an analog phase detector and a digital phase and frequency detector. The analog and digital detectors are mutually exclusive so that only one of them is active at any given time, resulting in a phase detector with both the broad capture range of digital circuits and the high speed and low noise of analog mixers. The detector has been used for phase locking the diode lasers generating the sequence of Raman pulses in an atom interferometer. The rms phase error of the phase lock is about 100 mrad in a 5 Hz–10 MHz bandwidth. The limit set on the interferometer phase resolution by the residual phase noise is 1.1 mrad. Since the digital circuitry is implemented with a programmable logic device the detector can be easily adapted to other experiments requiring frequency/phase stabilization of lasers sources.
 [DOI: 10.1063/1.1914785]

I. INTRODUCTION

Phase locking of diode lasers is a well established technique both in frequency metrology[1,2] and in cold atoms manipulation.[3]

In the specific field of cold atom interferometry,[4] a technique finding increasing applications both in high precision measurements of fundamental constants[5–7] and construction of high sensitivity inertial sensors,[8–10] a couple of phase–locked diode lasers almost resonant with the $D2$ line are often used to induce Raman transitions between the two hyperfine levels of the ground state of alkali atoms. The interferometric sequence is a combination of $\pi/2$ and π Raman pulses that split and recombine the atomic wave packets.

This application is particularly demanding since it requires not only a robust optical phase-locked-loop (OPLL), permitting continuous operation over long periods of time, but also the lowest possible rms phase error $\sqrt{\langle \varphi^2 \rangle}$, which is one of the factors limiting interferometer sensitivity.

The best performances in terms of robustness and reliability are generally obtained with digital phase and frequency detectors (DPFDs) because of their broad frequency capture range. An occasional electrical or mechanical disturbance abruptly driving away the lasers beat note from the locking point will be recovered even by a feedback loop with relatively small loop bandwidth.

The capture range of the DPFD is limited only by the maximum toggle frequency f_t of its flip flops: single integrated circuits implementing a DPFD are available with f_t up to 200 MHz (i.e., Analog Devices AD9901).[11] It is also not difficult to implement a broad phase range DPFD using standard transistor-transistor logic (TTL) components with f_t up to about 100 MHz.[12]

A DPFD is intrinsically noisier than a standard rf mixer used as an analog phase detector (APD) because the comparator converting the beat note to digital levels tends to have more jitter and to require a higher signal to noise (S/N) ratio since it is more sensitive to amplitude-to-phase noise conversion.

It is difficult to quantify precisely the noise level of a DPFD, due to the strong nonlinear dependence on the input (S/N) ratio. An APD, apart from some $1/f$ excess noise at

[a]Present address: Physikalisches Institut, Universität Stuttgart, 70550 Stuttgart, Germany
[b]Also at INFN, Sezione di Firenze, 50019 Sesto Fiorentino (FI), Italy, electronic mail: mrp@fci.unibo.it

low frequency, often has a noise density limited by the shot noise of the current flowing into the diodes, translating to a phase noise spectral density routinely below 1 μrad/$\sqrt{\text{Hz}}$.[13] The typical propagation delay of fast comparators and digital electronics in a DPFD is a few ns, while the turn on time of the Schottky diodes in an APD can easily reach a few hundred ps.

The capture range of the APD, however, is on the order of the loop bandwidth f_l which is typically 3–5 MHz, limited by the loop delay time and the phase lag in the diode laser frequency modulation response. If the beat note differs from the locking point by more than f_l the APD error signal is averaged to zero by the feedback loop.

Very low $\langle\varphi^2\rangle$ OPLLs are thus generally built around an APD,[13] possibly adding in parallel a DPFD at much lower gain.[14,15] In this type of combined APD+DPFD systems the effect of the DPFD is negligible when the APD keeps the OPLL in lock but it can bring the beat note back within the APD capture range in case of occasional disturbances. This often implies a loss of the phase memory due to the limited phase detection range (usually $\leqslant 4\pi$) of most single chip DPFD.

In this article, attempting to take the best of both the digital and the analog worlds, we present a modification of the APD+DPFD system where, depending on the magnitude of the phase error $\Delta\varphi$, only one of the two detectors is active at any given time. At small $|\Delta\varphi|$ only the APD generates the detector output, while the DPFD detects the occurrence of cycle slips in the APD. In this mode of operation any jitter in the DPFD is irrelevant. The occasional cycle slip increases $|\Delta\varphi|$ above threshold so the APD is immediately disabled and the DPFD generates the phase/frequency error signal until reentering the small $|\Delta\varphi|$ region. If $|\Delta\varphi|$ remains within the dynamic range of the DPFD, switching between the two modes does not cause a loss of phase memory in the DPFD.

With respect to a traditional APD+DPFD, this detector has the advantages of being insensitive to digital noise and having much better chances of quickly recovering from cycle slips without losing phase count. It can then be useful not only for reliable, low noise OPLLs but also for locking to, or counting, beat notes when either the limited available control bandwidth or the poor S/N ratio would make an OPLL that is based only on an APD too unstable. For example, a couple of spectroscopic applications involving the phase locking of a diode laser to an optical comb generator have already been reported.[16,17]

The article is organized as follows: in Secs. II–IV we present the principle of operation of the APD+DPFD and discuss some practical implementations. A detailed description of the circuit developed for our specific application and of the complete OPLL setup are given in Secs. V and VI, respectively. Finally in Sec. VII we present the experimental results and discuss the performances of our system.

II. PRINCIPLE OF OPERATION

The transfer function of an ideal phase and frequency detector (PFD) is shown in Fig. 1(a). For a phase difference $\Delta\varphi$ between the two inputs within a given dynamic range

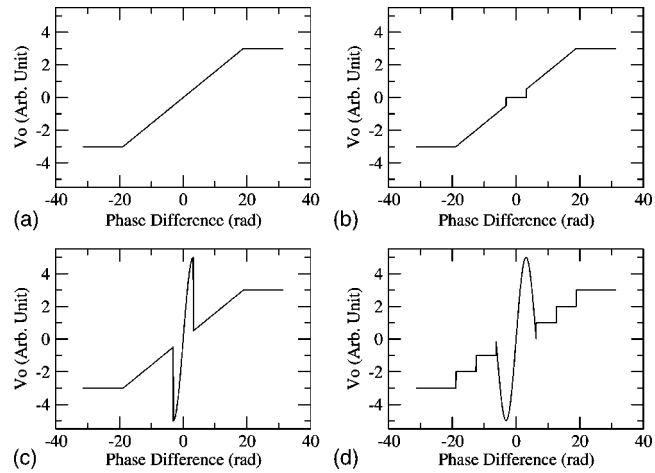

FIG. 1. Transfer functions for four different kinds of phase and frequency detectors. (a) Ideal PFD with a dynamic range of $\pm 6\pi$ and a saturation output of $V_m = \pm 3$ arbitrary units. (b) Same as (a) but with a dead zone of $\pm\pi/2$ centered around 0 phase difference. (c) Ideal APD+DPFD transfer function, assuming an APD/DFPD gain ratio of 5. (d) Approximation of (c) easily implemented with standard logic building blocks. Each step within the dynamic PFD range is 2π wide.

(for example $\pm 6\pi$ in Fig. 1) the output voltage is $V_0 \propto \Delta\varphi$. Outside the dynamic range the detector saturates to $V_0 = \pm V_m$ indicating the sign of the frequency difference of the inputs. Note that a PFD has a monotonic transfer function. So in an OPLL it is not possible to stabilize the slave laser (SL) both at higher and lower frequency with respect to the master laser (ML), as when employing an APD.

If the previous transfer function can be modified as in Fig. 1(b) by adding a "dead zone" of width π centered around $\Delta\varphi = 0$, the output V_D of the PFD can be combined, in the dead zone, with the error signal V_A of a standard APD where the input phases have been arranged so that $V_A \propto \sin(\Delta\varphi)$, obtaining a total output $V_0 = V_A$ if $|\Delta\varphi| \leqslant \pi/2$ and $V_0 = V_D$ otherwise, as shown in Fig. 1(c).

Even if the PFD is implemented with a noisy digital circuit, its output is null when $|\Delta\varphi| < \pi/2$ and only the APD is contributing to V_0. Nevertheless, the PFD can still detect cycle slips in the APD and suppress its output whenever $|\Delta\varphi| > \pi/2$. If the phase jump is within the PFD dynamic range and the servo loop has enough bandwidth, recovering to the $|\Delta\varphi| < \pi/2$ region can take place without loss of phase memory, i.e., saturation of the DPFD.

Two auxiliary output signals can also be generated easily: the first one can be used to read if the PFD is in the dead zone or not, i.e., if the APD is in lock. The second one is a flag signaling if a saturation of the PFD, i.e., a loss of phase memory, has ever occurred since the last flag reset. They can both be used to validate data not only for our specific application but, for example in a frequency chain where a beat note has to be counted for a given time, while making sure that all the OPLLs have been in lock during the measurement. A more rigid phase policy, namely set a flag if an APD cycle slip has ever been detected since the last flag reset, is also easily enforced.

III. DPFD BLOCK DIAGRAM

A DPFD can approximate the ideal PFD using a digital phase counter.[12] The two DPFD inputs which, according to

the standard jargon, will be named radio frequency (rf) and local oscillator (LO), are converted to digital levels by fast comparators. The counter, initially preset at midscale, will be incremented at the rising edges of the rf and decremented at the rising edges of LO. If the output of the counter drives a digital to analog converter (DAC), after a low pass filter, the output signal is proportional to the phase difference between rf and LO. The dynamic range is set by the number of bits in the counter and DAC. Overflow or underflow in the counter are prevented by blocking, with some extra logic, the rf input when in the "all ones" state and the LO when in the "all zeros" state. Note that this DPFD has zero output when rf and LO are in phase while the standard APD requires rf and LO out of phase by $\pm\pi/2$ for zero output.

A practical implementation builds the phase counter using two standard up/down counters and an adder: C_{RF} counts up the rf input while C_{LO} counts down the LO input. The sum of the outputs of C_{RF} and C_{LO} generated by the adder behaves exactly as required even when the counters overflow.

In a real system, the different commutation times of the flip flops in the counters and the carry propagation delay in the adder should also be taken into account. Since they do not have a fixed phase relation when out of lock, it is impossible to decide when to sample, i.e., store in a latch, the adder output, in order to read a stable value. On the other hand, sampling is desirable because it can be used to create a dead zone and because it helps in reducing glitches.

A reasonable choice is to sample the adder output at the falling edge of LO. When in lock, rf will be in phase with LO and so sampling will be halfway between two consecutive transitions of both counters, ensuring that propagation effects in the DPFD will not produce reading errors.

This sampling procedure corresponds to rounding the phase difference to an integer number of cycles so that the output of the DPFD has a staircase shape where each step is 2π wide. By inverting the LO signal, in order to shift the staircase by π and properly adjusting the LO phase to the APD, the total transfer function of this DPFD plus APD has the shape shown in Fig. 1(d). The two differences with the desired shape of Fig. 1(c), namely a staircase shape instead of a single dead zone and a width of 2π instead of π, with the addition of the two unstable points at $\Delta\varphi=\pm\pi$, do not significantly change the APD+DPFD operation.

The saturation logic uses two binary number comparators to check the latch output n against an upper and lower threshold (t_u and t_l, respectively), blocking C_{RF} if $n \geqslant t_u$ or C_{LO} if $n \leqslant t_l$. The output of the two comparators can also signal upper and lower saturation and set the saturation flag. It is not safe to maximize the DPFD dynamic range by letting $t_u=$ ''all ones'' and $t_l=$ ''all zeros'' since occasional rollovers can still take place when the rf and LO frequencies are very different.

A third comparator signalling the $n=z$ condition (where z is the binary code corresponding to zero DAC output) is required to enable the APD output and can be used to detect cycle slips.

Since, when in lock, the adder will oscillate between $n=z$ and $n=z+1$ (or $n=z-1$) if rf leads (or lags) LO, it is better to choose z for the binary number 100 … 001, instead of 100 … 000, to minimize commutation noise in the DAC by avoiding $011\ldots111 \leftrightarrow 100\ldots000$ transitions. This can be done by forcing a reset condition where C_{RF} is preset to z and C_{LO} is preset to "all zeros."

The block diagram of the DPFD is shown in Fig. 2.

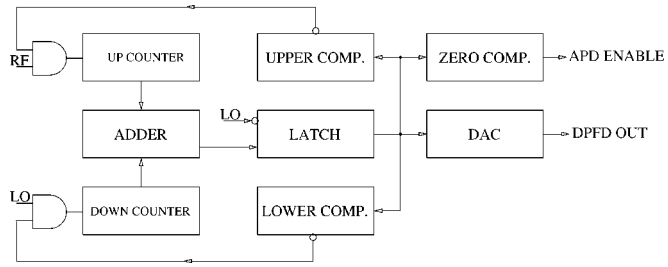

FIG. 2. Simplified block diagram of the DPFD. RF and LO have already been converted to digital signals. The optional cycle slip detection logic has been omitted.

IV. APD–DPFD INTERFACES

Adding an APD to the DPFD requires only a copy of the LO signal (LO_A) out of phase by $\pi/2$ with respect to the digital LO (LO_D) and a digitally controlled switch to enable the APD output when $\Delta\varphi$ falls within the DPFD dead zone.

The most straightforward design generates LO_D and LO_A from LO using a 90° power splitter, distributes the rf signal between the APD and DPFD with a 0° power splitter and enables the APD output with a digitally controlled rf switch as shown in Fig. 3(a). In this way, the APD does not suffer from any jitter induced by the comparators generating the digital versions of rf and LO.

Since rf components tend to be more expensive than digital logic and the LO signal has very high S/N, it can be considered replacing the 90° splitter and the rf switch with digital circuitry as in Fig. 3(b): both LO_A and LO_D are digital signals and the phase shifting can be accomplished either by using a delay line or by starting from a LO at twice the rf frequency. Driving the APD with a digital signal from the DPFD (via a buffer or an attenuator) replaces the rf switch. The APD output is controlled by gating the LO_A, an acceptable solution since high isolation is not required.

By pushing simplification even further [Fig. 3(c)], the rf input to the APD can also be derived from a comparator. At the risk of some extra phase noise, the 0° phase shifter can also be eliminated. Driving both APD inputs with digital signals also nicely implements an automatic gain control: the APD output voltage no longer depends on the rf amplitude (but below a certain amplitude threshold phase noise increases rapidly). It is even possible to avoid any analog circuitry at all, since the analog mixer can be replaced by its digital version, an exclusive or (XOR) gate. This last PFD is completely digital but can still be divided in a short propagation delay phase detector (the XOR gate) and a broad range PFD (the phase counter).

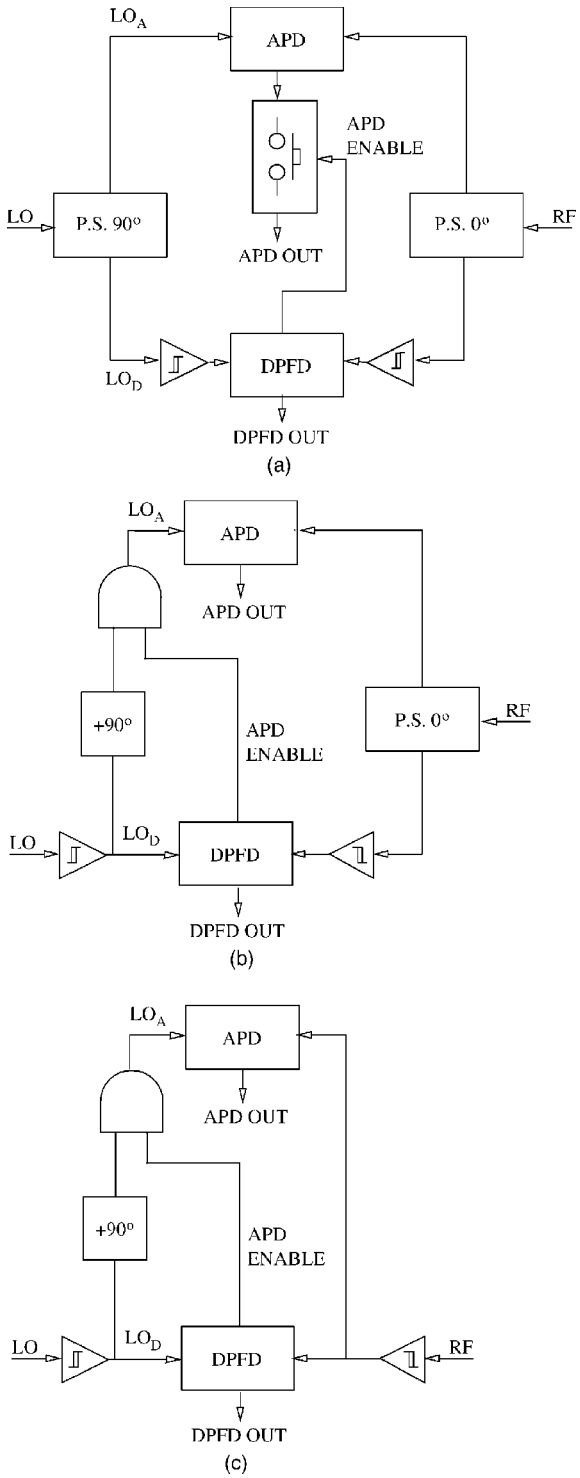

FIG. 3. Different possible APD–DPFD interfaces. (a) Both the rf and LO signals reaching the APD are analog. It requires two power splitters at 90° (power splitter (P.S.) 90°) and 0° (P.S. 0°) degrees and a digitally controlled rf switch. (b) The LO signal is digital while rf is still analog. The 90° power splitter is replaced by a digital 90° phase shifter while the APD output is gated by blocking the LO_A signal with an AND gate. (c) Same as (b) but rf is also a digital signal. No power splitters are required and the APD output is largely independent from rf amplitude. It can generate more phase noise than (a) and (b).

V. ACTUAL IMPLEMENTATION

All the DPFD components (counters, adder, comparators, and latch) are available as standard TTL indegrated circuits (ICs) in 4 bit blocks so it is straightforward to implement a DPFD with a dynamic range on the order of $\pm 12\pi$ (letting $t_u=14$, $t_l=1$) with a f_t of at least 100 MHz. The modest complexity of the circuit however makes it possible to fit all the digital components of the DPFD in a single complex programmable logic device (CPLD). A CPLD offers some distinct advantages with respect to a more traditional implementation. It is much more versatile since it can be easily reprogrammed to fix errors in the development phase and adapted to slightly different designs later [changing the number of bits in the DPFD, implementing a DPFD without a dead zone as in Fig. 1(a), adding prescalers on the inputs etc.]. The total APD+DPFD system is also less prone to noise since all the fast switching digital circuitry is concentrated in a single chip. The speed of DPFD built with a standard CPLD can reach $f_t=200$ MHz. In a low density CPLD (Altera EPM7064) an 8 bit DPFD with a dynamic range of $\pm 224\pi$ has been implemented. The CPLD program has been written in VERILOG and makes heavy use of a series of Altera specific predefined macros for counters, adders, comparators, and latches, allowing an exact correspondence between the code and the block diagram in Fig. 2.

The DPFD output is converted to a bipolar voltage of ±2.5 V, giving an average slope of 3.55 mV/rad, by a standard 8 bits current output DAC (Analog Device DAC08) and an operational amplifier converting current to voltage. A trimmer is provided to adjust the output voltage offset.

We have implemented the APD+DPFD interface in the simplified form of Fig. 3(c). The low $\langle \varphi^2 \rangle$ obtained has justified this choice. Both the rf and LO signals are converted to TTL logic levels by a couple of fast comparators (Linear Technology LT1016) driving, a 500 MHz APD (MiniCircuits RPD—1) providing a nominal output of 1 V/rad. The signals at the APD inputs have been adapted at +7 dBm with a resistive network. The main reason for using a real APD instead of a XOR gate is the lower propagation time, reducing the total loop delay.

The 90° phase shifter is a chain of eight noninverting buffers cascaded to form a delay line implemented around a TTL octal three—state buffer (SN74245). Each buffer adds a delay of about 2 ns. The proper output is selected with a jumper. The three—state control of the buffer switches the LO_A signal [replacing the AND gate in Fig. 3(c)]. A better solution would be a proper multitap delay line with a 1 or 2 ns delay per tap. In principle, it would also be possible to include the delay line into the CPLD. However, this is explicitly not recommended by the manufacturer. A frequency independent 90° phase shift generated by starting from a LO at twice the frequency and two flip flops commuting on opposite wave fronts is probably, however, the best solution if a suitable high frequency source for the LO is available. This last point is not totally trivial: in many interferometers, a frequency tunable, phase continuous, OPLL is required, forcing the use of a direct—digital—synthesis (DDS) oscillator as the LO source. Most of the DDSs with potentially low phase noise (i.e., after using a high quality master clock) have a maximum output frequency of 15–30 MHz, already below the optimum value (roughly $f_t/2$) maximizing the capture range.

Control signals are limited to upper and lower saturation detectors connected to light emitting diodes on the front panel. Two switches can separately enable the APD and the DPFD, allowing APD only, DPFD only, or APD+DPFD operation.

VI. EXPERIMENTAL SETUP

A detailed description of our interferometer has already been published elsewhere.[7,18] Therefore we will briefly summarize here only the setup involving the generation of the three $\pi/2-\pi-\pi/2$ Raman pulses forming the interferometric sequence.

As ML and SL we have used different laser diodes (Sanyo, Sharp, and Sacher) with similar results. The measurements presented in Sec. VII however have all been obtained with a Sanyo ML and a Sharp SL.

The laser diodes have been assembled in extended cavities with lengths of 1.5 and 3 cm, terminated by a 1800 lines/mm grating, mounted in Littrow configuration with a mechanical design similar to that described in Ref. 19. Injection current and temperature stabilization are provided by homemade electronics. When running at 80–90 mA, the typical optical power after the extended cavity is 25 mW. After a pair of anamorphic prisms, a 30 dB optical isolator and a half—wave plate, the ML and SL beams are combined on a polarizing beam splitter (PBS). The two half-wave plates are used to balance the ML and SL intensities on both PBS outputs; the first output carries a total power of less than 1 mW and, after a 45° polarizer, is sent to a fast photodiode (New-Focus 1002) with a responsivity of 0.1 mA/mW for generating the ML–SL beat note. The second PBS output injects a tapered amplifier whose transverse profile is cleaned by a cylindrical lens and a fiber. A hot Rb cell provides filtering in the frequency domain. The Raman beams finally reach an acousto-optic modulator (AOM). The AOM transmission is controlled by an arbitrary function generator, producing the pulse sequence.

The width of $\pi/2$ pulses is about $\tau=50\ \mu$s, while the total duration of the $\pi/2-\pi-\pi/2$ interferometric sequence is typically $2T=200$ ms.

The beat note at about 6.8 GHz detected by the photodiode is amplified (27 dB) by a low noise figure (below 2 dB) 4–8 GHz amplifier (JCA 48-301). A first downconversion stage is formed by a mixer with conversion losses of 5.5 dB (MITEQ M0408) and a fixed frequency low phase noise local oscillator (Anritsu MG3692A) at about 6.874 GHz. The mixer intermediate frequency (IF) output is further amplified (27 dB) by a 500 MHz amplifier (MiniCircuits ZFL—500 LN) and finally sent to a −10 dB directional coupler. The 10% output is used for analysis and monitor (residual phase noise measurements or observation with a spectrum analyzer) while the 90% output is sent to the rf input of the APD+DPFD detector. The LO input is provided by a 80 MHz DDS (Agilent 33250A) phase locked to the 10 MHz Anritsu time base. During the interferometric sequence the DDS must execute phase-continuous linear frequency ramps to compensate for the gravity-induced Doppler shift, due to the parabolic flight of the atomic cloud. To characterize the OPLL, however, the DDS has been operated at a fixed frequency of 40 MHz.

The DPFD and APD outputs drive a three–paths feedback loop acting on the SL injection current, both directly at the laser mount (fast current path) and via the current driver (slow current path), and on the SL external cavity length, via a low voltage piezo stack [piezo transducer (PZT) path].

The fast current path is directly derived from the APD. The IF output enters a 6 dB gain stage (also lowering the APD output impedance) followed by a gain setting resistive voltage divider with an output impedance close to 50 Ω. A standard RG-58 coaxial cable connects the fast output to the laser diode through a passive network formed by an impedance matching 50 Ω resistor to ground and a 1 kΩ in parallel with a small capacitor in the 220–680 pF range. The resistor of the passive filter acts as a 1 mA/V voltage-to-current converter, while the capacitor provides an essential phase lead starting from 300 kHz to 1.2 MHz that compensates a pole generally present in the frequency modulation response of diode lasers. A large (1 μF or so) dc blocking capacitor can also be included. A servo bandwidth of at least 3 MHz or better is usually possible, but care should be taken to minimize the length of optical and electrical paths from the laser to the photodiode, the APD and back, since the loop delay can produce a significant phase shift. The total delay should be kept below 28 ns for a phase shift of less than 30° at 3 MHz. Every 30 cm of free space or 20 cm of RG-58 cable will add 1 ns. The propagation delay of the comparator should also be taken into account.

The slow current path acts on the modulation input of the current source. Our drivers include a modulation circuit similar to that described in Ref. 20, with a bandwidth exceeding 1 MHz and a gain of 100 μA/V. The APD output is processed by a passive lag-lead network with the pole around 10 kHz and zero at 300 kHz and is then combined with the DPFD output with the proper gain ratio and sent to the current driver. An optional inverter can be used to adjust the sign of the feedback. The slow current loop serves both for the purpose of safely (for the SL) increasing the gain of the analog loop in the frequency region where the interferometer is more sensitive to phase noise (see below) and for that of pushing the bandwidth of the digital loop up to few tens of kHz.

The PZT path sums both the APD and DPFD and includes a proportional-integral amplifier, an optional inverter, and an output offset stage for manually tuning the SL operating frequency. The crossing between proportional and integral part is around 200 Hz and the unity gain frequency f_{PZT} is 1 kHz for the APD, a bit less for the DPFD, and is limited by the PZT frequency response. The frequency tuning coefficient at the PZT input is on the order of 1 GHz/V. The extra integrator ensures that at low frequency the PZT path will have higher gain than the current ones. The crossover is around 1 Hz.

The complete DPFD and APD circuitry plus the loop filter has been assembled on a standard Euro Card size (160×100 mm^2) double layer printed circuit board.[21]

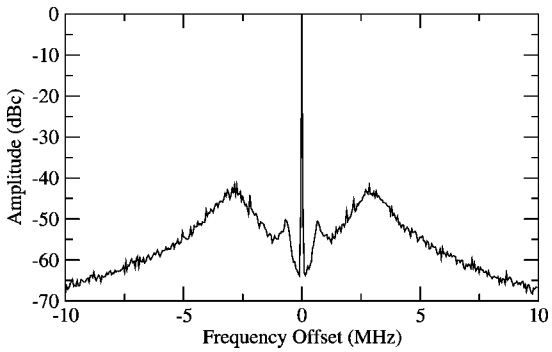

FIG. 4. Closed loop beat note signal at 40 MHz. The servo bumps at 800 kHz and 3 MHz due to the slow and fast current loop are clearly visible. The resolution bandwidth is 10 kHz. The plot is the average of 100 scans.

VII. RESULTS

A typical spectrum of the 40 MHz closed loop beat note is shown in Fig. 4. A numerical integration shows that the fraction of power in the carrier amounts to 0.985.

The closed loop square modulus of the single-sided phase noise spectral density S_φ has been recorded by demodulating the 40 MHz beat note at the directional coupler output.

In order to reject the DDS contribution to the phase noise, an analog mixer compares the beat note (LO input) directly to a 90° out of phase copy of the DDS signal (rf input). The Fourier transform of the IF output, scaled to $\mathrm{rad}^2/\mathrm{Hz}$, is shown in Fig. 5.

In the frequency range from 5 Hz to 200 kHz S_φ can be approximated by

$$S_\varphi = \begin{cases} \alpha_\varphi/f & \text{if } 5\ \mathrm{Hz} < f < 200\ \mathrm{Hz}, \\ \beta_\varphi & \text{if } 200\ \mathrm{Hz} < f < 20\ \mathrm{kHz}, \\ \gamma_\varphi f^2 & \text{if } 20\ \mathrm{kHz} < f < 200\ \mathrm{kHz}, \end{cases} \tag{1}$$

with $\alpha_\varphi = 3\times10^{-9}\ \mathrm{rad}^2$, $\beta_\varphi = 1\times10^{-11}\ \mathrm{rad}^2/\mathrm{Hz}$, and $\gamma_\varphi = 2.5\times10^{-20}\ \mathrm{rad}^2/\mathrm{Hz}^3$.

Above 200 kHz, the servo bumps of the slow and fast current loops, at 800 kHz and 3 MHz respectively, are clearly visible.

In the following we will refer to the $1/f$, white, and f^2 noise zones of S_φ as zone I,II, and III, respectively, while the servo bumps region, above 200 kHz, will be referred to as zone IV.

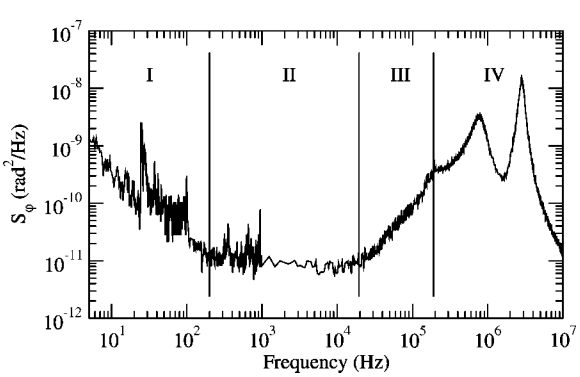

FIG. 5. Square modulus of the single-sided phase noise spectral density S_φ from 5 Hz to 10 MHz of the OPLL. The spectrum is divided in four different regions according to the power laws that they follow.

TABLE I. Contributions to the mean square phase noise angle $\langle\varphi^2\rangle$ of the OPLL and to the square of phase resolution of the interferometer $\Delta\Phi^2_{\mathrm{OPLL}}$ [see Eq. (3)] from the four noise zones of S_φ.

S_φ zone	$\langle\varphi^2\rangle(\mathrm{rad}^2)$	$\Delta\Phi^2_{\mathrm{OPLL}}(\mathrm{rad}^2)$
I	1×10^{-8}	9×10^{-8}
II	20×10^{-8}	46×10^{-8}
III	6.7×10^{-5}	23×10^{-8}
IV	1.1×10^{-2}	34×10^{-8}
Total	1.1×10^{-2}	112×10^{-8}

By integrating S_φ we obtain $\sqrt{\langle\varphi^2\rangle}\simeq 100$ mrad in the 5 Hz–10 MHz bandwidth. The contribution to $\langle\varphi^2\rangle$ from each one of the four S_φ noise zones is reported in Table I.

An atom interferometer measures the transition probability p between two atomic states, expressed as

$$p = \tfrac{1}{2}(1 + C\cos\Phi) \tag{2}$$

where C is the contrast of the atomic fringes and Φ is the relative phase accumulated along the two interfering paths. The sensitivity Δp depends then on the S/N ratio of the detection ΔC and the phase resolution $\Delta\Phi$. To evaluate the impact of S_φ on $\Delta\Phi$ the procedure outlined in Ref. 22 can be followed. As a result, the contribution $\Delta\Phi^2_{\mathrm{OPLL}}$ of the OPLL phase noise to $\Delta\Phi^2$ is given by a weighted value of the S_φ integral

$$\Delta\Phi^2_{\mathrm{OPLL}} = \int_0^\infty S_\varphi(f)|H(f)|^2 df, \tag{3}$$

where $H(f)$ is the Fourier transform of the interferometer sensitivity function $h(t)$, given by

$$h(t) = \begin{cases} \omega_0\cos[\omega_0(t+T)] & \text{for } -T \leqslant t \leqslant -T+\tau, \\ \omega_0\cos[\omega_0(t-T)] & \text{for } T-\tau \leqslant t \leqslant T, \\ -\omega_0\cos(\omega_0 t) & \text{for } -\tau \leqslant t \leqslant \tau, \\ 0 \quad \text{otherwise}, \end{cases} \tag{4}$$

where $2T$ and τ are defined as in Sec. VI, while $\omega_0 = 2\pi f_0 = \pi/(2\tau)$. Therefore, one gets

$$|H(f)|^2 = \frac{16 f_0^4}{(f^2 - f_0^2)^2}\sin^2(\pi f T)\left[\sin[\pi f(T-2\tau)] + \frac{f}{f_0}\cos(\pi f T)\right]^2. \tag{5}$$

As intuitively expected, both low frequency noise, at $f < f_1 = 1/(\pi T)$ and high frequency noise, at $f > f_0 = 1/(4\tau)$ are heavily attenuated by $|H(f)|^2$. Note that the apparent second order pole at $f = f_0$ is not real since it is compensated for by a corresponding zero by the term in square brackets. For an evaluation of $\Delta\Phi^2_{\mathrm{OPLL}}$, approximate expressions for Eq. (5) can be easily obtained. Again, the contributions to $\Delta\Phi^2_{\mathrm{OPLL}}$ from the four S_φ noise zones are listed in Table I. The zone I value has been overestimated by extending the low frequency integration limit to zero.

The total value of $\Delta\Phi_{\mathrm{OPLL}}$ is 1.1 mrad, with comparable contributions from all the four zones.

Improving $\langle\varphi^2\rangle$ essentially requires reducing the servo bumps area. By developing a broadband current modulator, a single current loop can probably be used, both simplifying the feedback circuitry and removing the 800 kHz bump. Alternatively, a more careful crossover between the fast and slow current paths should be implemented.

Reducing $\Delta\Phi^2_{\mathrm{OPLL}}$, however, requires improvements in all zones. At present the $1/f$ excess noise is probably limited by an insufficient rf level on the mixer in the first downconversion stage. The white noise floor β_φ is roughly consistent (within a factor of 3) with the limits set by the amplitude S/N ratio of the ML–SL beat note. Replacing the photodiode with a model capable of higher optical power levels (more than 1 mW) can then probably lower β_φ. The f^2 zone is caused by insufficient loop gain for $f>20$ kHz so an extra lag-lead network or an extra integrator are required starting to further increase gain at a few hundred kHz.

We have not observed any evidence of extra phase noise generation by driving the rf and the LO APD input signals with the digital outputs of two fast voltage comparators. Reaching the ultimate β_φ however might require driving the APD with an analog rf signal.

As far as stability and reliability are concerned, the DPFD ensures a capture range of about 80 MHz, which could be easily improved by adopting a faster CPLD, and usually unrecoverable losses of lock in the OPLL (requiring manual intervention) are induced only by thermal drifts in the ML or SL laser.

ACKNOWLEDGMENTS

This work was supported by INFN, MIUR, INFM, ASI, CRF, and LENS. The authors would like to thank R. Drullinger for a critical reading of the manuscript.

[1] T. Udem, A. Huber, B. Gross, J. Reichert, M. Prevedelli, M. Weitz, and T. W. Hänsch, Phys. Rev. Lett. **79**, 2646 (1997).
[2] T. Udem, J. Reichert, R. Holzwarth, and T. W. Hänsch, Phys. Rev. Lett. **82**, 3568 (1999).
[3] G. Santarelli, A. Clairon, S. N. Lea, and G. M. Tino, Opt. Commun. **104**, 339 (1994).
[4] *Atom Interferometry*, edited by P. R. Berman (Academic, New York, 1997).
[5] D. S. Weiss, B. C. Young, and S. Chu, Appl. Phys. B: Lasers Opt. **B59**, 217 (1994).
[6] R. Battesti, P. Cladé, S. Guellati-Khélifa, C. Schwob, B. Grémaud, F. Nez, L. Julien, and F. Biraben, Phys. Rev. Lett. **92**, 253001 (2004).
[7] M. Fattori, G. Lamporesi, T. Petelski, J. Stuhler, and G. M. Tino, Phys. Lett. A **318**, 184 (2003).
[8] S. C. A. Peters and K. Y. Chung, Metrologia **38**, 25 (2001).
[9] J. M. McGuirk, G. T. Foster, J. B. Fixler, M. J. Snadden, and M. A. Kasevich, Phys. Rev. A **65**, 033608 (2002).
[10] F. Yver-Leduc, P. Cheinet, J. Fils, A. Clairon, N. Dimarcq, D. Holleville, P. Bouyer, and A. Landragin, J. Opt. B: Quantum Semiclassical Opt. **5**, S136 (2003).
[11] Specific commercial products are named for the sole purpose of an easier reproduction of our results. Other components can have similar or superior characteristics.
[12] M. Prevedelli, T. Freegarde, and T. W. Hänsch, Appl. Phys. B: Lasers Opt. **B61**, S241 (1995).
[13] J. Ye and J. Hall, Opt. Lett. **24**, 1838 (1999).
[14] A. Peters, Ph D thesis, Stanford University, Stanford, CA, 1998.
[15] The notable exception of a very low $\langle\varphi^2\rangle$ OPLL based only on a DPFD has been developed at BNM-SYRTE.
[16] N. Beverini, M. Prevedelli, F. Sorrentino, B. Nyushkov, and A. Ruffini, Quantum Electron. **34**, 559 (2004).
[17] D. Mazzotti, P. Cancio, G. Giusfredi, P. D. Natale, and M. Prevedelli, Opt. Lett. (in press).
[18] J. Stuhler, M. Fattori, T. Petelski, and G. M. Tino, J. Opt. B: Quantum Semiclassical Opt. **5**, S75 (2003).
[19] L. Ricci, M. Weidenmüller, T. Esslinger, A. Hemmerich, C. Zimmermann, V. Vuletic, W. König, and T. W. Hänsch, Opt. Commun. **117**, 541 (1995).
[20] K. G. Libbrecht and J. Hall, Rev. Sci. Instrum. **64**, 2133 (1993).
[21] Complete schematics, parts list, Verilog source code, Gerber files, data sheets etc. are available sending e-mail to the corresponding author.
[22] P. Cheinet, B. Canuel, F. P. D. Santos, A. Gauguet, F. Leduc, and A. Landragin (unpublished)