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Hybridge Zero–Current–Switching Rectifier for High–Frequency DC–DC Converter Applications

M. Bartoli, A. Reatti, Member, IEEE
University of Florence, Department of Electronic Engineering,
Via di S. Marta, 3, 50139 Florence – Italy
Phone: (39)(55)4796389 and Fax: (39)(55)494569;
E –"Mail: MAILSERVER@MAILSERVER.IDG.CNR.FI
and
M. K. Kazimierczuk, Senior Member, IEEE
Wright State University, Department of Electrical Engineering,
Dayton, Ohio 45435, USA
Phone: (513)873–5059 and Fax: (513)873–5009;
E – Mail: MKAZIM@VALHALLA.CS.WRIGHT.EDU

Abstract – An analysis and experimental verification of a hybridge current–driven zero–current–switching rectifier are given. In the hybridge rectifier, the diodes turn on at zero *di/dt,* low *dv/dt,* and turns off at low *di/dt*. Therefore, the hybridge rectifier is suitable for high–frequency high–efficiency applications. The current source driving the rectifier can be constituted by a class D or a class E inverter. Since these inverters operate with nearly zero switching losses, high power–density dc–dc converters can be assembled by using resonant inverters and hybridge rectifiers. A dc–dc converter based on a class D series resonant inverter and a hybridge rectifier was designed and tested for a constant output voltage V_O = 12 V and an output current I_O from no–load to 12 A. The converter was operated at a dc input voltage ranging from 200 to 380 V and a minimum frequency of f = 600 kHz. The theoretical results and measured performances were in good agreement. A maximum converter efficiency as high as 90% has been achieved for the dc–dc converter operated at full load.

I. Introduction

High–frequency rectifiers are needed to build high power–density dc–to–dc converters. Bridge rectifiers provide a full–wave rectification and require a simple transformer with only one secondary winding. However, two diodes are simultaneously ON during each half–period. This results in high power losses at a high output current operation. Moreover, voltage drops across the diodes make the full–bridge rectifier unsuitable for low output voltage applications. Rectifier losses can be reduced using the well–known center–tapped rectifier. However, the transformer in this circuit have two secondary windings which are not efficiently used because the current flows in each secondary winding only for one–half of the switching period. In the hybridge rectifier, a transformer with only one secondary winding is used [1]–[7]. Moreover, the rms value of the secondary side ac–current is half of that circulating in the center–tapped rectifier. The limitation of this rectifier circuit is that high–switching losses and high noise level are produced at frequencies above 500 kHz if it is operated with a pulse–width–modulated (PWM) voltage or current source at the primary side. Thus, soft–switching operation is highly desirable to achieve an high–frequency high–efficiency full–wave rectification. This is achieved if the hybridge rectifier is driven by a sinusoidal current source. Actually the current source can be realized by using a class E or a class D series resonant inverter [7]–[15]. Switching losses are nearly zero in these inverters, and, therefore, they can be operated at high frequency with an high efficiency. As a result, high power–density dc–dc converters can be assembled by using resonant inverters and hybrigde rectifiers.

The purpose of this paper is to present design equations and experimental results for a hybridge current–driven zero–current–switching (ZCS) low *di/dt* rectifier. This rectifier preserves major advantages of conventional bridge and center–tapped rectifiers and overcomes many limitations of these circuits. As in full–wave full–bridge and center–tapped rectifiers, the filter capacitors are small because they are operated at a frequency which is twice that of the input source. Conduction losses in the diodes are reduced because the average current through each diode is one–half of the output dc current as in center–tapped rectifiers. However, each inductor of the hybridge rectifier carries one–half of the dc output current while the entire output current flows through the output inductor in the center–tapped rectifier. As a result, conduction losses are lower in the hybridge rectifiers. The hybridge current–driven zero–current–switching (ZCS) low *di/dt* rectifier overcomes also the limits of its PWM counterpart because the diode current and voltage waveforms do not overlap at diode transitions. Moreover, the diodes turn on at zero voltage and zero current with zero *di/dt* and limited *dv/dt* and turn off with a limited *di/dt*. As a result, the switching losses and noise level are drastically reduced in the hybridge current–driven zero–current–switching (ZCS) low *di/dt* rectifier. Therefore, this rectifier can be operated at higher frequencies than a PWM hybridge rectifier, resulting in a lower volume and weight. This allows for operations at low output voltage ripple also when small capacitances and inductances are used.

The hybridge current–driven zero–current–switching (ZCS) low *di/dt* rectifier circuit was used in combination with a class D series resonant inverter used as a current source. A 144 W dc–dc converter was assembled and operated as a voltage regulator at a dc voltage ranging from 200 to 380 V dc, an output voltage V_O = 12 V regulated over the entire line voltage range and from no–load to a full load I_O =12 A. The dc–to–dc converter was frequency–controlled in the 650–to–950 kHz range. A maximum dc–to–dc converter efficiency η above 90% was achieved at full load.

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II. Rectifier Circuit Description And Operation

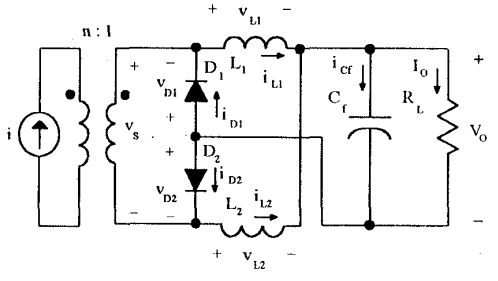
A circuit for a hybridge current-driven ZCS low *di/dt* is shown in Fig 1. Figs 1(a) and (b) show the non-inverting and the inverting circuit of the hybridge rectifier. Each of the two circuits are driven by a sinusoidal current source with

$$i = I_m \sin \omega t \tag{1}$$

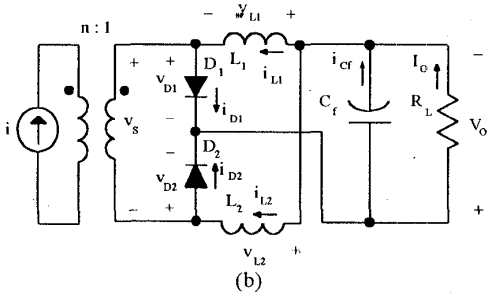
where I_m is the current amplitude, $\omega = 2\pi f$ is the angular frequency of the current, and f is the operating frequency of the current source and rectifier transformer. The rectifier circuit consists of two diodes D_1 and D_2, two inductors L_1 and L_2, and a filter capacitor C_f. Resistance R_L represents the dc load. The two inductors and single-pole low-pass rectifier composed by the parallel combination of C_f and R_L are operated at a frequency of $2f$ while diodes are operated at a frequency of f. This results in small volume inductors and capacitors. Moreover, a low ac ripple of the output voltage can be easily achieved with reduced values of capacitance C_f because the filter capacitor is operated at twice the input current frequency.

In the inverting rectifier circuit of Fig. 1(b), the two diodes have a common cathode connection. Therefore, the center tapped rectifiers normally available on the market with two diodes built in the same case can be used. This results in a reduction of the number of components and volume of the rectifier circuit.

Figs. 2(a) to (d) and (e) to (h) show the four topological modes the rectifier of Fig. 1(a) goes through during one switching period for a diode on-duty cycle $0 < D \leq 0.5$ and $0.5 < D \leq 1$, respectively.



(a)



(b)

Fig. 1. Schematic circuit of the hybridge current-driven rectifier.
(a) Non-inverting circuit.
(b) Inverting circuit

The inverting rectifier circuit of Fig. 1(b) goes through four topological modes as the non-inverting rectifier. The difference between the two rectifier topological modes are the current directions in the circuit components.

The voltage and current waveforms for the rectifier of Fig. 1(a) are shown in Fig. 3. These waveforms are the same also for the inverting rectifier of Fig. 1(b).

A. Operation for $0 < D \leq 0.5$

During the first topological mode of Fig. 2(a), D_1 is ON, the load is supplied by the current source through the transformer secondary side represented by a current source ni. When D_1 is ON, the voltage across L_1 is equal to the reverse output voltage V_O, and the current through diode D_1 is $i_{D1} = i_{L1} - ni$ and increases with limited *di/dt*. Moreover, *di/dt* is zero at diode D_1 turn-on. When the i_{D1} reaches zero, diode D_1 turns off and mode II begins. During mode II inductors L_1 and L_2 and the transformer are in the same current path and the output capacitor C_f supplies the current to the dc load. The voltages across the inductors are sinusoidal and the reverse voltage across the diodes are portion of a sinusoid shifted downward by a DC voltage V_O. When the voltage across D_2 reaches its threshold, D_2 turns on at low *dv/dt* and zero *di/dt* with theoretically zero switching losses. During mode III, I_O partially flows through diode D_2 in series with inductor L_2 and partially through inductor L_1. When diode D_2 turns off, mode III ends and mode IV begins. The current path of mode IV is identical to that of mode II.

B. Operation for $0.5 < D \leq 1$

The circuit operation for $0.5 < D \leq 1$ is similar to that described for $0 < D \leq 0.5$. The main difference is that both D_1 and D_2 are ON during modes I and III. As a consequence, both inductors L_1 and L_2 store part of the energy absorbed by the load resistance, reducing the current through the transformer windings and the ac voltage ripple across C_f.

III. Rectifier Design Equations

The equations for the rectifier design are derived under the following assumptions:

1) Diodes are modelled as ideal switches.
2) The transformer is ideal, the turns ratio is n, and the transformer leakage inductances are neglected.
3) The output voltage is equal to V_O and is assumed to have a zero ripple.
4) The rectifier circuit is symmetric. Therefore, we have $L_1 = L_2 = L$.

Results of the analysis are valid for both the operation at $0 < D \leq 0.5$ and $0.5 < D \leq 1$.

The initial turn-on delay angle of diode D_1 is

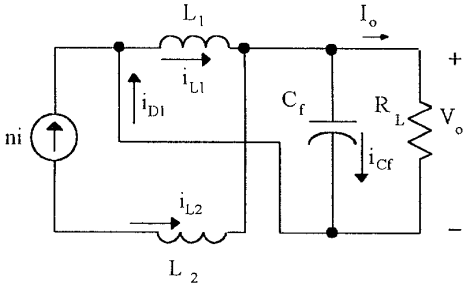
$$\phi = tg^{-1}\left[\frac{\sin 2\pi D - 2\pi D}{1 - \cos 2\pi D}\right]. \tag{2}$$

Since a symmetrical operation of the rectifier is assumed, angle ϕ is also the delay angle of diode D_2. A plot of ϕ as a function of D is depicted in Fig. 4. The amplitude of the sinusoidal input current is given as function of ϕ as follows

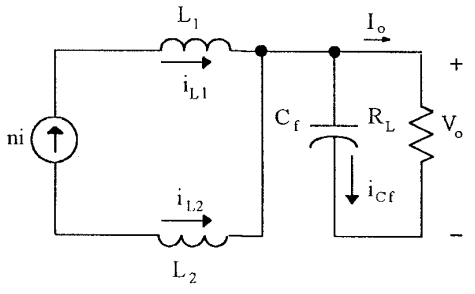
$$I_m = -\frac{V_O}{n\omega L \cos\phi}. \tag{3}$$

The load resistance R_L normalized with respect to the reactance $\omega L = \omega L_1 = \omega L_2$ as a function of the on-diode duty cycle is

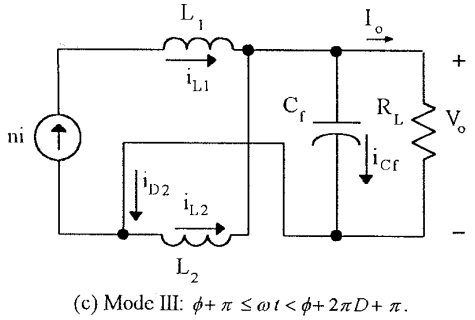
$$\frac{R_L}{\omega L} = \frac{\pi(1 - \cos 2\pi D)}{(1 - \cos 2\pi D)^2 + (\sin 2\pi D - 2\pi D)^2 + 2\pi^2 D^2 (1 - \cos 2\pi D)}. \tag{4}$$



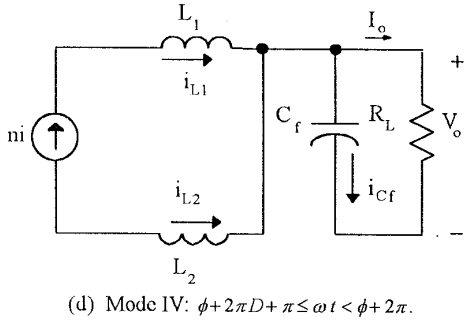
(a) Mode I: $\phi \le \omega t < \phi + 2\pi D$.



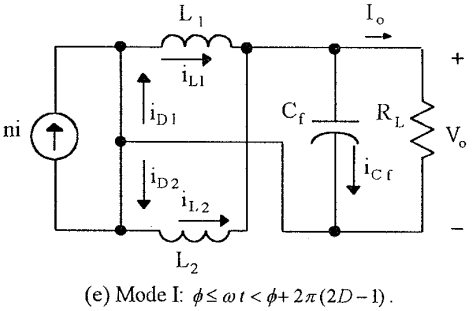
(b) Mode II: $\phi + 2\pi D \le \omega t < \phi + \pi$.



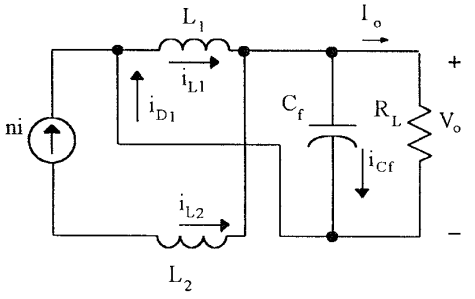
(c) Mode III: $\phi + \pi \le \omega t < \phi + 2\pi D + \pi$.



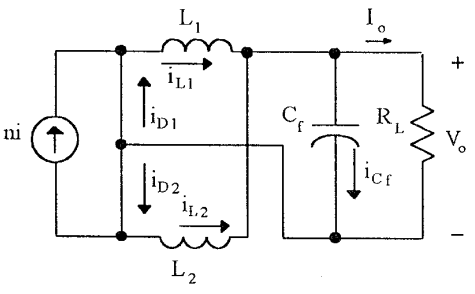
(d) Mode IV: $\phi + 2\pi D + \pi \le \omega t < \phi + 2\pi$.



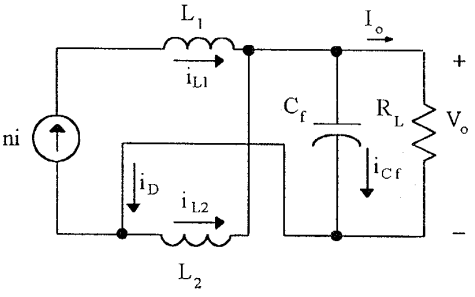
(e) Mode I: $\phi \le \omega t < \phi + 2\pi(2D-1)$.



(f) Mode II: $\phi + 2\pi(2D-1) \le \omega t < \phi + 2\pi D$.



(g) Mode III: $\phi + 2\pi D \le \omega t < \phi + \pi$.



(h) Mode IV: $\phi + \pi \le \omega t < \phi + 2\pi$.

Fig. 2. Equivalent circuits of the hybridge current rectifier for various intervals.
(I) Operation at $0 \le D < 0.5$: (a) D_1 ON and D_2 OFF, (b) D_1 OFF and D_2 OFF, (c) D_1 OFF and D_2 ON, (d) D_1 OFF and D_2 OFF.
(II) Operation at $0.5 \le D < 1$: (e) D_1 ON and D_2 ON, (f) D_1 ON and D_2 OFF, (g) D_1 ON and D_2 ON, (h) D_1 OFF and D_2 ON.

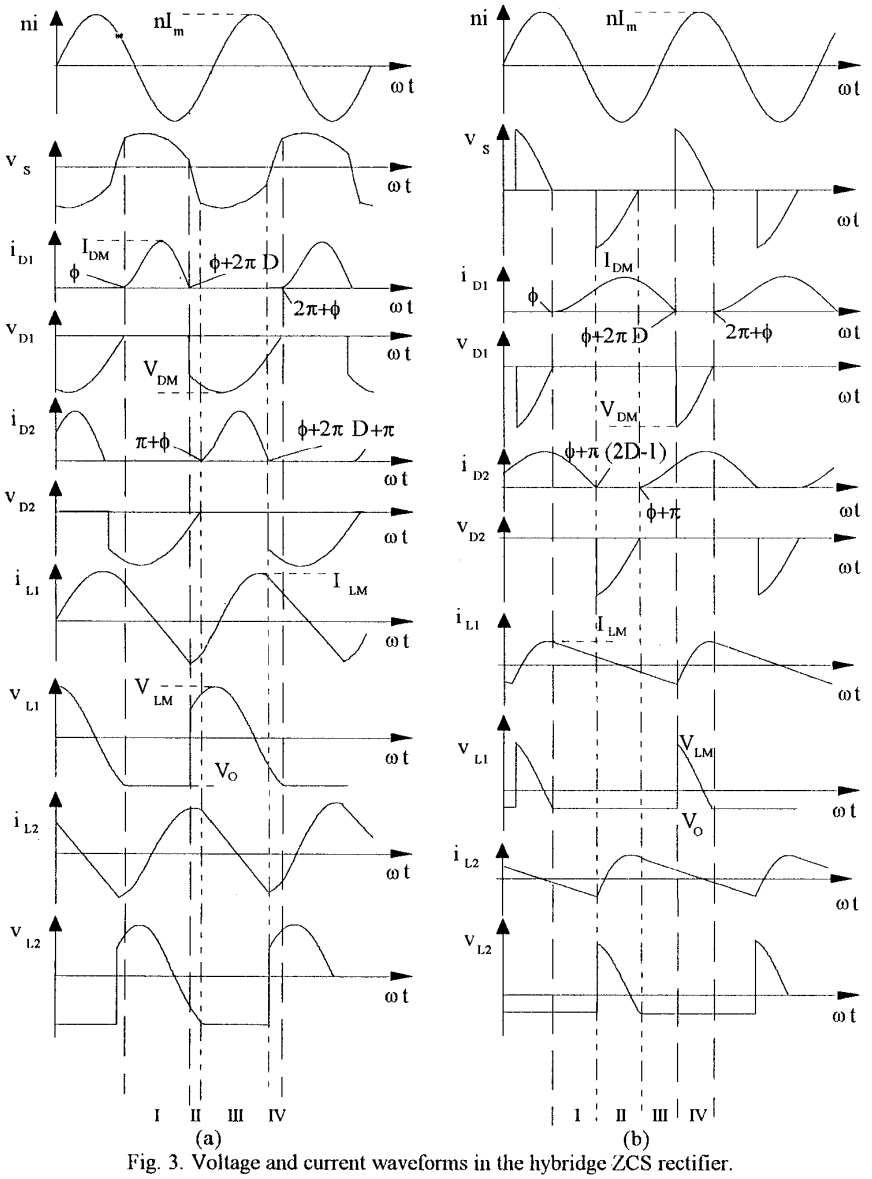


Fig. 3. Voltage and current waveforms in the hybridge ZCS rectifier.
(a) For $0 < D \leq 0.5$. (b) For $0.5 < D \leq 1$.

Fig. 5 shows the on–duty cycle D as a function of the load resistance R_L normalized with respect to the reactance ωL.
The maximum current through the inductors normalized with respect to I_O is given by

$$\frac{I_{LM}}{I_O} = -\frac{R_L}{\omega L \cos\phi} = \frac{\pi(\cos 2\pi D - 1)}{\cos\phi\left[(1-\cos 2\pi D)^2 + (\sin 2\pi D - 2\pi D)^2 + 2\pi^2 D^2(1-\cos 2\pi D)\right]} \tag{5}$$

and is plotted in Fig. 6 as a function of $R_L / \omega L$.
The maximum current through each diode is expressed as

$$\frac{I_{DM}}{I_O} = -2\frac{R_L}{\omega L}(\pi - \phi + \tan\phi) = \frac{2\pi\left[(\phi-\pi)(1-\cos 2\pi D) - \sin 2\pi D + 2\pi D\right]}{(1-\cos 2\pi D)^2 + (\sin 2\pi D - 2\pi D)^2 - 2\pi^2 D^2(1-\cos 2\pi D)} \tag{6}$$

Fig. 7 shows the plot of I_{DM} / I_O versus $R_L / \omega L$.
The maximum reverse diode voltage across each diode normalized with respect to V_O is

$$\frac{V_{DM}}{V_O} = 1 - \frac{1}{\cos\phi} \tag{7}$$

and is plotted as a function of $R_L / \omega L$ in Fig. 8.

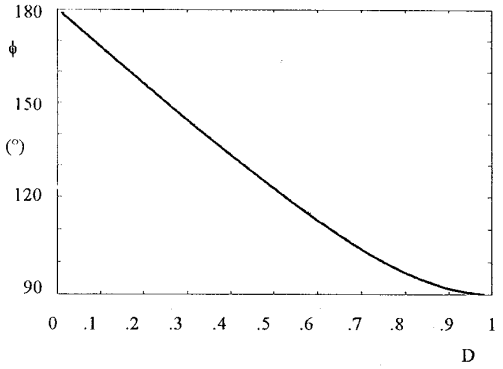


Fig. 4. Delay angle ϕ as a function of the diode on–duty cycle D

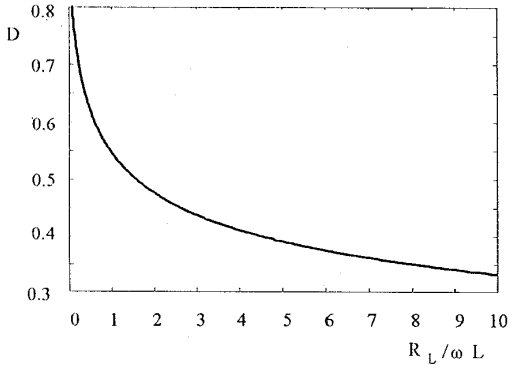


Fig. 5. Duty–cycle D as a function of the normalized load resistance $R_L / \omega L$.

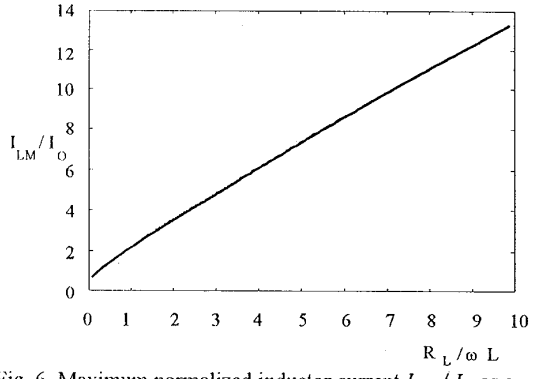


Fig. 6. Maximum normalized inductor current I_{LM} / I_O as a function of the normalized load resistance $R_L / \omega L$.

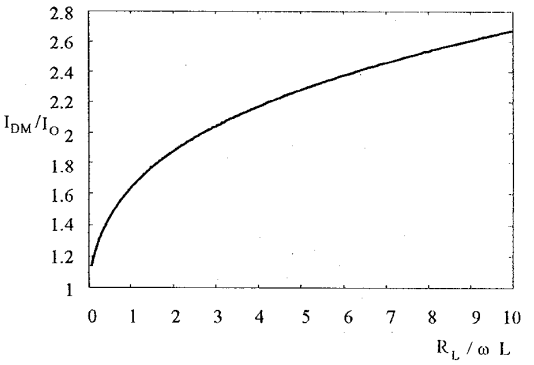


Fig. 7. Maximum normalized diode current I_{DM} / I_O as a function of the normalized load resistance $R_L / \omega L$.

The voltage across the equivalent input resistance of the rectifier as seen at the terminals of the transformer primary side normalized with respect to the output voltage V_O is given by

$$\frac{V_{Rim}}{nV_O} = 2\cos(\phi + 2\pi D) - 2\cos\phi + \frac{sin^2(\phi + 2\pi D) - sin^2\phi}{cos\phi} \quad (8)$$

and is plotted in Fig. 9 as a function of the normalized load resistance.

The input resistance of the rectifier normalized with respect to the load resistance R_L is given by

$$\frac{R_I}{n^2 R_L} = \frac{\omega L}{\pi R_L} x\left[2 - sin^2\phi + cos^2\phi - cos\phi\, cos(\phi + 2\pi D) - sin^2(\phi + 2\pi D)\right] \quad (9)$$

and is plotted in Fig. 10 as a function of the normalized load resistance $R_L/\omega L$.

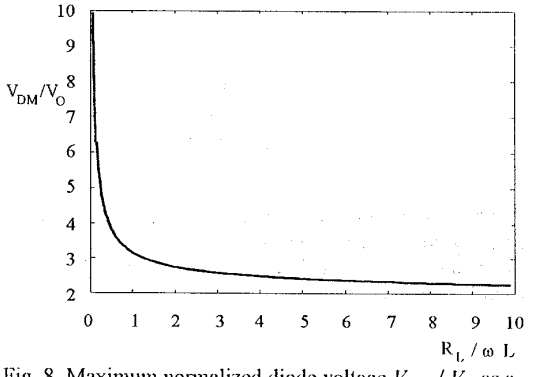


Fig. 8. Maximum normalized diode voltage V_{DM} / V_O as a function of the normalized load resistance $R_L / \omega L$.

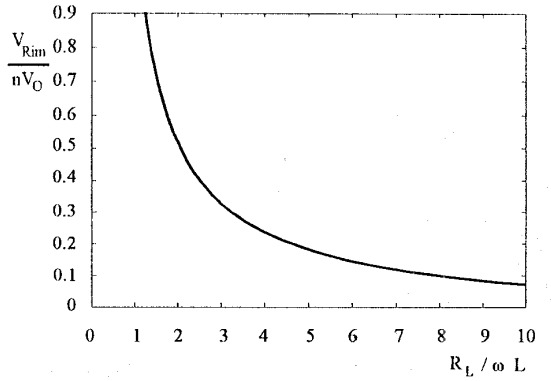


Fig. 9. Normalized primary side resistive voltage $V_{Rim} / n V_O$ as a function of the normalized load resistance $R_L / \omega L$.

The design parameters of the hybridge ZCS rectifier are summed up in Table I.

TABLE I. RECTIFIER DESIGN PARAMETERS

D	ϕ (°)	$R_L/\omega L$	I_{DM}/I_O	V_{DM}/V_O
0.1	168	143	8.89	2.02
0.2	156	86	4.44	2.09
0.3	144	15.8	2.96	2.23
0.4	133	4.49	2.22	2.46
0.5	122	1.57	1.78	2.86
0.6	112	.6	1.49	3.61
0.7	104	.233	1.28	5.21
0.8	96.6	.079	1.137	9.7
0.9	91	.0167	1.04	33.7

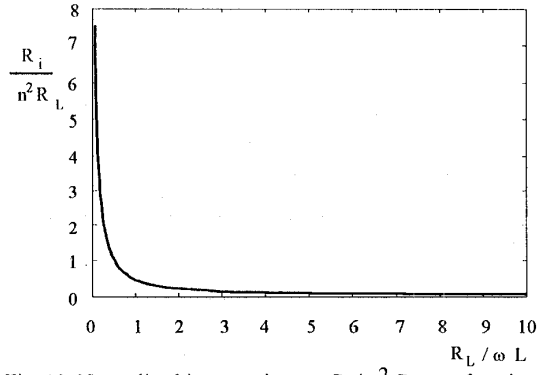


Fig. 10. Normalized input resistance $R_i / n^2 R_L$ as a function of the normalized load resistance $R_L / \omega L$.

IV Design Example

A dc–dc converter was built and tested to achieve the following design specifications:

– Output power P_O = 144 W.
– Output voltage V_O = 12 V.
– Output current I_O from 3 to 100 % of the nominal output current I_{ON} = 12 A.
– Input voltage V_{Imin} = 200 Vdc and V_{Imax} = 380 Vdc.
– Output power P_O = 144 W.
– Minimum transformer operating frequency f = 600 kHz.

The schematic circuit of the dc–dc converter constituted by a class D resonant inverter and a hybridge rectifier is shown in Fig. 11. The inverter is operated as a nearly sinusoidal current source.

The minimum load resistance is $R_{Lmim} = V_O/I_{ON} = 1\ \Omega$. Assuming a diode duty cycle D = 0.5, the normalized load resistance resulting from the plot of Fig. 5 is $R_L/\omega L$ = 1.57. Therefore, the two inductors L_1 and L_2 have an inductance of $L = R_L/1.57\omega = 1/1.57 \text{x} 2\pi\ 500 \text{x} 10^3 = 200$ nH.

From Figs. 5 and 6 the maximum diode currents and voltages are $I_{DM} = 1.78\ I_O = 21.3$ A, and $V_{DM} = 2.86\ V_O = 35$ V, respectively. The converter dc voltage transfer function must be $M_{Vdc} = V_O/V_{Imin} = 12/200 = 0.06$. The class D series resonant inverter voltage transfer functions is given in [14]. Assuming an inverter efficiency η_I = 90%, a loaded quality factor Q_L = 5, and an inverter operating frequency $f = 1.05\ f_O$, where f_O is the resonance frequency of the inverter LC circuit, the dc–to–ac inverter voltage transfer function is calculated as

$$M_I = \frac{\sqrt{2}\eta_I}{\pi\sqrt{1+Q_L^2\left(\frac{f}{f_O}-\frac{f_O}{f}\right)^2}} = \frac{\sqrt{2}\text{x}0.9}{\pi\sqrt{1+25\left(1.05-1.05^{-1}\right)^2}} = 0.37. \quad (10)$$

The rectifier ac–to–dc transfer function is $M_R \equiv V_O/V_{Rin} = M_{Vdc}/M_I = 0.06/0.37 = 0.16$. As shown in Fig. 9, the voltage across the equivalent resistance of the rectifier seen at the terminals of the transformer primary side is V_{Rin}/nV_O = 0.68 for $R_L/\omega L$ = 1.57. The transformer turns ratio is calculated as $n = (0.16\text{x}0.68)^{-1} = 10$. As shown in Fig. 10 the normalized input resistance of the rectifier is $R_i/n^2R_L = 0.234$, and, therefore, the input resistance is $R_i = 10^2\text{x}1\text{x}0.234 = 23.4\ \Omega$. Assuming a resonance frequency of f_O = 600 kHz for the inverter, the inductance and capacitance of the resonant circuit are calculated as $L_R = Q_L R_i/2\pi f_O = 5\text{x}23.4/2\pi\text{x}600\text{x}10^3 = 31$ µH and $C_R = 1/(2\pi f_O)^2 L_R = 1/(2\pi\text{x}600\text{x}10^3)^2\ 31\text{x}10^{-6} = 2.2$ nF.

V. Experimental Results

The dc–to–dc converter assembled with a class–D series resonant dc–ac inverter and an inverting hybridge rectifier was frequency–controlled in the 600–to–950 kHz range. Two International Rectifier IRF740 MOSFETs where used in the inverter. A Philips 2.2 nF/250 V polyester capacitor was used as a resonant capacitor. The resonant inductor was assembled by winding 60 turns of a 90x0.1 Litz wire on an Amidon iron–powder Mix #2 T–94 toroidal core. A quality factor Q = 200 was measured for the resonant inductor at an operating frequency varying from 500 to 700 kHz. The transformer was built on a ETD29 Siemens N87 ferrite core. The primary was wound with 24 turns of 60 x 0.1 mm LITZ wire and the secondary winding with 2 turns of copper strips 15 x 0.15 mm. A Motorola 30CT45 Schottky diode was used for the rectifier. The filter inductances $L_1 = L_2 = 0.2$ µH were assembled by using two Amidon T50 iron–powder Mix #2 toroidal cores. One electrolytic Oscon 100 µF capacitor was used as filter capacitors. The operation at the minimum frequency is achieved for the minimum input voltage V_I = 200 V and the maximum load I_O = 12 A and the converter is operated at the maximum frequency when the input voltage is V_{Imax} = 380 V and output current I_O = 1.2 A. Fig. 12 shows the experimental waveforms of the voltage and current of the inverter lower MOSFET M_2. Since the inverter is operated above the resonant frequency, the current lags the voltage and is negative at the MOSFET turn–on.

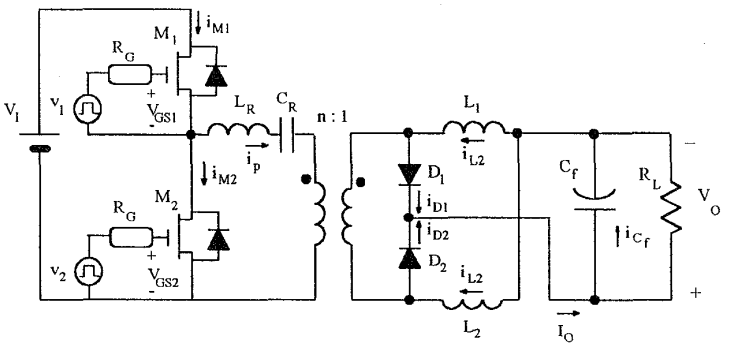


Fig. 11. Schematic circuit of the dc–dc converter constituted by a class D series resonant inverter and an inverting hybridge rectifier.

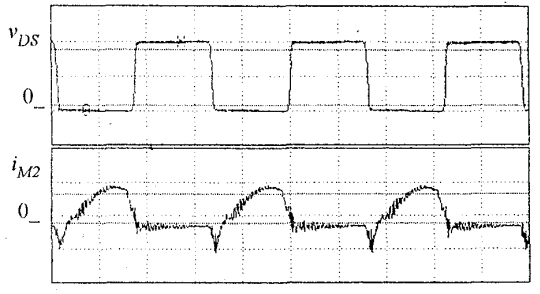


Fig. 12. Waveforms of MOSFET M_2 drain to source voltage v_{DS} and source current i_{M2} at an operating frequency of f = 615 kHz, dc input voltage V_I = 200 V, output voltage V_O = 12 V, and I_O = 12 A. Vertical: upper trace 100V/div.; lower trace 2 A/div., horizontal: 500 ns/div..

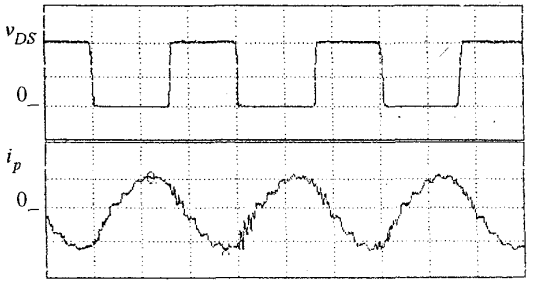


Fig. 13. Waveforms of MOSFET M_1 drain to source voltage v_{DS} and transformer primary side current i_p at an operating frequency of f = 660 kHz, dc input voltage V_I = 250 V, output voltage V_O = 12 V, and I_O = 12 A. Vertical: upper trace 125 V/div.; lower trace 2.5 A/div., horizontal: 500 ns/div..

Therefore, the current flows through the MOSFET parasitic diode which clamps the drain–to–source voltage at a low value, e.g., 0.5 V. This allows for a nearly zero–loss turn–on of the inverter MOSFETs.

The transformer primary side current waveform shown in Fig. 13 is nearly sinusoidal. This demonstrates that the class D series resonant inverter is operated as a sinusoidal current source also at low loaded quality factors. The waveforms of the voltage v_p across the terminals of the transformer primary winding and the current through MOSFET M_2 are shown in Fig. 14. The parasitic oscillation of the experimantal waveform v_p was caused by the transformer leakage inductance which resonates with the diode parasitic capacitances.

The waveforms of the output voltage ripple v_{oac} and the ac component of current i_{L1ac} through inductor L_1 are shown in Fig. 15. Current i_{L1ac} was observed with a passive current probe was nearly the same as the theoretically predicted current shifted downwards by the inductor dc component $I_{L1dc} = I_O/2 = 6$ A. Since the measured maximum ac current was $i_{L1ac} = 8$ A, the inductor maximum currents through the inductors were $I_{LM} = 14$ A.

A plot of the dc–to–dc converter efficiency versus the ac input voltage measured at an output current I_O = 12.5 A and an output voltage V_O = 12 V is depicted in Fig. 15(a). The efficiency was higher than 84% over the entire voltage range and reached a maximum of 88.5%. A plot of the measured efficiency as a function of I_O at a dc input voltage V_I = 310 V and an output voltage V_O = 12 V is shown in Fig. 15 (b). An efficiency η = 90 % was at full load. and the efficiency was higher than 80% for a dc output current varying from 2.3 A to 12 A, which corresponds to a load in the 30% to 100% range.

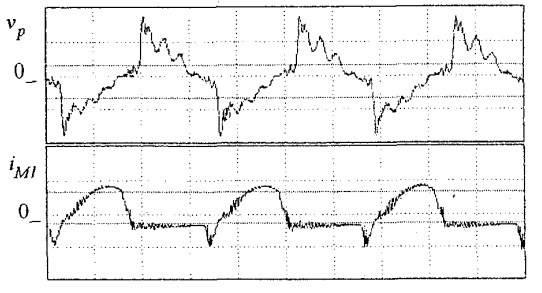


Fig. 14. Waveforms of the transformer primary side voltage v_p and MOSFET M_1 source current i_{M1} at an operating frequency of f = 615 kHz, dc input voltage V_I = 200 V, output voltage V_O = 12 V, and I_O = 12 A. Vertical: upper trace 100 V/div.; lower trace 2 A/div., horizontal: 500 ns/div..

IV. Conclusions

A circuit of a hybridge zero *di/dt* low *dv/dt* rectifier has been introduced. The equations describing the circuit operation been presented and verified experimentally. This rectifier preserves major advantages of conventional bridge and center–tapped rectifiers and overcomes many limitations of these circuits. Conduction losses are reduced because the average current through each diode and inductor is one–half of the output dc current as in center–tapped rectifiers.

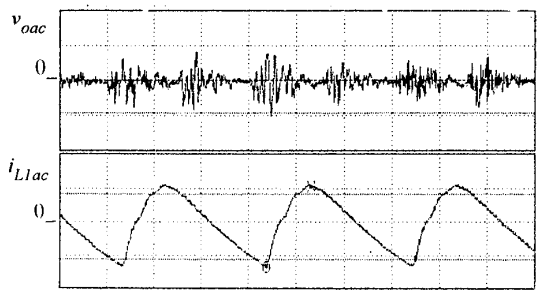


Fig. 15. Waveforms of output voltage ripple v_{oac} and ac component i_{L1ac} of the current through inductor L_1 at an operating frequency of f = 660 kHz, dc input voltage V_I = 250 V, output voltage V_O = 12 V, and I_O = 12 A. Vertical: upper trace 50 mV/div.; lower trace 8 A/div., horizontal: 500 ns/div..

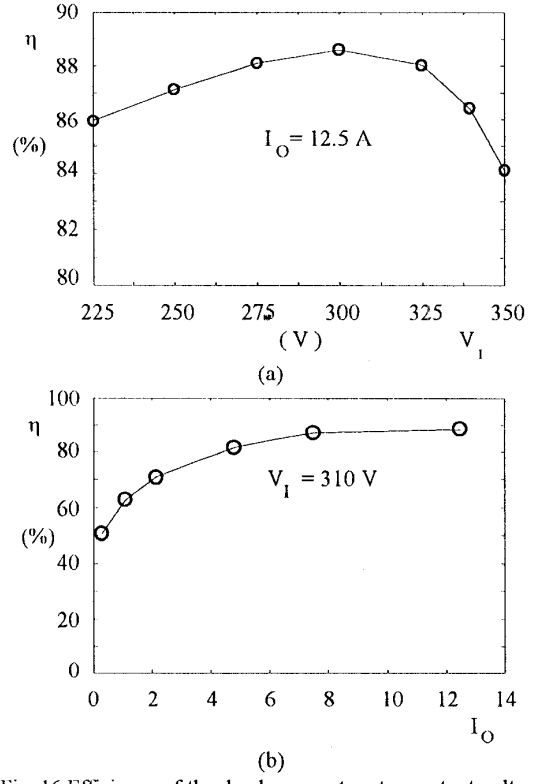


Fig. 16 Efficiency of the dc–dc converter at an output voltage V_O = 12 V. (a) Efficiency versus input voltage V_I. (b) Efficiency versus output current I_O.

A full–wave rectification is achieved with two diodes and a transformer with only one secondary winding. The diode current and voltage waveforms do not overlap at diode transitions and the diodes turn on at zero voltage and zero current with zero *di/dt* and limited *dv/dt* and turn off with a limited *di/dt*. As a result, switching losses and noise level are drastically reduced in the current–driven circuit. The feasible high–frequency operation of the hybridge rectifier is possible allows for small capacitances and inductances to be used. Finally, the current–driven hybridge ZCS low *di/dt* full–wave rectifier is compatible with high–frequency inverters as class D and class E series resonant inverters in assembling dc–dc converters.

A possible limitation of the current–driven hybridge rectifier is the high number of wound components. This does not significantly affect the overall volume and weight of the rectifier but contributes to the cost increase of the rectifier. However, if the two inductors are integrated onto one core this problem is overcome and the overall size of the integrated inductors is lower than in a center–tapped current–driven rectifier. Therefore, as a future work, it is recommended to evaluate the feasibility of a hybridge rectifier with the two inductor and the transformer integrated onto only one core. Moreover, the use of power MOSFETs with low–on–resistance could improve the rectifier efficiency.

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