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Analysis and Design of a Current-Driven Two-Inductor ZCS Low di_D/dt Full-Wave Rectifier

Alberto Reatti, *Member, IEEE*

Abstract— An analysis and experimental verification of a current-driven two-inductor zero-current-switching (ZCS) low di_D/dt full-wave rectifier are given. The design equations are derived using the time-domain analysis and Fourier series technique. The rectifier operates as a full-wave rectifier with two diodes and a one-secondary winding transformer overcoming the limitations of class D current-driven full-bridge and center-tapped rectifiers and preserving their advantages. The rectifier operates with lower conduction losses than the center tapped rectifier. Moreover, the diodes turn on at zero di_D/dt , low dv_D/dt , and turn off at low di_D/dt . As a consequence, switching losses are reduced and this rectifier is suitable for a high-frequency and high-efficiency operation. Integrated inductors can be used to reduce the size, volume, and cost of the circuit. A breadboard of the rectifier was designed and tested for a constant output voltage $V_O = 12$ V, and an output current I_O ranging from no-load to 12 A. The rectifier was driven by an off-line ac-ac converter operated at an input rms voltage varying from 176–270 V and a minimum frequency of 550 kHz. The predicted results are in good agreement with those measured. A full-load efficiency of 89.4% was achieved for the entire ac-dc converter.

I. INTRODUCTION

THE INCREASING demand of high-power density dc-dc converters has necessitated the development of new converter topologies which can be operated at high-frequencies with high efficiencies. This can be achieved if switching losses are removed or drastically reduced. Some inverter topologies allow for nearly zero-losses transitions of the switches, e.g., class E and class D resonant inverters and can be operated with very high efficiencies, e.g., $\eta = 96\%$ as high-frequency dc-ac inverters [1]–[13]. These inverters have also been used as sinusoidal current and voltage sources driving class D and class E rectifiers to assemble high-frequency dc-dc converters [11]–[25]. The overall efficiency of a dc-dc converter highly depends on the rectifier circuit (including the transformer coupling the inverter and the rectifier) [19]–[22] and is mostly affected by conduction and switching losses of the diodes. If class E rectifiers are used [15]–[25], switching losses are reduced because the diodes turn on with low dv_D/dt and turn off at zero current with low dv_D/dt and limited di_D/dt . Both class D and class E bridge rectifiers provide a full-wave rectification and require a simple transformer with only one secondary winding. However, two diodes are simultaneously

ON during each half-period. This results in high power losses at a high-output current operation. Moreover, voltage drops on the diodes makes the full-bridge rectifiers unusable for low-output voltage applications. Diode conduction losses are reduced using class D and class E center-tapped rectifiers. However, the transformers in these circuits have two secondary windings which are not efficiently used because the current flows in each secondary winding only for one-half of the switching period. The class E full-wave rectifier [19]–[22] is another rectifier circuit which can be operated at high frequencies but requires two transformers with both the primary and the secondary windings connected in series and, therefore, results in a higher number of components and increased cost than other rectifier circuits.

The purpose of this paper is to present an analysis and experimental results for a current-driven two-inductor ZCS low di_D/dt rectifier shown in Fig. 1(a). This circuit operates as a full-wave rectifier with nearly zero switching losses. Therefore, its operating frequency is not limited in the range of tens of kilohertz such as in PWM source driven two-inductor rectifiers [26]–[32]. Moreover, conduction losses and output ripple are lower than in the half-wave class E zero-current switching rectifier [22]–[25]. As a result, the current-driven two-inductor rectifier can be operated at hundreds of kilohertz and is suitable for high-power density applications.

Other advantages of the current-driven two-inductor ZCS low di_D/dt rectifier are as follows:

- The flux density in the transformer is sinusoidal with no dc component, resulting in a full utilization of the core hysteresis loop and in a size reduction of the transformer core.
- A transformer with only one secondary winding is needed. Because of this, a larger winding area than in a center-tapped rectifier with the same turns ratio is available in the transformer of the two-inductor rectifier. Therefore, strand and Litz wire winding can be used also on small core transformers. This allows for a significant reduction of the winding parasitic resistances at high operating frequencies. Moreover, the primary and secondary side currents are sinusoidal and only the winding ac resistance calculated at the rectifier operating frequency contributes to the power loss in the windings.
- The transformer leakage inductance is lower than in center-tapped rectifiers, and the asymmetrical operations due to the different flux linkage are prevented.
- A high-frequency operation of the rectifier allows the

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standard requirements on output voltage ripple to be satisfied by using small-volume inductors and capacitors.

- The rectifier operates as an impedance inverter and, therefore, is suitable for applications with class E and class D series resonant inverters.

The rectifier description and principle of operation are given in Section II. Section III contains the time-domain analysis and equations for the rectifier steady-state operation. Section IV shows a design example and experimental verifications of a current-driven two-inductor rectifier operated at an output power $P_O = 144$ W and an output voltage $V_O = 12$ V regulated over the entire line voltage range and from no-load to full load. An off-line bridge rectifier with a filter capacitor and a class D series resonant inverter operated at a minimum switching frequency of 550 kHz and at a dc voltage ranging from 240–315 V were used as a current source for the rectifier. A maximum efficiency $\eta = 89.4\%$ was achieved at full load for the entire ac–dc converter. It is shown in Section V that the two rectifier inductors can be integrated onto one core to reduce the circuit volume, and cost.

II. OPERATION OF THE RECTIFIER

A schematic circuit of the current-driven two-inductor ZCS low di_D/dt full-wave rectifier is shown in Fig. 1(a). The rectifier is driven by an ideal sinusoidal current source with

$$i = I_m \sin \omega t \quad (1)$$

where I_m is the current amplitude, $\omega = 2\pi f$ is the current angular frequency, and f is the rectifier operating frequency. The rectifier consists of a single secondary winding transformer with a turns ratio n , two diodes D_1 and D_2 , two inductors L_1 and L_2 , and a filter capacitor C_f . Resistor R_L is the dc load resistance. An equivalent circuit of the rectifier is shown in Fig. 1(b). The transformer magnetizing and leakage inductances, the core and winding equivalent resistances as well as the layer-layer, winding-to-core, and primary-to-secondary stray capacitances are neglected. The equivalent series resistance (ESR) of capacitor C_f is also neglected and the capacitance of C_f is assumed to be large enough so that output voltage V_O is ripple free.

Fig. 2(a)–(d) and (e)–(h) shows the four topological modes the rectifier circuit goes through during one switching period when operated at a diode on duty cycle D in the range $0 \leq D < 0.5$ and $0.5 \leq D < 1$, respectively. The steady-state operation voltage and current waveforms for $0 \leq D < 0.5$ and $0.5 \leq D < 1$ are depicted in Fig. 3(a) and (b), respectively.

In the two-inductor rectifier, the single output inductance of a center-tapped rectifier is replaced by two separate inductances. This involves a cost penalty but does not significantly affect the size of the circuit because the total energy storage of inductances L_1 and L_2 is nearly the same as in the single inductor of a center-tapped rectifier. Moreover, this circuit can be operated at high frequencies and the inductor and capacitor volumes are reduced.

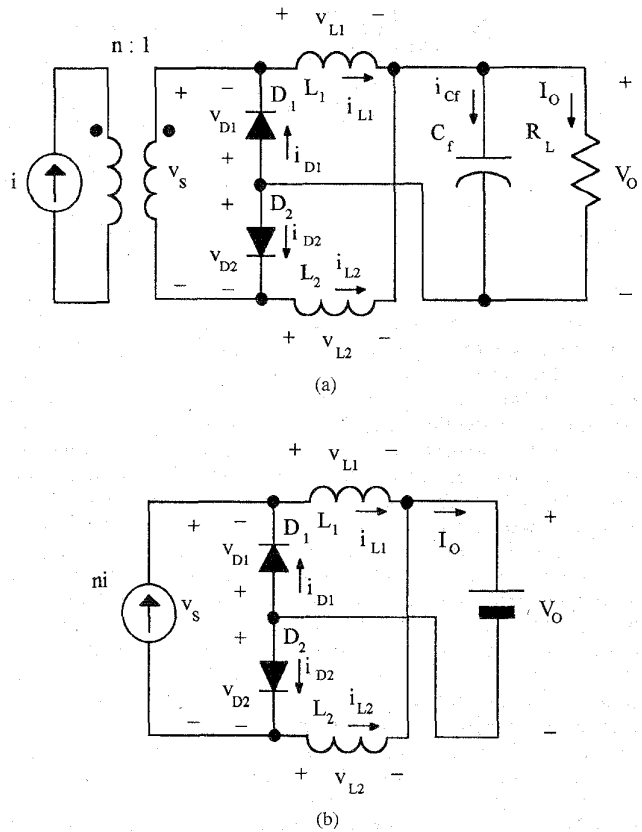


Fig. 1. Two-inductor ZCS low di_D/dt full-wave rectifier. (a) Schematic circuit. (b) Equivalent circuit.

A. Operation at $0 \leq D < 0.5$

The first topological mode begins at $\omega t = \phi$ when voltage v_{D1} becomes zero. During this interval D_1 is ON and D_2 is OFF, the current through L_2 is $i_{L2} = -ni$, the voltage across L_1 is $v_{L1} = -V_O$, and the current through L_1 decreases linearly with a slope $-V_O/L_1$ and an initial value $i(\phi) = nI_m \sin \phi$. Diode D_1 current is $i_{D1} = i_{L1} - ni$, increases starting from zero, reaches its maximum value, and then decreases to zero. Current i_{L1} is that of the transformer secondary side before diode D_1 turn on and $di_{L1}/dt = dni/dt$ at $\omega t = \phi$. As a result, we have $di_{D1}/dt = 0$ a low dv_{D1}/dt when D_1 turns on. The voltage across D_2 is $v_{D2} = -v_{L2} - V_O = -n\omega L_2 I_m \cos \omega t - V_O$ and reaches its maximum absolute value V_{DM} during this interval. This mode ends at $\omega t = \phi + 2\pi D$ when i_{D1} becomes zero and D_1 turns off.

The second topological mode begins at $\omega t = \phi + 2\pi D$. Both D_1 and D_2 are OFF during this interval, the transformer secondary side current flows through L_1 and L_2 and $i_{L1} = -i_{L2} = ni$. Therefore, the current through L_2 is still sinusoidal and inductor L_1 voltage is $v_{L1} = n\omega L_1 I_m \cos \omega t$. The reverse voltages across D_1 and D_2 are $v_{D1} = V_O + v_{L1}$ and $v_{D2} = V_O + v_{L2}$, respectively. Voltage v_{D1} abruptly increases from 0 to a finite value at the beginning of the second topological mode. However, diode current has a limited di_D/dt at diode D_1 turn off. Voltage v_{D2} still decreases and becomes zero at $\omega t = \phi + \pi$ ending the second topological mode.

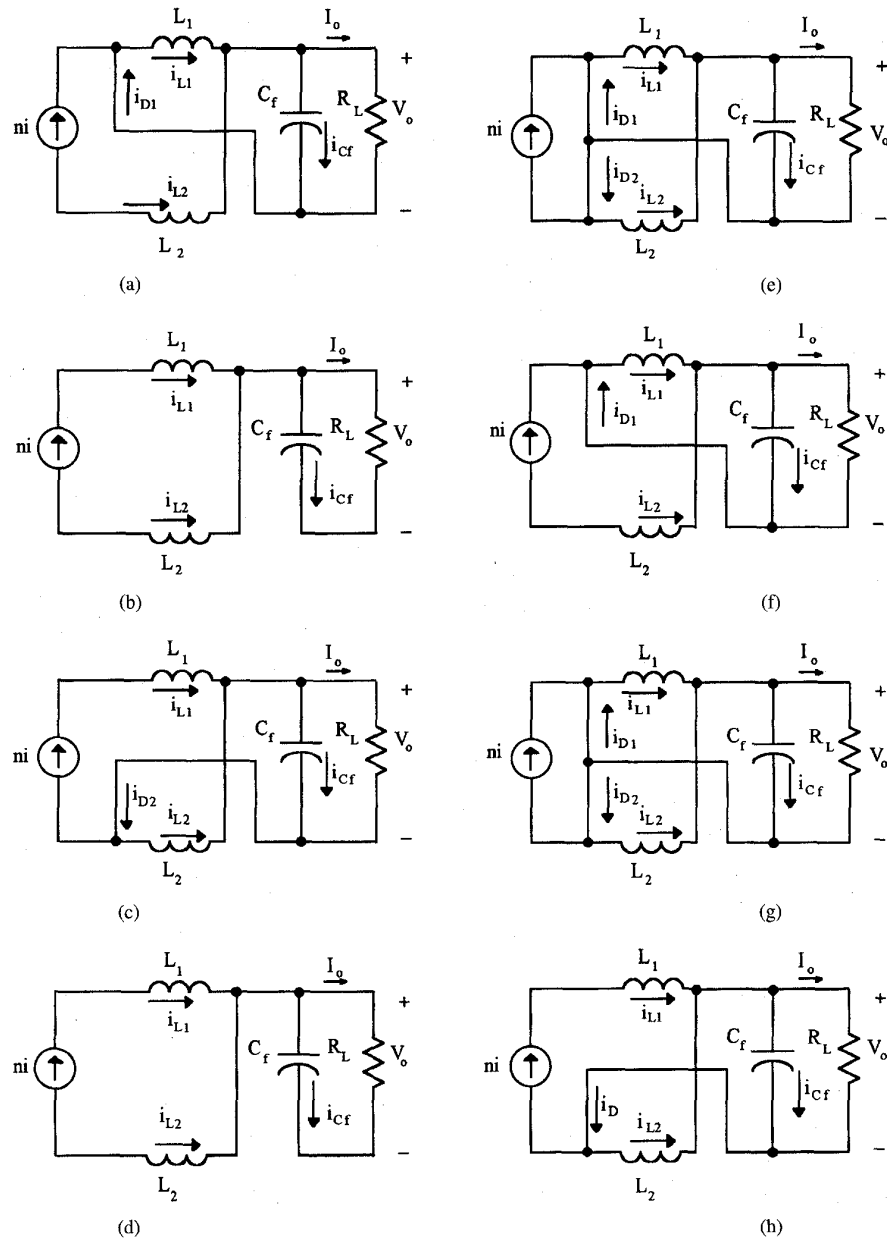


Fig. 2. Equivalent circuits of the two-inductor ZCS low di_D/dt full-wave rectifier for various intervals. (I) Operation at $0 \leq D < 0.5$. (a) D_1 ON and D_2 OFF. (b) D_1 OFF and D_2 OFF. (c) D_1 OFF and D_2 ON. (d) D_1 OFF and D_2 OFF. (II) Operation at $0.5 \leq D < 1$: (e) D_1 ON and D_2 ON. (f) D_1 ON and D_2 OFF. (g) D_1 ON and D_2 ON. (h) D_1 OFF and D_2 ON.

The third topological mode begins at $\omega t = \phi + \pi$ when diode D_2 turns on. The voltage across L_2 is $v_{L2} = -V_O$, that is, the same value assumed by v_{L1} during the first topological mode. The current through L_2 linearly decreases with a negative slope $-V_O/L_2$ starting from $nI_m \sin \phi$. The current through D_2 is $i_{D2} = i_{L2} - ni$ and i_{L2} and i_{D2} are shaped as i_{L1} and i_{D1} during the first topological mode. Voltage $v_{D1} = v_{L1} + V_O$ reaches its maximum value V_{DM} during this interval and then decreases. Current i_{D2} reaches zero at $\omega t = \phi + 2\pi D + \pi$, D_2 turns off, and the third topological mode ends.

The fourth topological mode begins at $\omega t = \phi + 2\pi D + \pi$. As in the second topological mode, inductor currents are

$i_{L1} = -i_{L2} = ni$, both diodes D_1 and D_2 are OFF, v_{D2} is shaped as v_{D1} during the second topological mode. Voltage v_{D1} decreases to zero at $\omega t = \phi + 2\pi$ ending the fourth topological mode and the switching period.

B. Operation at $0.5 \leq D < 1$

As for the operation at $0 \leq D < 0.5$, the first topological mode begins with diode D_1 turn-on at $\omega t = \phi$ with $di_{D1}/dt = 0$. During the first topological mode current $i_{D1} = i_{L1} - ni$ increases, the transformer secondary voltage is $v_S = 0$ because both D_1 and D_2 are ON, inductance voltages are $v_{L1} = v_{L2} = -V_O$, and both i_{L1} and i_{L2} linearly decrease with a slope

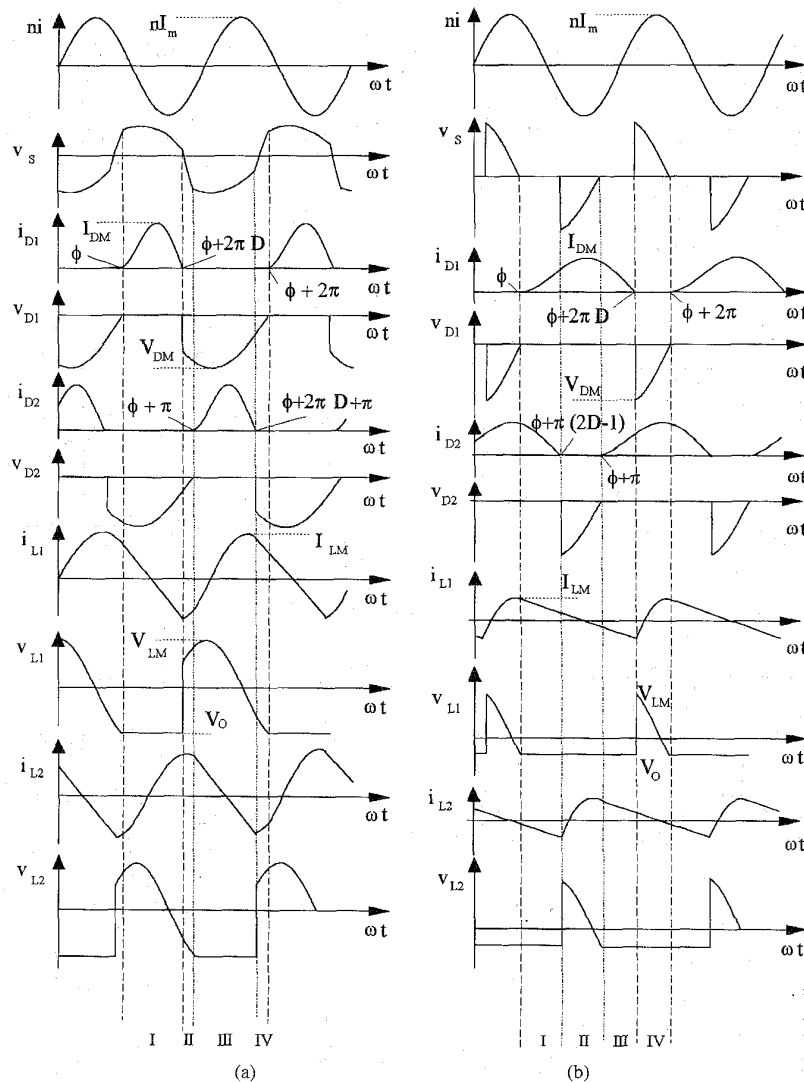


Fig. 3. Voltage and current waveforms in the two-inductor ZCS low di_D/dt full-wave rectifier. (a) For $0 \leq D < 0.5$. (b) For $0.5 \leq D < 1$.

given by $-V_O/L$. Current i_{D2} decreases and reaches zero at $\omega t = \phi + \pi(2D - 1)$ ending the first mode.

The second topological mode begins with diode D_2 turn-off. Current i_{D1} increases, reaches its maximum value I_{DM} during this interval, and then decreases. Current i_{L1} continues to linearly decrease because L_1 voltage is still $v_{L1} = -V_O$. Since D_2 is OFF, we have $i_{L2} = -ni$. Voltage v_{D2} abruptly increases from zero to its maximum absolute value V_{DM} at the beginning of this interval and then decreases according to $v_{D2} = -V_O - v_{L2} = V_O - nI_m\omega L_2 \cos \omega t$. Voltage v_{D2} becomes zero at $\omega t = \phi + \pi$, and the second topological mode ends.

At $\omega t = \phi + \pi$, diode D_2 turns on at zero di_{D2}/dt and the third topological mode begins. The current through D_2 is $i_{D2} = i_{L2} + ni$ and increases starting from zero. Both D_1 and D_2 are ON and L_1 and L_2 voltages and currents are the same as in the first interval. Diode D_1 current is $i_{D1} = i_{L1} - ni$ and becomes zero at $\omega t = \phi + 2\pi D$, turning off D_1 and ending the third topological mode.

The fourth topological mode begins when D_1 turns off. Since D_1 is OFF and D_2 is ON, i_{D2} continues to increase and reaches its maximum value I_{DM} , i_{L2} continues to decrease linearly with a slope given by $-V_O/L_2$. Inductor L_1 current is $i_{L1} = ni$ and increases with a sinusoidal waveform as i_{L2} in the second interval. Voltage v_{D1} reaches its maximum absolute value when D_1 turns off, then decreases to zero at $\omega t = \phi + 2\pi$ ending this topological mode and the switching period.

As shown by Fig. 3, for both the operations at $0 \leq D < 0.5$ and $0.5 \leq D < 1$ the current and voltage waveforms of diode D_2 are equal of those of diode D_1 with a delay angle 180° . Also the inductor current and voltage waveforms are equal and 180° out of phase. This demonstrates the symmetrical operation of the rectifier circuit. Center-tapped rectifiers can result in asymmetrical operation because the two secondary windings of an actual transformer are not perfectly coupled with the primary winding and the two secondary windings have two different leakage fluxes. This problem is prevented in the current-driven two-inductor ZCS low di_D/dt full-

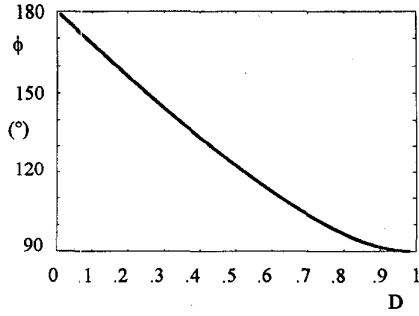


Fig. 4. Diode D_1 turn-on delay angle ϕ as a function of the diode ON duty-cycle D .

wave rectifier because the transformer has only one secondary winding. Since the diodes turn on at zero voltage with a limited dv_D/dt and $di_D/dt = 0$ and turn off at a limited di_D/dt , the waveforms of current and voltage of each diode do not overlap at diode transitions and switching losses are drastically reduced.

Combination of the two rectifier inductances L_1 and L_2 and filter capacitor C_f allows the rectifier output section to operate as a second order filter and, therefore, the ac output voltage ripple can be easily limited within standard requirements for dc-dc converters and power supplies.

III. ANALYSIS

The analysis of the two-inductor rectifier of Fig. 1 is carried out under the following assumptions:

- the transformer is assumed to be ideal, that is, the winding resistances, the core resistance, the leakage inductance, and the parasitic capacitances are neglected. Moreover, the magnetizing inductance is assumed to be large enough so that no energy is stored in the transformer;
- diodes D_1 and D_2 are ideal, e.g., they are assumed to be short circuits when ON and open circuits when OFF;
- the equivalent series resistance (ESR) of filter capacitor C_f is assumed to be zero and its capacitance large enough to neglect the output voltage ripple;
- the rectifier has a symmetrical behavior. Therefore, it is assumed that $L_1 = L_2 = L$.

The derivations are included in the Appendix and only final results are given in this section. The diode D_1 turn-on delay angle is

$$\tan \phi = \frac{\sin 2\pi D - 2\pi D}{1 - \cos 2\pi D}. \quad (2)$$

Because of the rectifier symmetrical behavior the on-duty cycle and turn-on delay angle of diode D_2 are D and $\phi + \pi$, respectively. Fig. 4 shows a plot of ϕ as a function of D . Phase ϕ decreases from 180 to 90° when D rises from 0 to 1.

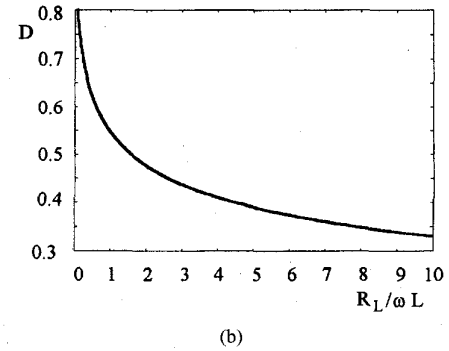
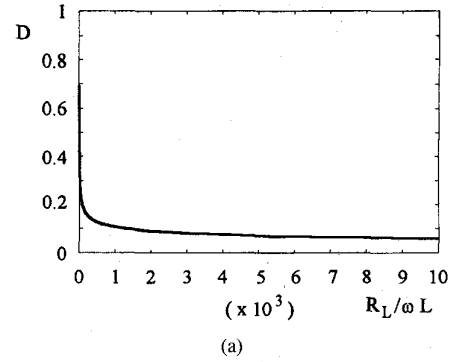


Fig. 5. Diode ON duty cycle D as a function of the normalized load resistance $R_L/\omega L$. (a) D versus $R_L/\omega L$ over the entire range of D . (b) Detail of Fig. 5(a).

The load resistance R_L normalized with respect to the impedance ωL of each inductor as a function of the diode duty cycle D is given in (3) (see the bottom of this page). Fig. 5(a) shows a plot of D as a function of $R_L/\omega L$ over the entire range of D . A zoom of this plot is depicted in Fig. 5(b) and shows that D decreases from 0.55 to 0.33 when $R_L/\omega L$ increases from 1 to 10. This means that the rectifier can be operated at a limited range of D over a wide range of load.

The amplitude of the sinusoidal primary side current is expressed as

$$\begin{aligned} I_m &= -\frac{I_O R_L}{n\omega L \cos \phi} \\ &= -\frac{V_O}{n\omega L \cos \phi} \end{aligned} \quad (4)$$

and the current through inductors L_1 and L_2 is given by

$$i_{L_1} = \frac{I_O R_L}{\omega L} \begin{cases} -\omega t + \phi + \tan \phi & \text{for } \phi \leq \omega t < \phi + 2\pi D \\ \frac{\sin \omega t}{\cos \phi} & \text{for } \phi + 2\pi D \leq \omega t < \phi + 2\pi \end{cases} \quad (5)$$

and

$$\frac{R_L}{\omega L} = \frac{\pi(1 - \cos 2\pi D)}{(1 - \cos 2\pi D)^2 + (\sin 2\pi D - 2\pi D)^2 - 2\pi^2 D^2(1 - \cos 2\pi D)}. \quad (3)$$

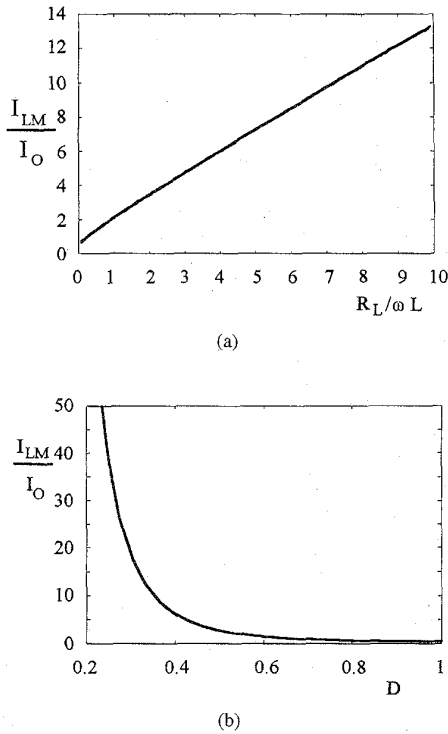


Fig. 6. Normalized peak values of inductor current I_{LM}/I_O as a function of $R_L/\omega L$ and D . (a) I_{LM}/I_O versus $R_L/\omega L$ (b) I_{LM}/I_O versus D .

$$i_{L2} = \frac{I_O R_L}{\omega L} \begin{cases} \frac{\sin \omega t}{\cos \phi} & \text{for } \phi \leq \omega t < \phi + \pi \\ -\omega t + \phi + \tan \phi & \text{for } \phi + \pi \leq \omega t < \phi + \pi + 2\pi D \\ \frac{\sin \omega t}{\cos \phi} & \text{for } \phi + \pi + 2\pi D \leq \omega t < \phi + 2\pi \end{cases} \quad (6)$$

respectively. Since ϕ is greater than 90° , the maximum current through the inductances I_{LM} is given by the amplitude of the secondary side current nI_m . Combination of (3) and (4) yields (7) (see below). Fig. 6(a) and (b) shows the plots of the inductor maximum current normalized with respect of the dc output current I_{LM}/I_O as functions of $R_L/\omega L$ and

D , respectively. The currents through the two inductances decrease as the load resistance is reduced. As a consequence, the rectifier is operated at a low normalized inductor current at high loads and the full-load efficiency of the rectifier circuit is increased. The currents through the rectifier diodes D_1 and D_2 are

$$i_{D1} = \frac{I_O R_L}{\omega L} \begin{cases} -[\omega t - \phi + \pi] + \tan \phi \\ -\frac{\sin \omega t}{\cos \phi} & \text{for } \phi \leq \omega t < \phi + 2\pi D \\ 0 & \text{for } \phi + 2\pi D \leq \omega t < \phi + 2\pi \end{cases} \quad (8)$$

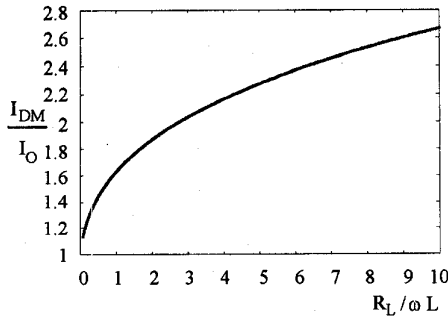
and

$$i_{D2} = \frac{I_O R_L}{\omega L} \begin{cases} 0 & \text{for } \phi \leq \omega t < \phi + \pi \\ -[\omega t - \phi + \pi] + \tan \phi - \frac{\sin \omega t}{\cos \phi} & \text{for } \phi + \pi \leq \omega t < \phi + \pi + 2\pi D \\ 0 & \text{for } \phi + \pi + 2\pi D \leq \omega t < \phi + 2\pi \end{cases} \quad (9)$$

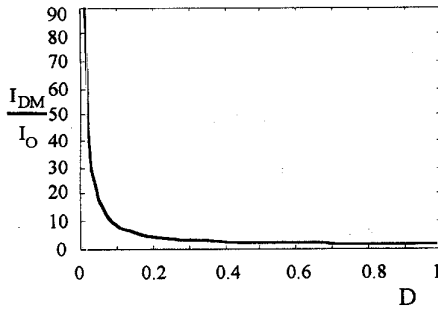
respectively. The current through diode D_1 reaches its maximum value at $\omega t = 2\pi - \phi$ and the current through D_2 at $\omega t = 3\pi - \phi$. As an example, the delay angle is $\phi = 127^\circ$ at $D = 0.45$, diode D_1 is ON during the interval $127^\circ \leq \omega t < 289^\circ$, the maximum of i_{D1} occurs at $\omega t = 233^\circ$, diode D_2 is ON during the interval $307^\circ \leq \omega t < 469^\circ$, and the maximum of i_{D2} occurs at $\omega t = 413^\circ$. Substitution of $\omega t = 2\pi - \phi$ into (8) and combination of this with (2) and (3) yields the following expression for the maximum diode current I_{DM} normalized with respect to the dc output current I_O shown in (10) (see the bottom of this page). The plots of I_{DM}/I_O as a function of $R_L/\omega L$ and D are shown in Fig. 7(a) and (b), respectively. The diode normalized maximum current decreases when the load resistance decreases, that is, when the output current I_O increases, and ranges in a smaller interval than the inductor current. Fig. 7(b) shows that the current through the diodes becomes more and more impulsive when D decreases.

$$\frac{I_{LM}}{I_O} = -\frac{1}{\cos \phi} \frac{\pi(1 - \cos 2\pi D)}{(1 - \cos 2\pi D)^2 + (\sin 2\pi D - 2\pi D)^2 - 2\pi^2 D^2(1 - \cos 2\pi D)} \quad (7)$$

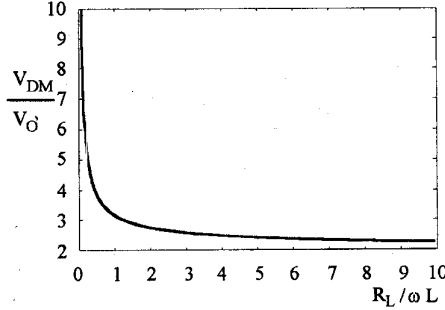
$$\frac{I_{DM}}{I_O} = -2 \frac{R_L}{\omega L} (\pi - \phi + \tan \phi) \frac{2\pi[(\phi - \pi)(1 - \cos 2\pi D) - \sin 2\pi D + 2\pi D]}{(1 - \cos 2\pi D)^2 + (\sin 2\pi D - 2\pi D)^2 - 2\pi^2 D^2(1 - \cos 2\pi D)} \quad (10)$$



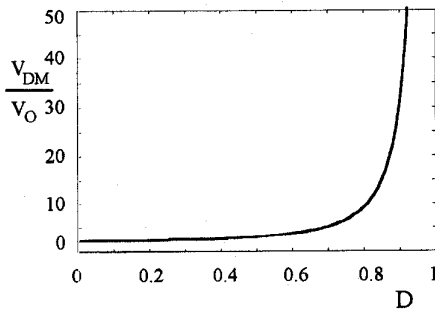
(a)



(b)

 Fig. 7. Normalized peak values of diode current I_{DM}/I_O as functions of $R_L/\omega L$ and D . (a) I_{DM}/I_O versus $R_L/\omega L$. (b) I_{DM}/I_O versus D .


(a)

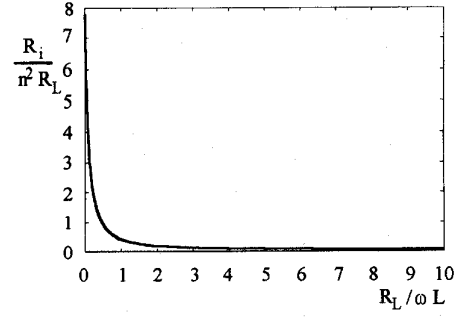


(b)

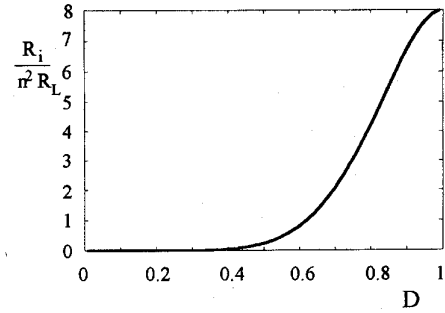
 Fig. 8. Normalized peak values of diode voltage V_{DM}/V_O as functions of $R_L/\omega L$ and D . (a) V_{DM}/V_O versus $R_L/\omega L$. (b) V_{DM}/V_O versus D .

The instantaneous voltages across the diodes D_1 and D_2 are given by

$$v_{D_1} = V_O$$



(a)



(b)

 Fig. 9. Normalized values of input resistance $R_i/n^2 R_L$ as functions of $R_L/\omega L$ and D . (a) $R_i/n^2 R_L$ versus $R_L/\omega L$ and (b) $R_i/n^2 R_L$ versus D .

$$\begin{cases} 0 & \text{for } \phi \leq \omega t < \phi + 2\pi D \\ -1 + \frac{\cos \omega t}{\cos \phi} & \text{for } \phi + 2\pi D \leq \omega t < \phi + 2\pi \end{cases} \quad (11)$$

and

$$v_{D_2} = V_O \begin{cases} -1 + \frac{\cos \omega t}{\cos \phi} & \text{for } \phi \leq \omega t < \phi + \pi \\ 0 & \text{for } \phi + \pi \leq \omega t < \phi + \pi + 2\pi D \\ -1 + \frac{\cos \omega t}{\cos \phi} & \text{for } \phi + \pi + 2\pi D \leq \omega t < \phi + 2\pi \end{cases} \quad (12)$$

The maximum reverse voltage across diode D_1 occurs at $\omega t = \pi$. Substitution of this into (11) gives the diode maximum reverse voltage normalized with respect to the dc output voltage V_O as

$$\frac{V_{DM}}{V_O} = 1 - \frac{1}{\cos \phi} \quad (13)$$

Fig. 8(a) and (b) shows the plots of V_{DM}/V_O as functions of $R_L/\omega L$ and D , respectively. The maximum reverse voltage assumes high values when $R_L/\omega L$ tends to zero.

The equivalent input impedance of the rectifier circuit seen at the transformer primary side at the operating frequency is determined by deriving the expressions of the input voltage components in phase and 90° out of phase with respect to the input current $i = I_m \sin \omega t$. These components are

$$V_{Rim} = \frac{n^2 \omega L I_m}{\pi} \{ 2 \cos \phi [\cos \phi - \cos(\phi + 2\pi D)] \}$$

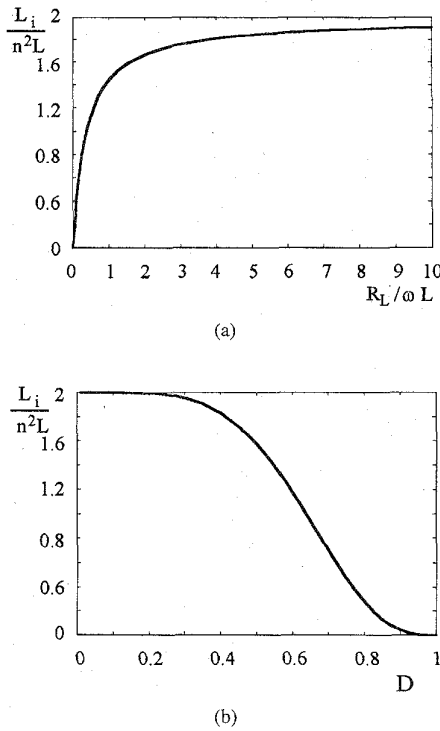


Fig. 10. Normalized values of input inductance L_I/n^2L as functions of $R_L/\omega L$ and D . (a) L_I/n^2L versus $R_L/\omega L$. (b) L_I/n^2L versus D .

$$+ \sin^2 \phi - \sin^2(\phi + 2\pi D)\} \quad (14)$$

and

$$V_{Xim} = \frac{n^2 \omega L I_m}{\pi} \{2 \cos \phi [\sin(\phi + 2\pi D) - \sin \phi] + 2\pi(1 - D) + \sin \phi \cos \phi - \sin(\phi + 2\pi D) \cos(\phi + 2\pi D)\} \quad (15)$$

respectively. Substitution of (4) and (14) into $R_I = V_{Rim}/I_m$ gives the rectifier input resistance at the transformer secondary side normalized with respect to the load resistance

$$\frac{R_I}{n^2 R_L} = \frac{\omega L}{\pi R_L} [1 - 3 \cos^2 \phi + 2 \cos \phi \cos(\phi + 2\pi D) - \sin^2(\phi + 2\pi D)]. \quad (16)$$

The plot of $R_I/n^2 R_L$ as a function of $R_L/\omega L$ is shown in Fig. 9(a). Since the normalized input resistance decreases as the load resistance increases, the rectifier operates as resistance inverter. Moreover, the input resistance remains nearly constant for a $R_L/\omega L \geq 2$. The plot of $R_I/n^2 R_L$

as a function of D of Fig. 9(b) shows that the input resistance is nearly constant for $0 \leq D \leq 0.5$.

By definition, the rectifier input reactance at the transformer primary side, calculated at the operating frequency is $X_I = \omega L_I = V_{Xim}/I_m$. Combination of this, (4) and (15) yields the rectifier input inductance (reactance) normalized with respect to inductance L (reactance $X_L = \omega L$) shown in (17) (see bottom of the page).

The plots of $L_I/n^2 L$ as functions of $R_L/\omega L$ and D are shown in Fig. 10(a) and (b), respectively. The normalized input inductance ranges from 0–2 for a normalized load resistance increasing from 0–10, and rises from 1.6–2 for $R_L/\omega L$ varying from 1–10.

The rectifier voltage transfer function is

$$H_V \equiv \frac{V_O}{V_{1 \text{ rms}}} = \frac{V_O \sqrt{2}}{\sqrt{V_{Rim}^2 + V_{Xim}^2}} \quad (18)$$

where $V_{1 \text{ rms}}$ is the rms value of the transformer primary side voltage. Combination of (4), (14), (15), and (18) gives the voltage transfer function normalized with respect to the transformer turns ratio

$$nH_V = \pi \sqrt{2} \cos \phi \{ [1 - 3 \cos^2 \phi + 2 \cos \phi \cos(\phi + 2\pi D) - \sin^2(\phi + 2\pi D)]^2 + \{ (2\pi - D) + 3 \cos \phi \sin \phi + \sin(\phi + 2\pi D)[2 \cos \phi + \cos(\phi + 2\pi D)] \}^2 \}^{-1/2} \quad (19)$$

which is plotted in Fig. 11(a) and (b) as a function of $R_L/\omega L$ and D , respectively. The voltage transfer function remains nearly constant for a normalized load resistance varying from 2–10.

By using (3) and (4), the rectifier current transfer function normalized with respect to n is expressed in (20) (shown at the bottom of the next page) where $I_{1 \text{ rms}} = I_m/\sqrt{2}$ is the rms value of the current through the transformer primary winding. Plots of H_i/n as functions of the normalized load resistance and duty cycle are shown in Fig. 12.

The expression of rectifier transconductance normalized with respect to the transformer turns ratio n and inductor reactance ωL is derived by using (4)

$$\omega L n G_R \equiv \frac{I_{1 \text{ rms}}}{V_O} = \frac{-1}{\sqrt{2} \cos \phi} \quad (21)$$

and is plotted in Fig. 13(a) and (b) versus $R_L/\omega L$ and D , respectively. The values of the rectifier design parameters are summed up in Table I.

$$\frac{X_I}{n^2 X_L} = \frac{L_I}{n^2 L} = \frac{2\pi(1 - D) + \cos \phi \sin \phi + \sin(\phi + 2\pi D)[2 \cos \phi - \cos(\phi + 2\pi D)]}{\pi} \quad (17)$$

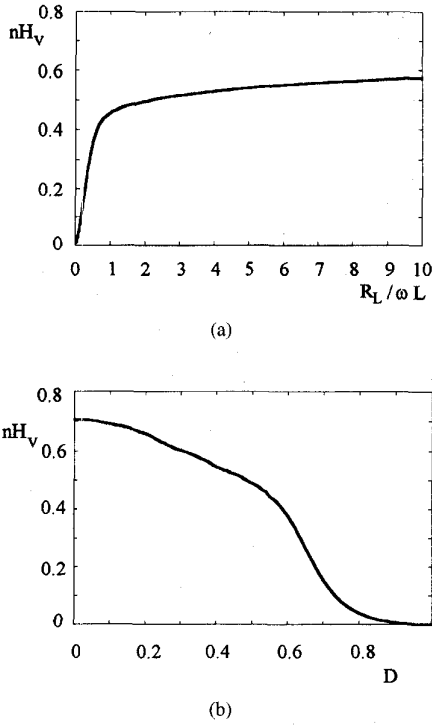


Fig. 11. Normalized values of voltage transfer function nH_V as functions of $R_L/\omega L$ and D . (a) nH_V versus $R_L/\omega L$. (b) nH_V versus D .

IV. DESIGN EXAMPLE AND EXPERIMENTAL VERIFICATION

A rectifier circuit with a maximum output power $P_{O \max} = 144$ W operated at a nominal switching frequency $f = 550$ kHz and an output voltage $V_O = 12$ V regulated over an output current ranging from 3–100% of the maximum value $I_{O \max}$ was designed and experimentally tested.

A. Design Example

The minimum dc load resistance and the maximum dc output current are $R_{L \min} = V_O^2/P_{O \max} = 144/144 = 1 \Omega$ and $I_{O \max} = P_{O \max}/V_O = 144/12 = 12$ A, respectively. In a rectifier operated at a frequency greater than 500 kHz, Schottky diodes are preferred to pn diodes. To achieve low conduction losses the diode forward voltage drop and current must be low. As shown in Table I, the diode current is reduced if D is increased. However, the diode reverse voltage is more than five times greater than the output voltage at $D = 0.7$, that is, the diode should sustain a 62 V reverse voltage. Since Schottky diodes with a reverse voltage greater than 60 V are expensive and not easily available, a maximum duty cycle $D_{\max} = 0.6$

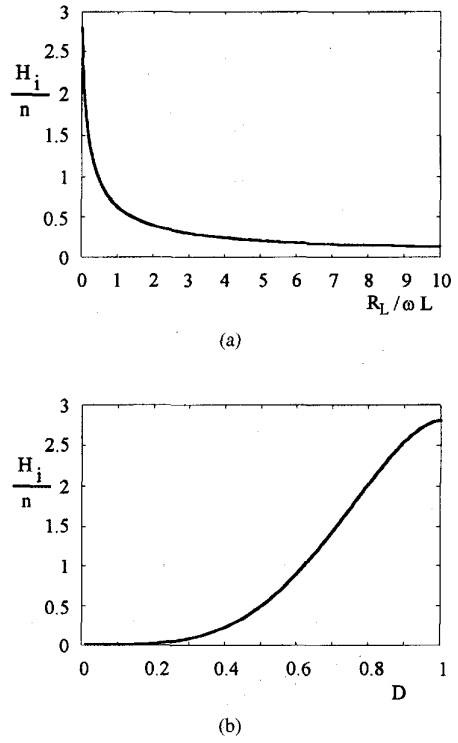


Fig. 12. Normalized values of current transfer function H_i/n as functions of $R_L/\omega L$ and D . (a) H_i/n versus $R_L/\omega L$. (b) H_i/n versus D .

was chosen. From (10) and (13), the maximum current and voltage of diodes are calculated as $I_{DM} = 1.49 I_{O \max} = 17.88$ A, and $V_{DM} = 3.61 V_O = 43.32$ V, respectively. From (3), we have $R_{L \min}/\omega L = 0.6$ at $D = 0.6$ which allows the values of the two inductances to be calculated as $L_1 = L_2 = L = R_{L \min}/0.6 \omega = (0.6 \times 2\pi \times 500 \times 10^3)^{-1} = 530$ nH. Equation (16) gives the minimum normalized input resistance as $R_{i \min}/n^2 R_{L \min} = 0.81$. The minimum input resistance at the terminals of the transformer secondary side is $R_{iS \min} = R_{i \min}/n^2 = 0.81 \times R_{L \min} = 0.81 \Omega$. The maximum current through inductors and transformer secondary winding is given by $I_m = (2P_{O \max}/R_{iS \min})^{0.5} = (288/0.81)^{0.5} = 18.85$ A.

B. Experimental Verification

A breadboard of the ac–dc converter shown in Fig. 14 was assembled to test the two-inductor rectifier. The rectifier circuit was driven by an ac–ac converter supplied by an ac line voltage V_{ac} with an rms voltage ranging from 160–275 V and composed by a ac–dc bridge rectifier with a capacitive filter and a high frequency dc–ac series resonant inverter operated

$$\begin{aligned}
 \frac{H_I}{n} &\equiv \frac{I_O}{nI_{1 \text{ rms}}} \\
 &= \frac{\sqrt{2}\omega L \cos \phi}{R_L} \\
 &= \frac{\pi\sqrt{2}(\cos 2\pi D - 1) \cos \phi}{(1 - \cos 2\pi D)^2 + (\sin 2\pi D - 2\pi D)^2 - 2\pi^2 D^2(1 - \cos 2\pi D)}
 \end{aligned} \tag{20}$$

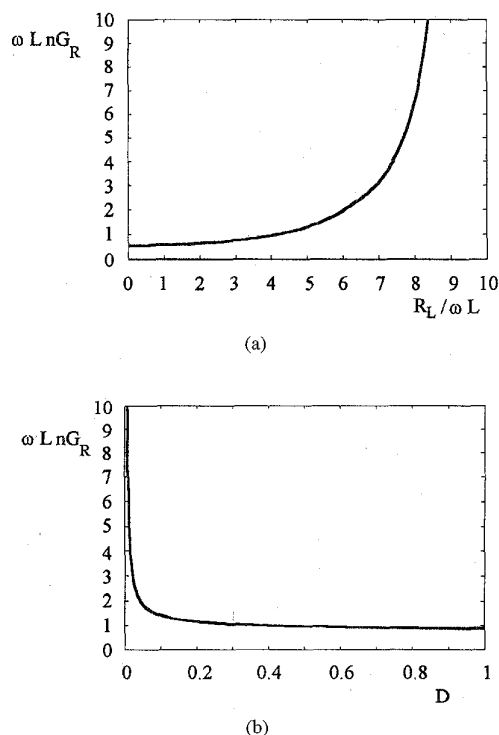


Fig. 13. Normalized values of transconductance $\omega L n G_R$ as functions of $R_L/\omega L$ and D . (a) $\omega L n G_R$ versus $R_L/\omega L$. (b) $\omega L n G_R$ versus D .

above the resonance frequency as a current source [12]. The transformer was built on a ETD39 Siemens N87 ferrite core. The primary side was wound with 24 turns of 60×0.1 mm Litz wire and the secondary with 2 turns of 15×0.15 mm copper strip. The rectifier was assembled by using two Motorola MBR2060 Schottky diodes. Inductors L_1 and L_2 were assembled by winding 11 turns of 90×0.1 mm Litz wire on two T-50 Amidon Mix #2 iron-powder toroidal cores. Since this core has an inductance factor $A_L = 49 \mu\text{H}/(100 \text{ Turns})$, an inductance $L = N^2 A_L \times 10^{-10} = 121 \times 49 \times 10^{-10} = 590 \text{ nH}$ was achieved. One electrolytic Oscon $100 \mu\text{F}/20 \text{ V}$ capacitor was used as a filter capacitor.

Fig. 15 shows the waveforms of the voltages v_{D1} and v_S

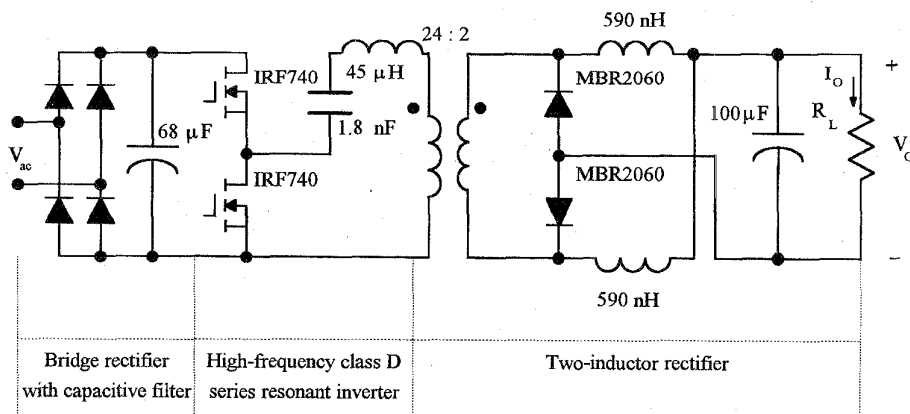


Fig. 14. Schematic circuit of the ac-to-dc off-line converter assembled to experimentally test the two-inductor rectifier.

TABLE I
PARAMETERS OF THE CURRENT-DRIVEN TWO-INDUCTOR
ZCS LOW di_D/dt FULL-WAVE RECTIFIER

D	ϕ ($^\circ$)	$R_L/\omega L$	I_{DM}/I_O	V_{DM}/V_O	$R/n^2 R_L$	$L_1/n^2 L$	nH_V	H_1/n	$\omega L n G_R$
0.05	174	2.3E4	17.78	2	3.7E-9	2	.703	6E-5	.711
0.1	168	1.4E3	8.89	2.02	9.33E-7	2	.692	9.66E-4	.723
0.2	156	86	4.44	2.09	2.26E-4	2	.649	.015	.773
0.3	144	15.8	2.96	2.23	.0053	1.95	.589	.073	.868
0.4	133	4.49	2.22	2.46	.0466	1.83	.529	.216	1.032
0.5	122	1.57	1.78	2.86	.234	1.58	.476	.483	1.312
0.6	112	.6	1.49	3.61	.81	1.18	.379	.897	1.844
0.7	104	.233	1.28	5.21	2.1	.71	.153	1.44	2.975
0.8	96.6	.079	1.137	9.7	4.22	.285	.038	2.05	6.158
0.9	91	.0167	1.04	33.7	6.7	.0456	.006	2.59	23.12
0.95	90.5	.004	1.01	129	7.64	.0062	.001	2.76	90.70

across diode D_1 and transformer secondary side terminals, respectively, measured at an operating frequency of $f = 615$ kHz, an ac input voltage $V_{ac} = 160 \text{ Vrms}$, output voltage $V_O = 12 \text{ V}$, and $I_O = 12 \text{ A}$. The Motorola MBR2060 Schottky diode data sheets give a diode parasitic capacitance of $C_T = 300$ pF and an inductance per leg of $L_p = 40 \text{ nH}$, respectively. These parasitic components, along the two filter inductances and the transformer secondary side leakage inductance L_{l2} form a resonant circuit whose resonant frequency is $f_{op} = 1/[2\pi(2L + 2L_p + L_{l2})C_T]$. This resonant circuit causes the ringing superimposed to the ideal waveforms of v_{D1} and v_S , resulting in the observed waveforms shown in Fig. 15. The parasitic oscillation could be reduced by using a printed circuit board and/or using snubber circuits constituted by a series combination of a resistance and capacitance, connected in parallel with the each diode as demonstrated in [15]. The latter solution would increase the power loss in the rectifier circuit and reduce the efficiency.

Fig. 16 shows the waveforms of the voltages across diodes D_1 and D_2 . The diodes were operated at a duty cycle $D = 0.61$ which confirms the theoretical calculation. The measured diode maximum reverse voltage $V_{DM} = 57.7 \text{ V}$ is 33.19% higher

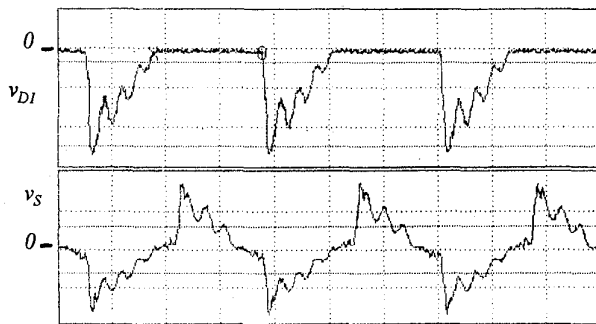


Fig. 15. Waveforms of voltage v_{D1} across diode D_1 and v_S across the transformer secondary side at an operating frequency of $f = 615$ kHz, ac input voltage $V_{ac} = 160$ Vrms, output voltage $V_O = 12$ V, and $R_L = 1 \Omega$. Vertical: upper 20 V/div; lower 30 V/div, horizontal 500 ns/div.

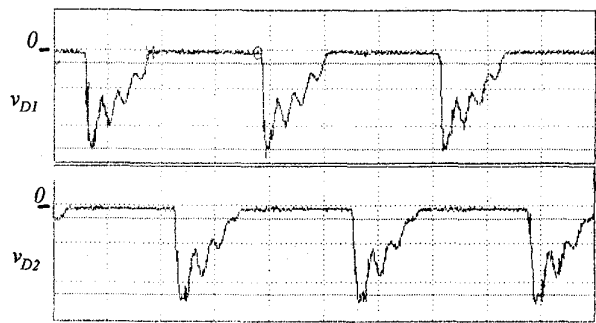


Fig. 16. Waveforms of voltages v_{D1} and v_{D2} across diodes D_1 and D_2 at an operating frequency of $f = 615$ kHz, ac input voltage $V_{ac} = 160$ Vrms, output voltage $V_O = 12$ V, and $R_L = 1 \Omega$. Vertical: upper 20 V/div; lower 4 A/div, horizontal 500 ns/div.

than the calculated V_{DM} because of the parasitic oscillations.

The waveforms of the output voltage ripple v_{oac} and the ac component of current i_{L1ac} through inductor L_1 are shown in Fig. 17. The combination of the two inductances and the filter capacitor resulted in a peak-peak voltage ripple lower than 90 mV (0.75% of the dc output voltage) under any operating condition. Current i_{L1ac} was observed with a passive current probe and was nearly the same as the theoretically predicted shifted downwards by the inductor dc component $I_{L1DC} = I_O/2 = 6$ A. Since the measured maximum ac current was $i_{L1ac} = 11.43$ A, the maximum currents through inductors were $I_{LM} = 17.43$ A which is 2.52% lower than the predicted current. The measured inductor current was only 2.52% lower than the predicted current with a measured inductance 11.32% higher than that calculated. Therefore, one can conclude that the current through inductances is slightly affected by the inductance value.

The measured results of the two-inductor rectifier are compared with the design calculations in Table II. The calculated and the measured values agreed except for the maximum diode reverse voltage V_{DM} which was 33.19% higher than calculated because of the parasitic oscillations.

A plot of the overall ac–dc converter efficiency versus the ac input voltage V_{ac} measured at an output voltage $V_O = 12$ V and different values of the output current I_O is depicted in Fig. 18(a). At a full load operation ($I_O = 12$ A) the efficiency

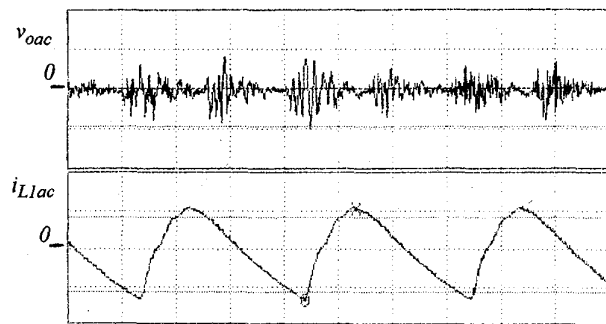
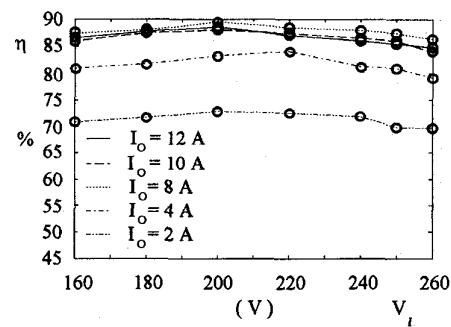
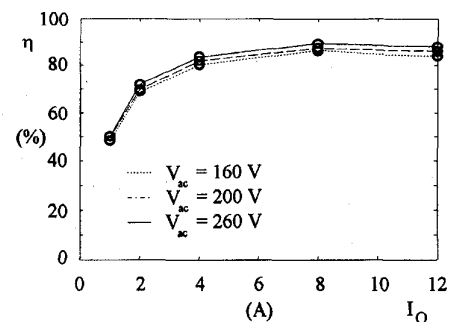


Fig. 17. Waveforms of output voltage ripple v_{oac} and ac component i_{L1ac} of the current through inductor L_1 at an operating frequency of $f = 660$ kHz, ac input voltage $V_{ac} = 220$ Vrms, output voltage $V_O = 12$ V, and $R_L = 1 \Omega$. Vertical: upper 50 mV/div; lower 8 A/div, horizontal 500 ns/div.



(a)



(b)

Fig. 18. Efficiency η as a function of V_{ac} and I_O at an output voltage $V_O = 12$ V. (a) η versus V_{ac} . (b) η versus I_O .

was never lower than 84% and reached a maximum of 88.5%. For an increasing V_{ac} , the ac voltage at the transformer primary side, and, therefore, the output voltage V_O , were kept constant by increasing the switching frequency of the series resonant inverter. A plot of the measured efficiency as a function of input voltage V_{ac} is shown in Fig. 18(b). The output voltage V_O was kept constant by operating the inverter at higher frequencies when the load resistance was increased. An efficiency $\eta = 89.4\%$ was achieved for the rectifier when operated at $I_O = 8$ A and $V_{ac} = 200$ V. The converter efficiency kept nearly constant over the entire range of V_{ac} and maintained higher than 80% for a dc output current ranging from 30–100% of I_{Omax} .

TABLE II
PARAMETERS OF THE CURRENT-DRIVEN TWO-INDUCTOR ZCS LOW di_D/dt FULL-WAVE RECTIFIER AT $V_O = 12$ V AND $R_L = 1 \Omega$

Parameter	Unit	Calculated	Measured	Deviation (%)
D	/	0.6	0.61	1.67
L	nH	530	590	11.32
V_{DM}	V	43.32	57.7	33.19
I_{DM}	A	17.57	17.31	-1.48
I_{LM}	A	17.88	17.43	-2.52
I_m	A	18.85	17.85	-5.31
nH_V	/	0.358	0.36	0.55
H/n	/	0.946	0.95	0.42

V. INTEGRATED MAGNETICS

The two separate filter inductors represent a limitation of the current-driven two-inductor ZCS low di_D/dt rectifier because they contribute to increase the rectifier number of component and cost. A solution to this problem is to combine the two inductors by winding both of them on a same E core as shown in Fig. 19. The magnetic reluctance of the E core central leg is

$$\mathfrak{R}_c = \frac{l_c}{\mu_r \mu_o A_c} \quad (22)$$

where l_c is the length of the central leg, μ_r is the core relative magnetic permeability, $\mu_o = 4\pi \times 10^{-7}$ H/m, and A_c is the central leg cross sectional area. The cross sectional area of each outside legs of an E core is half of the cross sectional area of the central leg. Therefore, if an air gap with a length l_g is introduced on each outside leg a magnetic reluctance

$$\begin{aligned} \mathfrak{R}_e &= \frac{l_c}{2\mu_r \mu_o A_c} \left(1 + \frac{l_g}{l_c} \mu_r \right) \\ &= \frac{\mathfrak{R}_c}{2} \left(1 + \frac{l_g}{l_c} \mu_r \right) \end{aligned} \quad (23)$$

is achieved for each outside leg, assuming that the fringing flux is negligible. If a ferrite core with a large relative μ_r is used, a short air gap yields a reluctance \mathfrak{R}_e much higher than \mathfrak{R}_c . As a consequence, flux ϕ_1 flows through the left outside leg, the two left parts of the core horizontal legs, and central leg. Only a negligible portion of ϕ_1 flows through the right outside leg and only a negligible part of flux ϕ_2 flows through the left outside leg. Therefore, the fluxes of two inductors L_1 and L_2 have two separate paths and do not affect each other.

An integrated inductor was assembled by winding 10 turns of a 90×0.1 Litz wire on a E20 Philips 3F3 ferrite core with $l_g = 1$ mm length air gap on each outside leg. The measured value of each inductance was $L_1 = L_2 = L = 615 \mu\text{H}$. The large-signal relative permeability of a 3F3 ferrite is $\mu_r = 4000$, the length of each vertical leg of an E20 core is $l_c = 16$ mm, and the cross sectional area of the central leg is $A_c = 30 \text{ mm}^2$. Substitution of these values in (22) and (23) yields $\mathfrak{R}_e \approx 125\mathfrak{R}_c$. This allows the two inductors to operate independently. The experimental current and voltage waveforms were not significantly modified by replacing the two separate inductors with the integrated magnetic. The

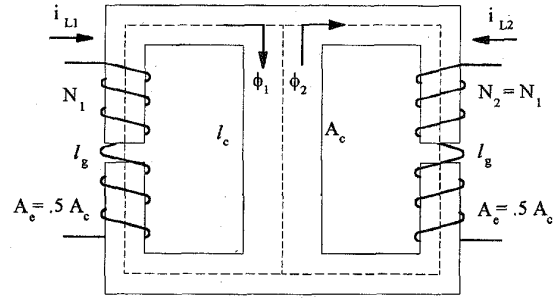


Fig. 19. Inductors integrated onto a single E core.

overall converter efficiency was lower over the entire load and input voltage ranges and a full load efficiency $\eta = 83\%$ was measured at an rms input voltage $V_{ac} = 220$ V.

VI. CONCLUSION

An analysis and experimental verifications of a current-driven two-inductor ZCS low di_D/dt full-wave rectifier have been presented. This rectifier preserves major advantages of conventional bridge and center-tapped rectifiers and overcomes many limitations of these circuits because it offers a full-wave rectification with two diodes and a transformer with only one secondary winding. As in full-wave full-bridge and center-tapped rectifiers, the filter capacitors are small because they are operated at a frequency which is twice that of the input source. Conduction losses in the diodes are reduced because the average current through each diode is one-half of the output dc current as in center-tapped rectifiers. However, each inductor of the two-inductor rectifier carries one-half of the dc output current while the entire output current flows through the filter inductor of the center-tapped rectifier. As a result, conduction losses are lower in the two-inductor rectifiers.

The current-driven two-inductor ZCS low di_D/dt full-wave rectifier overcomes the limits of its PWM counterpart because the diodes turn on at zero voltage and zero current with zero di_D/dt and limited dv_D/dt and turn off with a limited di_D/dt . As a result, the switching losses and noise level are reduced and this circuit can be operated at higher frequencies than a PWM two-inductor rectifier, resulting in lower volume and weight. Moreover, the limited values of di_D/dt allow switching losses to be reduced also when pn junction diodes are used. Since a high-frequency operation of the current-driven two-inductor rectifier is possible, the output voltage ripple is reduced by using smaller capacitances and inductances than in center-tapped and PWM two-inductor rectifiers. Finally, the current-driven two-inductor ZCS low di_D/dt full-wave rectifier is compatible with high-frequency inverters as class D and class E series resonant inverters.

Because of these features, the current-driven two-inductor ZCS low di_D/dt full-wave rectifier, is particularly suitable for high-frequency, high-power density applications requiring a low-output voltage and high-output current.

A possible limitation of the current-driven two-inductor rectifier is the high number of magnetic components. This does not significantly affect the overall volume and weight of the rectifier but contributes to the cost increase of the circuit.

However, two inductors can be integrated onto one core and this problem is overcome.

As a future work, it is recommended to evaluate the feasibility of a current-driven two-inductor rectifier with the two inductors and the transformer integrated onto only one core.

APPENDIX DERIVATION OF DESIGN EQUATIONS

The current through the transformer primary winding of Fig. 1 is given in (1). Since symmetrical behavior of the rectifier is assumed, the two inductances are $L_1 = L_2 = L$ and the dc components of the currents through the diodes are $I_{D1DC} = I_{D2DC} = I_{DC} = I_O/2$.

1) Operation at $0 \leq D < 0.5$:

A. Mode I

$$\phi \leq \omega t < 2\pi D + \phi$$

The transformer secondary current flows through inductor L_1 when D_1 is OFF and, therefore, inductor current is $i_{L1} = ni = nI_m \sin \omega t$ for $\omega t \leq \phi$. Once D_1 has turned on, the voltage across L_1 is $v_{L1} = -V_O$. This gives

$$\begin{aligned} v_{L1}|_{\omega t=\phi} &= -V_O \\ &= L \left. \frac{di_{L1}}{d(\omega t)} \right|_{\omega t=\phi} \\ &= n I_m \omega L \cos \phi. \end{aligned} \quad (24)$$

Substitution of $V_O = R_L I_O$ into (24) yields (4). The voltage across inductance L_1 is

$$v_{L1} = -V_O \quad (25)$$

and the current through L_1 is given by

$$\begin{aligned} i_{L1} &= \frac{1}{\omega L} \int v_{L1} d(\omega t) \\ &= -\frac{V_O}{\omega L} (\omega t - \phi) + n I_m \sin \phi. \end{aligned} \quad (26)$$

Since diode D_1 is conducting, voltage v_{D1} is zero. Combination of (1) and (26) gives

$$\begin{aligned} i_{D1} &= i_{L1} - ni \\ &= -\frac{V_O}{\omega L} (\omega t - \phi) + n I_m \sin \phi - n I_m \sin \omega t. \end{aligned} \quad (27)$$

Solution of $di_{D1}/d(\omega t) = 0$, which is $\omega t = 2\pi - \phi$, yields the phase angle where the current through diode D_1 reaches its maximum value. By substituting this value of the phase angle into (27), the expression of the diode maximum current is derived as

$$I_{DM1} = -2 \left[\frac{V_O}{\omega L} (\pi - \phi) + n I_m \sin \phi \right]. \quad (28)$$

Combination of (2), (4), (28), and $V_O = R_L I_O$ results in (10).

Since D_1 is OFF for $\phi + \pi \leq \omega t < \phi + 2\pi$, the average current through diode D_1 is

$$\begin{aligned} \frac{I_O}{2} &= \frac{1}{2\pi} \int_{\phi}^{\phi+2\pi} i_{D1}(\omega t) d(\omega t) \\ &= \frac{1}{2\pi} \left\{ -V_O \frac{(\phi + 2\pi D)^2 - \phi^2 + 4\pi D \phi}{2\omega L} \right. \\ &\quad \left. + n I_m [2\pi D \sin \phi - \cos \phi + \cos(\phi + 2\pi D)] \right\}. \end{aligned} \quad (29)$$

Substitution of $V_O = R_L I_O$ and (4) into (29) yields

$$\frac{R_L}{\omega L} = \frac{\pi}{1 - 2\pi^2 D^2 - \cos 2\pi D + \tan \phi [\sin 2\pi D - 2\pi D]}. \quad (30)$$

Combination of this with (2) gives (3).

B. Mode II

$$\phi + 2\pi D \leq \omega t < \phi + \pi.$$

This topological mode begins with diode D_1 turn-off, both D_1 and D_2 are OFF, and L_1 current is

$$\begin{aligned} i_{L1} &= ni \\ &= n I_m \sin \omega t. \end{aligned} \quad (31)$$

At $\omega t = \phi + 2\pi D$, the inductor L_1 and the secondary winding currents are

$$i_{L1}|_{\omega t=\phi+2\pi D} = -2\pi D \frac{V_O}{\omega L} + n I_m \sin \phi \quad (32)$$

and

$$ni|_{\omega t=\phi+2\pi D} = I_m \sin(\phi + 2\pi D) \quad (33)$$

respectively. Substitution of (32) and (33) into (31) yields

$$\begin{aligned} -\frac{V_O 2\pi D}{\omega L} + n I_m \sin \phi \\ - n I_m (\sin \phi \cos 2\pi D + \sin 2\pi D \cos \phi) = 0 \end{aligned} \quad (34)$$

which results in (2) if it is divided by $\cos \phi$ and combined with (4).

The voltages across diodes D_1 and D_2 are given by

$$\begin{aligned} v_{D1} &= v_{D2} \\ &= -V_O - L \frac{di_{L1}}{dt} \\ &= -V_O - n \omega L I_m \cos \omega t. \end{aligned} \quad (35)$$

Substitution of (4) into this yields (11) and (12).

C. Mode III

$$\phi + \pi \leq \omega t < \phi + 2\pi D + \pi.$$

During this topological mode D_1 is OFF and D_2 ON, L_1 current is $i_{L1} = ni = n I_m \sin \omega t$ as in the previous topological mode and reaches its maximum value during this interval because ϕ ranges from 90–180°. The maximum value

of i_{L1} is nI_m . Combination of $V_O = R_L I_O$, (3) and (4) gives (7).

D. Mode IV

$$\phi + 2\pi D + \pi \leq \omega t < \phi + 2\pi.$$

During this interval both D_1 and D_2 are OFF and the reverse voltages across diodes and current through inductor L_1 are still given by (35) and (31), respectively. Using the Fourier expansion, the fundamental component of the primary side voltage becomes

$$V_i = nv_s(t) = V_{Rim} \sin \omega t + V_{Xim} \sin \left(\omega t + \frac{\pi}{2} \right) \quad (36)$$

the amplitude of V_{Rim} and V_{Xim} are given by

$$V_{Rim} = \frac{1}{\pi} \int_0^{2\pi} nv_s \sin \omega t d(\omega t) \quad (37)$$

and

$$V_{Xim} = \frac{1}{\pi} \int_0^{2\pi} nv_s \cos \omega t d(\omega t) \quad (38)$$

respectively. By using (4), the transformer secondary side voltage is expressed as

$$v_s = \begin{cases} n\omega LI_m (\cos \omega t + \cos \phi) & \text{for } \phi \leq \omega t < \phi + 2\pi D \\ 2n\omega LI_m \cos \omega t & \text{for } \phi + 2\pi D \leq \omega t < \phi + \pi \\ n\omega LI_m (\cos \omega t - \cos \phi) & \text{for } \phi + \pi \leq \omega t < \phi + 2\pi D + \pi \\ 2n\omega LI_m \cos \omega t & \text{for } \phi + 2\pi D + \pi \leq \omega t < \phi + 2\pi \end{cases} \quad (39)$$

Combination of this with (36)–(38) yields (14) and (15).

2) Operation with $0.5 < D \leq 1$: The expressions of the inductor and diode current and voltages for a rectifier operation with $0.5 < D \leq 1$ are the same as for the operation with $0 < D \leq 0.5$. The transformer secondary side voltage is

$$v_s = \begin{cases} 0 & \text{for } \phi \leq \omega t < \phi + \pi(2D - 1) \\ n\omega LI_m (\cos \omega t + \cos \phi) & \text{for } \phi + \pi(2D - 1) \leq \omega t < \phi + \pi \\ 0 & \text{for } \phi + \pi \leq \omega t < \phi + 2\pi D \\ n\omega LI_m (\cos \omega t - \cos \phi) & \text{for } \phi + 2\pi D \leq \omega t < \phi + 2\pi \end{cases} \quad (40)$$

Combination of (36), (37), and (40) gives (14) and (15).

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1.5 V Full-Swing BiCMOS Dynamic Logic Circuits

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Abstract—This paper presents the design of BiCMOS dynamic logic circuits that are capable of full-swing operation from low supply voltages down to 1.5 V. Basic full-swing low-voltage BiCMOS cells are introduced. These include emitter-follower complementary n-type cell, quasi-complementary n-type cell and a p-type cell based on the transiently saturated full-swing technique. The propagation delay, power consumption and the full-swing capability of such cells have been studied both at the cell level and in a 4 b CLA design. The results clearly show the validity of the proposed circuits for high-speed low-voltage operation.

I. INTRODUCTION

BiCMOS digital integrated circuit technology has been emerging due to the demand for superior performance. By combining CMOS and bipolar transistors, BiCMOS circuits exploit the advantages of both CMOS and bipolar technologies, such as low dc power dissipation, high packing density, fast switching speed, and large load drive capabilities. On the other hand, as battery-operated portable equipment, such as mobile or handy phones and palm-top computers, continues to gain popularity, low-voltage low-power technology for integrated circuits is in great demand. The power consumption of IC's is also limited by the increasing density of transistors on a single chip. Moreover, as technology is scaled down to sub-micron regime, the supply voltages must be reduced for reliability reasons [1].

In conventional static CMOS digital circuits extra area is consumed to build repeated pull-up p devices after pull-down n devices [2]. For example, the CMOS two-input NAND gate consists of a pull-up section composed of two PMOS transistors in parallel and a pull-down section composed of two NMOS transistors in series, with each of the inputs connected to the gates of a pair of PMOS and NMOS transistors. The area penalty associated with this can be avoided using dynamic techniques by replacing the pull-up (pull-down) circuitry with a clocked PMOS (NMOS) to precharge the output high (low) [3], as shown in Fig. 1 in which circuit (a) is usually known as an n-type dynamic logic gate and circuit

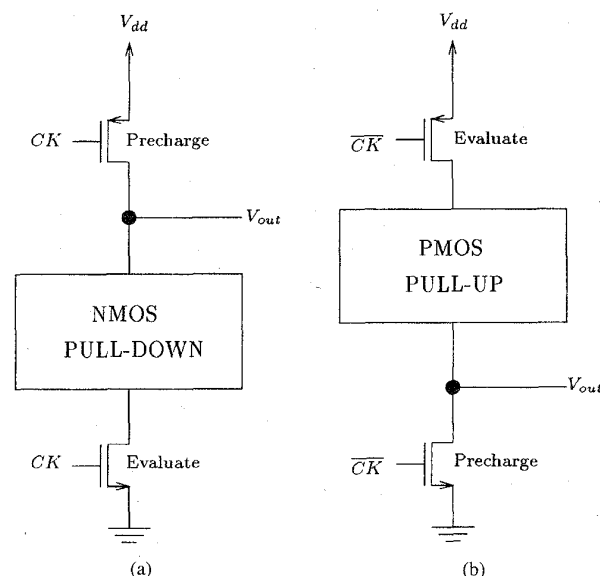


Fig. 1. CMOS dynamic circuits. (a) Precharge-high, evaluate-low. (b) Precharge-low, evaluate-high.

(b) as a p-type dynamic logic gate. However, the tradeoff is that CMOS dynamic circuits consume more power than static ones. Moreover, dynamic circuits may face charge sharing and race problems that circuit designers should take into account when encountering design of dynamic logic gates. Therefore, circuit design using the dynamic approach is generally more challenging than that using the static approach.

Although there have been many static BiCMOS logic circuits for low-voltage low-power applications reported in [4]–[8], very limited work has been done with BiCMOS dynamic circuits in general [9] and for low-voltage applications in particular. This paper presents new BiCMOS dynamic basic cells suitable for low-voltage applications. The new cells are capable of full-swing operation from low supply voltages down to 1.5 V. In the following sections, the new BiCMOS dynamic logic cells will be presented first, followed by SPICE simulations to demonstrate their performance. A brief comparison with BiCMOS static designs at the gate level is then provided. Finally, the conclusion is given.

II. BiCMOS DYNAMIC LOGIC CIRCUITS

We start this section by a brief discussion of existing cells in the context of low-voltage operation then introduce the new cells.

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