A front-end board for modular ultrasound open scanners

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Abstract. The development of advanced techniques for three-dimensional (3D) ultrasound imaging demands open scanners able to control thousands of piezoelectric transducers simultaneously and independently on two-dimensional (2D) array probes. This work proposes a 64-channel front-end module (FEM) capable of transmitting, receiving, condition, and digitize ultrasound signals and of transferring them to a processing unit by using a 10GEthernet protocol with a global data-rate of 40 GBps. Multiple FEM units can synchronously operate by sharing a common front-plane board to build high channel count (N×64) open scanners.

Keywords: ultrasound imaging, modular open platform, high channel count.

1 Introduction

The development of advanced techniques for three-dimensional (3D) ultrasound imaging requires open scanners [1] (i.e., systems characterized by high flexibility, programmability, and access to raw echo-data) able to simultaneously and independently control thousands of piezoelectric transducers on two-dimensional (2D) array probes. Even though the channel count can be increased by synchronizing multiple research scanners [2], [3], managing such an architecture is extremely complex, and, at some extent, physically and computationally prohibitive. Also, it has limitations on data transfer among systems, to host PCs [4], or to graphic processing units (GPUs) due to the communication devices, which cannot sustain the high rates (in the order of tens/hundreds of Gbps) required to transfer, acquire, and, possibly, process the raw radiofrequency data.

This work proposes a 64-channel front-end module (FEM), which can be replicated to build high channel count (N×64) open scanners through the synchronous operation of multiple FEM units that share a common front-plane board.

2 Methods

2.1 Front-end module architecture

The FEM manages 64 transmission (TX) and reception (RX) channels: it controls the TX of high voltage signals; the RX, conditioning, analog to digital conversion of echo-

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signals; and the data transfer to a cascade processing back-end module (BEM). The FEM is realized by two stacked boards: the baseboard (BB) and the FPGA module. The BB is implemented in a 16×10 cm printed circuit board, where four 16-channel TX devices (STHV1600, STM, Italy) generate ±100V, 3/5-level, pulsed waveforms and manage the TX/RX transition. The parameters of each transmitter are stored in an internal memory via serial peripheral interface (SPI). In RX, the analog signals gathered by the probe are amplified, filtered, and digitized by two 32-channel analog front-end chips (AFE5832LP, Texas Instruments, USA). The amplification is performed by a low noise amplifier (LNA), a variable attenuator for time-gain compensation and a selectable gain power amplifier. A third-order low-pass filter can be set at the desired cut-off frequency. The integrated analog to digital converters (ADCs) work on 10-bit resolution at 50 MSps. The FEM can communicate with a BEM through a quad small form-factor pluggable optical transceiver (FTL410QE4N, Finisar, USA). This is inserted in a metal cage and connected to an optical fiber with a multi-fiber termination push-on connector to be easily linked to different processing units. The FPGA module is implemented in a 6×8 cm board and embeds a 2-GB random access memory and an FPGA (Cyclone 10 GX, Intel, USA). Currently, the latter oversees the control of the BB's devices and communication with the BEM. Having the FPGA on a different PCB facilitates a possible upgrade based on a new, more powerful and/or cost-effective device.

2.2 FPGA firmware

The FPGA firmware oversees the TX of the sampled data to the BEM and the RX and interpretation of the commands to control and program the transmitters, the AFEs, and the transceivers. The FPGA also receives 2×16 LVDS digital streams from the ADCs: this data is deserialized, segmented into standard Ethernet frames and sent to the BEM through four 10GEthernet channels via optical communication. To correctly implement the media access controller (MAC) and the physical (PHY) layers of the 10GEthernet protocol, the firmware relies on the Low Latency (LL) Ethernet 10G MAC and the Intel Cyclone 10GX Transceiver PHY Intel FPGA IP cores.

The current operational settings of the transmitters and AFE interfaces and of the optical transceivers are selected by the BEM, which sends the programming commands to the FPGA through the Ethernet channel. Relying on a standard organization of the data packets, the FPGA can decode the commands, determine which is the recipient module and eventually forward the commands.

3 Results and Discussion

The TX, RX, and data streaming functionalities were tested. The transmitters were programmed to generate the TX signals with varying burst length, frequency and amplitude. The TX output was acquired with an oscilloscope (DSOX2014A, Keysight, USA) and compared with the expected one. Fig. 1 shows an example of a 10V-amplitude, 4-cycle burst at 4 MHz and demonstrates the good match between the two signals.

A waveform synthesizer (3325A, Agilent, USA), generating a saw-tooth signal, was connected to the RX AFE input. The digitized data, deserialized by the FPGA, was visualized on a PC through a signal analyser software (SignalTap II Logic Analyzer, Intel, USA) and resulted consistent with the input. In RX, the on-board FPGA received data, converted with 10 bits @50 MSps, from the 2×16 LVDS lanes of the two AFEs (1 Gbps per lane), accounting for a total transfer rate towards the FPGA of 32 Gbps.

The transfer rate towards the BEM was measured by generating, directly on the FPGA, test frames, which were transferred through the four optical channels to a PC, equipped with a standard network interface card (NIC). The quad data-stream was buffered and transmitted as 10GEthernet protocol frames through four independent high-speed bitstreams (10 Gbps per channel) to the optical transceivers, and a maximum output data rate of 40 Gbps (4×10 Gbps) was measured.

In conclusion, these results confirm the board suitability for the application. Further work is in progress towards the testing of a combination of multiple (N) boards, with the goal of implementing an N×64 channel echographic system.

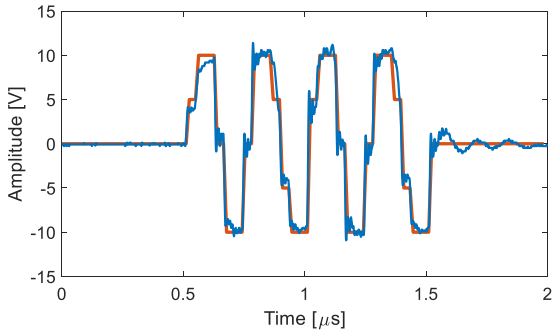

Fig. 1. Example of a 10V-amplitude, 4-cycle burst with frequency of 4 MHz: the signal generated by the 5-level pulser (blue line), acquired through the oscilloscope, is compared to the theoretical waveform (orange line).

References

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