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ORIGINAL RESEARCH

Modelling of a pulse-skipping modulated DC–DC buck converter

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Abstract

This paper presents an accurate averaged model of a Buck converter controlled via pulse-skipping modulation (PSM). The derived model includes the parasitic elements of the circuit components, and it is not yet given in the literature. Output capacitor voltage and inductor current are analysed under steady-state operation by deriving the expressions of average and ripple amplitude values. The accuracy improvements introduced by the proposed model are validated by comparison against models existing in the literature. A design procedure based on the proposed model is formulated and experimentally validated. The expressions for the control-to-output and the input-to-output network functions, both including the parasitic components of the converter circuit, are derived and utilized to exploit the circuit dynamic behaviour in the frequency domain.

1 | INTRODUCTION

Many modern electronic applications involve devices that must remain active for their whole useful life. During most of their operating life, these circuits are operated under 'sleep' or 'standby' modes [1]. In these cases, a high efficiency conversion must be ensured even at light load operations [2]. As known, the conversion efficiency of a DC–DC converter is higher at heavy load but drastically reduces when the converter operates at light loads. For this reason, several efforts have been spent to improve the conversion efficiency of DC–DC converters when operated at light loads [3–5]. One of the most relevant aspects influencing the converter performance is its modulation. Pulse-skipping modulation (PSM), for example, operates similarly to pulse width modulation (PWM), but some cycles are skipped to regulate the output voltage [6]. Due to the reduced number of pulses, the switching losses are reduced, and, therefore, PSM represents a suitable modulation technique for those applications where high conversion efficiency at lights load is required, such as wireless sensor networks [7], energy harvesting [8–11] and photovoltaic systems [12–15].

Differently from the PWM modulation, the PSM technique is not yet widely studied in literature. Only a few works related to steady-state models have been proposed. In [16], the efficiency of a Flyback converter driven by the PSM and PWM is compared. The results highlight that the converter results in a higher efficiency at light loads and in a faster transient speed response when operated by PSM than by PWM. In [17] an extensive model of a Buck converter operating with PSM is proposed, but only its steady-state operation is investigated. Moreover, both continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are studied, but the effect of the parasitic components is completely neglected. In [18], a digital controller for the voltage regulation of the Buck converter operating with PSM is proposed. The same paper shows that a PSM with an optimized number of skipped cycles results in better performance than both PWM and pulse frequency modulation (PFM). In [19], the same digital control strategy proposed in [18] has been modified to achieve also a duty cycle variation. Here, it is also shown that this approach leads to a monolithic spectral behaviour facilitating the design of the input filters for EMI reduction. Although this approach has several benefits, this strategy is computationally complex, and an FPGA is needed to ensure high-speed calculations and, therefore the circuit complexity and costs are increased. Other analyses of a Buck converter operating with PSM in terms of voltage transfer function, output voltage ripple and average inductor current in steady-state condition are presented in [20]. Although these analyses give very accurate results under ideal conditions, the models are not reliable in describing the practical converter

operations, because the parasitic elements of the circuit components are not considered. This is because, as well known, parasitic highly affect the converter operation under in both steady-state and dynamic conditions. In steady-state, voltage ripples and average current can be significantly influenced by capacitor and inductor parasitic resistances [21, 22]. In dynamic condition, parasitic resistances affect the position of zeros and poles and, therefore, they have an important role for the stability of the system [23, 24].

For this reason, in this paper, an accurate analysis describing the DC–DC Buck converter behaviour operating with PSM under both steady-state and dynamic conditions is proposed.

The main objectives of the proposed paper to address the lack in literature can be summarized as follows:

- To derive a steady-state input-to-output voltage transfer function that considers the parasitic of the components.
- To derive the average value of the inductor current and the amplitude of its ripple.
- To derive an accurate expression of the output voltage ripple.
- To apply the derived equation in a design procedure of a Buck converter with PSM.
- To validate the accuracy of the proposed equation through extensive experimental measurements.
- To propose a small-signal model using the circuit-averaging method. The two main transfer functions, that is, the input-to-output voltage transfer function and the control-to-output network functions are derived. Note that the circuit averaging method allows us to obtain intuitive insight of the converter behaviour by a simpler linear model with respect to the state-space averaging method which requires considerable matrix algebra manipulation when many parasitic are considered.

The advantage of a linearized model is that it can be easily studied by using software suitable for symbolic analysis so that also a parametric analysis can be performed [25]. Moreover, it allows the bode plots, useful for the feedback-loop design, to be derived.

The paper is structured as follows. First, an extensive state space representation, complete with parasitic components of both passive components and switching devices, is presented. In Section 2, the analytic voltage expressions of the network functions, DC and ripple inductor current, DC and ripple output voltage, are derived. Design equations for the converter are proposed by considering the worst-case scenario of the peak-to-peak output voltage ripple. Following, the accuracy of the proposed model is compared with other models available in literature. In Section 3, the experimental validation of the proposed steady-state model is presented. In Section 4, a new small signal model for the Buck converter operating under PSM is derived and the control-to-output voltage and the input-to-output voltage functions, which are useful for the feedback loop design, are proposed and validated. Final remarks and conclusions close the paper.

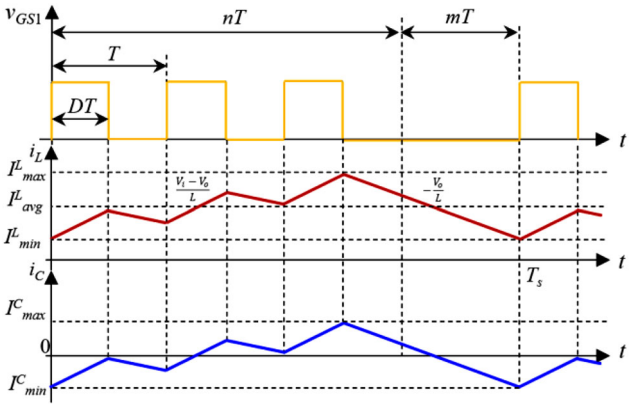

FIGURE 1 Current and voltage waveforms of Buck converter with PSM with $n = 3$, $m = 1$ and $D = 0.5$. Upper MOSFET driving signal v_{GS1} (yellow trace), inductor current i_L (red trace) and capacitor current i_C (blue trace)

2 | PULSE-SKIPPING MODULATED BUCK CONVERTER

Pulse-skipping modulation is a variation to the classic PWM where a degree of freedom is added by skipping m pulses every $m + n$ pulses. An example of the controlled switch driving signal for this modulation is represented by the yellow trace in Figure 1, which also shows the inductor and capacitor currents during a generic period in CCM for a Buck converter. Thus, the modulation depth can be defined by two parameters: (a) the duty cycle D and (b) the number of skipped pulses m. The ratio between the total pulses and the skipped pulses is $M = m/(n + m)$. As shown in Figure 1, the complete period of the PSM is $T_S = (m + n)\,T$, where T is the single pulse period.

In this work, this modulation technique is studied on a Buck converter by considering the parasitic components, as shown in Figures 2a and 2b. Depending on the use of a MOSFET or a diode as a switch Q_2, a synchronous or asynchronous buck converter is obtained. In this paper, a synchronous converter is studied, according to the circuit shown in Figure 2a. The MOSFETs are modelled as ideal switches with a series conduction resistance (the power MOSFET channel ON resistance): r_{DS1} resistance for Q_1, and r_{DS2} for Q_2. Accounting for different resistances makes the following analysis simple for generalization towards asynchronous buck converters. The dynamic behaviour of this topology in CCM is easily described by two sets of state equations, obtained from Kirchhoff's voltage law (KVL) and Kirchhoff's current law (KCL) of the two operation modes in Figures 2b and 2c. Considering the two state variables $x_1 = i_L$ and $x_2 = v_C$, and the independent input $u = V_I$, the two state matrices A_{ON}, A_{OFF} and the two input matrices B_{ON}, B_{OFF} are

$$A_{ON} = \begin{bmatrix} -\dfrac{r_L + r_{DS1}}{L} & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{R_L C} \end{bmatrix}, \quad B_{ON} = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} \tag{1}$$

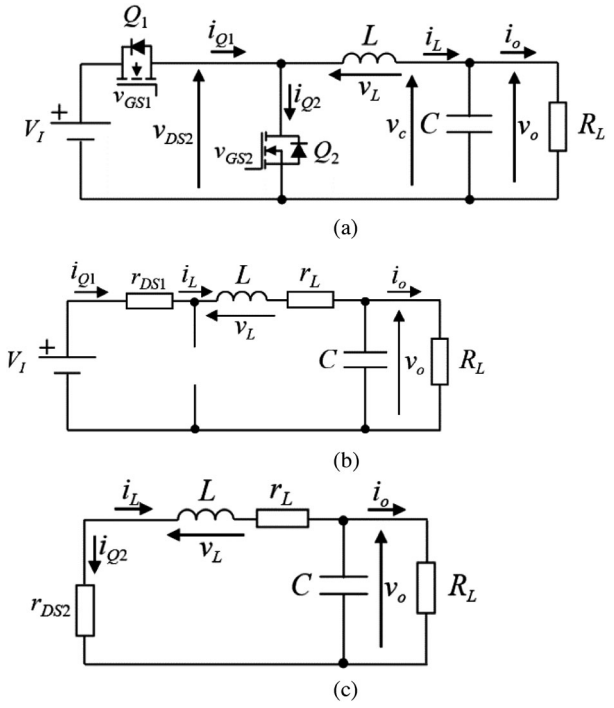

FIGURE 2 Buck converter topology. (a) Electrical circuit of the synchronous converter. (b) ON state equivalent circuit. (c) OFF state equivalent circuit

$$A_{OFF} = \begin{bmatrix} -\dfrac{r_L + r_{DS2}}{L} & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{R_L C} \end{bmatrix}, \quad B_{OFF} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{2}$$

2.1 | Voltage transfer function

The steady-state DC voltage transfer function of the PSM-driven Buck is derived through a state-space average approach. The normalized ON period of the circuit is $T_{ON}/T_s = (1-M)D$, and the normalized OFF period of the circuit is $T_{OFF}/T_s = 1 - (T_{ON}/T_s) = 1 - (1-M)D = 1 - D + MD$. The state space representation (1) and (2) is averaged giving the representation of the system.

$$\dot{x} = \left[(1-M)DA_{ON} + (1 - D + MD)A_{OFF}\right]x + \\ + \left[(1-M)DB_{ON} + (1 - D + MD)B_{OFF}\right]u \tag{3}$$

$$A = A_{OFF} + D(A_{ON} - A_{OFF}) - MD(A_{ON} - A_{OFF}) \tag{4}$$

$$B = B_{OFF} + D(B_{ON} - B_{OFF}) - MD(B_{ON} - B_{OFF}) \tag{5}$$

Through some manipulations the two averaged states and input matrices can be rearranged as

$$A = \begin{bmatrix} -\dfrac{r_L + r_F + (D - DM)(r_{DS} + r_F)}{L} & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{R_L C} \end{bmatrix} \tag{6}$$

$$B = \begin{bmatrix} \frac{1}{L}D(1-M) \\ 0 \end{bmatrix} \tag{7}$$

To derive the voltage transfer function, the averaged system will be considered at equilibrium

$$\begin{bmatrix} 0 \\ 0 \end{bmatrix} = A \begin{bmatrix} I_L \\ V_C \end{bmatrix} + B V_I \tag{8}$$

At equilibrium, the output voltage V_o is equal to the voltage across the capacitor V_c. Through some simple manipulations, the output voltage can be found as follows:

$$M_V = \frac{V_o}{V_I} = \frac{R_L\left[D(1-M)\right]}{R_L + r_L + r_F + (D - MD)(r_{DS} - r_F)} \tag{9}$$

2.2 | Ripple and average inductor current

The current in each sub-interval is approximated as linear, under the assumption that the effects of the inductor series resistance on the current waveforms are negligible and the inductor voltage is constant and equal to $v_L = V_I - V_O$ during the ON state, and $v_L = -V_O$ during the OFF state. The inductor DC current I_L^{avg} can be calculated by integrating the instantaneous current $i_L(t)$ from 0 to T_s. This integral can be divided into $n + m$ sub-intervals

$$I_L^{avg} = \frac{1}{T_s}\int_0^{T_s} i_L(t)dt \\ = \frac{1}{T_s}\left[\int_0^{DT} i_L(t)dt + \int_{DT}^{T} i_L(t)dt + \cdots \right. \\ \left. \cdots + \int_{(n-1)T}^{(n-1)T+DT} i_L(t)dt + \int_{(n-1)T+DT}^{nT} i_L(t)dt + \int_{nT}^{(n+m)T} i_L(t)dt\right] \tag{10}$$

Assuming to operate in steady-state conditions, it is safe to assume for the inductor current that $i_L(0) = i_L(T_s) = I_L^{min}$.

By using this assumption, apart from the first and the last integral (which can be computed as the area of a triangle), all the integrals can be computed as the area of a trapezoid. For the kth ON state ($k < n$), by assuming that the value of the current at the start of this interval equals $I(L,k)^{ini}$, the area is

$$\frac{1}{2}\left[I_{L,k}^{ini} + \left(I_{L,k}^{ini} + \frac{V_I - V_o}{L}DT\right)\right]DT \tag{11}$$

and for the kth OFF state:

$$\frac{(T - DT)}{2}\left[I_{L,k}^{ini} + \left(I_{L,k}^{ini} + \frac{V_I - V_o}{L}DT\right)\right.$$

$$+\left(I_{L,k}^{ini}+\frac{V_{IN}-V_o}{L}DT-\frac{V_o}{L}(T-DT)\right)\Bigg] \quad (12)$$

The area of the kth subinterval (both ON and OFF states) is equal to

$$I_{L,k}^{ini}T+\frac{1}{2}\frac{V_I-V_o}{L}D\left[DT^2+2T(T-DT)\right]-\frac{1}{2}\frac{V_o}{L}T^2(1-D)^2 \quad (13)$$

and the difference among the area of different subintervals is linked only to first term $I_{(L,k)}{}^{init}T$. Following terms for $k < n$ are obtained by

$$I_{L,k+1}^{ini}=I_{L,k}^{ini}+\frac{V_I-V_o}{L}DT-\frac{V_o}{L}(T-DT)=I_{L,k}^{ini}+k\left(\frac{V_I}{L}DT-\frac{V_o}{L}T\right) \quad (14)$$

The value $I_{(L,k)}{}^{init}+[(V_{IN}-V_o)\,DT]/L$ is the maximum value of the inductor current assumed in the kth interval (ON and OFF states) and in the following we name it $I_{L,k}{}^{max}$, for $k < n$. Being $I_{L,1}{}^{ini} = I_L{}^{min}$ and the max value of the inductor current achieved after the nth ON state, we easily achieve

$$I_L^{\max}=\left(I_{L,n-1}^{ini}+\frac{V_I-V_o}{L}DT\right)=I_L^{\min}+\frac{V_I}{L}nDT-\frac{V_o}{L}(n-1+D)T \quad (15)$$

At this point, by assuming that at the end of the period the inductor current again assumes the value $I_L{}^{min}$, and by considering that the discharge has a slope of $-V_o / L$ and is long $T(m + 1 - D)$ we find

$$I_L^{\min}=I_L^{\max}-\frac{V_o}{L}T(m+1-D) \quad (16)$$

This, after some simple manipulations, leads to the ideal voltage transfer function given as

$$\frac{V_o}{V_I}=\frac{n}{n+m}D=(1-M)D \quad (17)$$

This last result allows all the relations to be derived as functions of V_o. The slope of the inductor current during the ON state is

$$\frac{V_I-V_o}{L}=\frac{V_o(n+m)/nD-V_o}{L}=\frac{(n+m-nD)\,V_o}{nDL} \quad (18)$$

Thus, the DC value of the inductor current is

$$I_L^{avg}=I_L^{\min}+\frac{V_I}{L}\left(n\frac{DT}{2}+\frac{nDT}{2(n+m)}(1-D)\right)-\frac{V_o}{L}\left(n\frac{T}{2}\right) \quad (19)$$

The previous expressions can be furtherly elaborated by writing them only as functions of V_I or V_o

$$I_L^{\max}=I_L^{\min}+\frac{V_o(n+m)T}{L}-\frac{V_o(n-1+D)T}{L}=I_L^{\min}+\frac{V_o(m+1-D)T}{L} \quad (20)$$

$$I_L^{avg}=I_L^{\min}+\frac{V_o}{L}\left[\frac{(n+m)T}{2}+\frac{(n+m)T}{2(n+m)}(1-D)-n\frac{T}{2}\right]=I_L^{\min}+\frac{V_o}{L}\left(\frac{m+1-D}{2}T\right) \quad (21)$$

Finally,

$$I_L^{avg}=\frac{I_L^{\min}+I_L^{\max}}{2} \quad (22)$$

Thus, the inductor ripple current is symmetric and equal to

$$\Delta I_L=\frac{V_I}{L}nDT-\frac{V_o}{L}(n-1+D)T=\frac{V_o}{L}(m+1-D)T \quad (23)$$

2.2.1 | Capacitor voltage ripple

The capacitor voltage ripple is linked to the ripple of the capacitor charge. Starting from the capacitor current:

$$i_c(t)=i_L(t)-I_L^{avg} \quad (24)$$

In steady-state condition, the average value of the ripple voltage capacitor is zero, while its minimum and maximum values are related by

$$I_C^{\min}=I_L^{\min}-I_L^{avg}=\frac{1}{2}\left(I_L^{\min}-I_L^{\max}\right)=-\frac{1}{2}\left(I_L^{\max}-I_L^{\min}\right)=-I_C^{\max} \quad (25)$$

Indeed, in a Buck converter, the capacitor current ripple is equal to the inductor one. Although we are interested in the ripple value of the charge, the previous expression is useful since it is possible to express the maximum and minimum values of I_c as a function of output voltage V_o. Thus,

$$I_C^{\max}=\frac{V_o}{L}\left(\frac{m+1-D}{2}T\right)=-I_C^{\min} \quad (26)$$

The difference between the current and the charge ripple values is that the latter has not a zero-average value, which instead is

$$Q_c^{avg}=C\,V_0 \quad (27)$$

In addition, the discharge of capacitor does not occur during the OFF interval but only when the capacitor current is

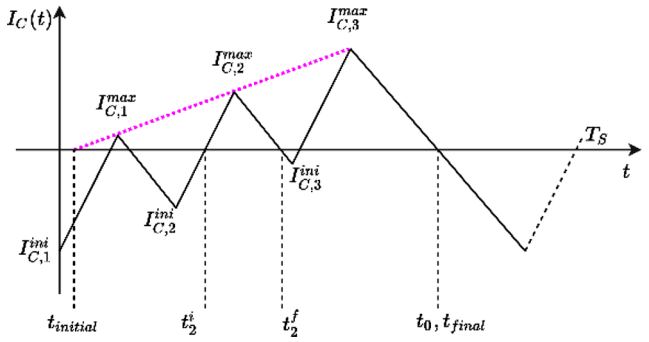

FIGURE 3 Capacitor current showing the initial and maximum values for each period, and the times for the intersection points in period $k = 2$ converter topology

negative, and this occurs when the inductor current is lower than its average value. To evaluate the maximum and minimum capacitor charge values, the instant when the capacitor current changes sign must be determined. To better understand the mechanism, we can refer to Figure 3. Let us consider the last interval of inductor discharge of duration $T(1 - D + m)$. During this period, the capacitor charge reaches its maximum in correspondence of the intersection of the segment of slope $-Vo/L$ with the time-axis t_0 (i.e., when capacitor current is zero).

Theoretically, it should be possible not only to determine t_0, but also a sequence of intersections $\{t_{k1}{}^i, t_{k1}{}^f, t_{k2}{}^i, t_{k2}{}^f, \ldots, t_{kn}{}^f, t_0\}$, as shown in Figure 3, for the determination of the exact value of Q. An analytical formulation cannot be done without resorting to very complicated expressions, and this would result in a procedure not useful for the design. Thus, although such a procedure can led to an exact evaluation of the charge inside the capacitor, a simplified approach that leads to a manageable formula is preferred. Referring again to Figure 3, the goal is to compute the area defined by the curve above (or under) the time axis. It is possible to approximate this area by using the line with the 'average' slope represented in purple. In this case, the area is easily computed as follows:

$$\frac{1}{2}\left(t_{final} - t_{initial}\right) I_C^{\max} \tag{28}$$

$$t_{final} = t_0 = T_s - \frac{m + 1 - D}{2(n + m)} T_s = \frac{2n + m + 1 - D}{2} T \tag{29}$$

For the computation of $t_{initial}$, the average slope can be used:

$$\frac{V_I - V_o}{L} D - \frac{V_o}{L}(1 - D) = \frac{(m + n - nD)\, V_o}{nL} - \frac{V_o}{L}(1 - D) = \frac{mV_o}{nL} \tag{30}$$

and then, by posing the curve with an average slope equal to zero:

$$I_C(t) = \frac{mV_o}{nL}\left(t_{nitial} - (n - 1)\, T - DT\right) + I_C^{\max} = \frac{mV_o}{nL}\left(t_{nitial} - (n - 1)\, T - DT\right)$$

$$+ \frac{V_o}{L}\left(\frac{m + 1 - D}{2} T\right) = 0 \tag{31}$$

which leads to

$$t_{initial} = \frac{mn - 2m(1 - D) - n(1 - D)}{2m} T \tag{32}$$

Since this area approximates the difference between the maximum and the minimum value of Q, the voltage ripple is expressed as

$$\Delta V_o = \frac{1}{2} \frac{n + m}{m} \left(\frac{m + 1 - D}{2}\right)^2 \frac{V_o}{LC} T^2 \tag{33}$$

2.3 | Converter design procedure

Equations (23) and (33) are useful to determine the inductor and capacitor values from the maximum desired ripple. However, the parameters m and n play a conflicting role during converter design. Considering all variables but n and m as fixed and unitary in (23) and (33), it can be observed that both ripples are proportional to both m and n. Thus, small values of m and n result in a lower overall ripple. However, the regulation resolution of the PSM is proportional to $m + n$. For design purposes, the total number of pulses $m + n = n_{tot}$ should be defined before sizing the capacitor and inductor. By re-arranging (23), the inductor equation is obtained as follows:

$$L > \frac{V_I T}{\Delta I_L} \left(\frac{(m + 1 - D)\,(n_{tot} - m)\, D}{n_{tot}}\right) \tag{34}$$

The maximum of (34) in terms of m slightly varies with D; however, it is conservative to evaluate it at $m = 0.5\ n_{tot}$ for a worst-case analysis. With the same considerations, the capacitor equation is

$$C > \frac{1}{2} \frac{V_I T^2}{L \Delta V_o} \left(\frac{n_{tot} - m}{m}\right) D \left(\frac{m + 1 - D}{2}\right)^2 \tag{35}$$

Design equations are given as a function of the input voltage but can be easily re-arranged as a function of output voltage (e.g., for an application of battery charging) through (9).

3 | SIMULATION AND EXPERIMENTAL VALIDATION

Two tests have been performed to validate the model. The first is against time-domain numerical simulations of the system. This comparison aims at validating the accuracy of the steady-state state-space model. The second is against experimental measurements and aims at validating the accuracy of the DC and ripple quantities estimation.

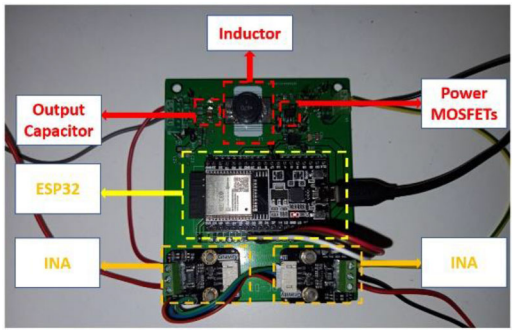

FIGURE 4 Designed Buck converter PCB prototype: components

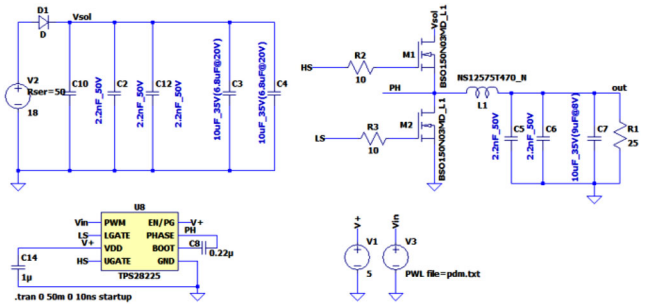

FIGURE 5 Buck converter LTspice simulation with manufacturer components models

3.1 | Buck converter characteristics and nominal condition

The equations obtained in the previous section were used to design a Buck converter. The total number of pulses is $n_{tot} = 32$, with a constant duty-cycle $D = 0.5$. Considering a maximum current ripple of 1.2 A and a maximum output voltage ripple of 0.5 V, the values for the inductor and capacitor are determined through (34) and (35). Although the previous analysis is general and it is valid independently from the DC–DC converter power rating, the complete characteristics of the converter, operating at a constant input voltage, are summarized in Table 2. The resulting converter, as shown in Figure 4, was assembled using the components given in Table 3. The PSM control signals are generated by ESP32 board and used to control the power MOSFET by the TPS28225 gate driver. As shown in Figure 4, the board also contains two INA219 for the input and output current sensing.

3.2 | Validation test 1: numerical simulation

The first test involved a comparison between the state-space system described in (1)–(5) and the simulated system in LTspice and Matlab Simulink. Both the Simulink and the LTspice models were implemented by using the values listed in Table 2 along with some libraries provided by manufacturers. The LTspice circuit is shown in Figure 5. The comparison was performed for four different operating conditions, shown in Table 4. In particular, the operating condition B is the one featuring the largest ripples for both inductor current and output voltage.

The transient and steady-state output voltage v_o and the inductor current i_L waveforms are shown in Figure 6. Different modulation settings were considered to evaluate the accuracy of the proposed method over many configurations. Figures 6a and 6b show the output voltage and inductor current for $n = 8$. The cases for $n = 16$, $n = 24$ and $n = 31$ are shown in Figures 6c–h respectively. For all tests, a value $n + m = 32$ has been assumed.

The simulation results confirm that the ripple evaluation through (23) and (33) is accurate and the converter designed using (34) and (35) respects the 1.2 A and 0.5 V ripple limits.

3.3 | Validation test 2: experimental comparison

The workbench utilized to run the experimental measurements, including the circuit given in Figure 4, is shown in Figure 7. The results, in terms of DC and ripple output voltages, are shown in Table 5. The experimental results were compared with LTspice simulations and the models available in [17] and [18]. The output voltage ripple resulting from the proposed analytical model was calculated by using (33) while the DC output voltage by using (9). The proposed method results in an accurate estimation of both the DC and output voltages ripple and has higher accuracy than other models available in the literature. A comparison between the measured output voltage and the boundaries given from Equations (33) and (9) is shown in Figure 8. Also, the inductor current ripple was evaluated, as shown in Table 6. Experimental results confirm that (23) allows for an accurate inductor current ripple estimation.

Finally, in Figure 9, DC–DC conversion efficiency for different values of n is shown. As expected, the efficiency increases as the number of pulses increases. The efficiency has been experimentally measured and compared with the converter efficiency given by the expression derived as follows. The considered losses are the conduction losses P_{con}, the switching losses P_{sw} and the parasitic losses on inductor and capacitor P_{rL} and P_{rC}:

$$P_{loss} = P_{con} + P_{sw} + P_{rL} + P_{rC} \tag{36}$$

From the losses, the efficency can be calculated as the ration between the output power P_o and the total input power $P_i = P_o + P_{loss}$ as follows:

$$\eta = \frac{P_o}{P_i} = \frac{P_o}{P_o + P_{loss}} = \frac{1}{1 + \frac{P_{loss}}{P}} = \frac{1}{1 + \frac{D(1-M)r_{DS1} + (1-D)Mr_{DS2} + r_L}{R_L} + \frac{f_s C_o R_L}{M_V^2} + \frac{r_C R_L (1-D)^2 M^2}{12 f_s^2 L^2}} \tag{37}$$

where M_v is the voltage transfer function shown in (9).

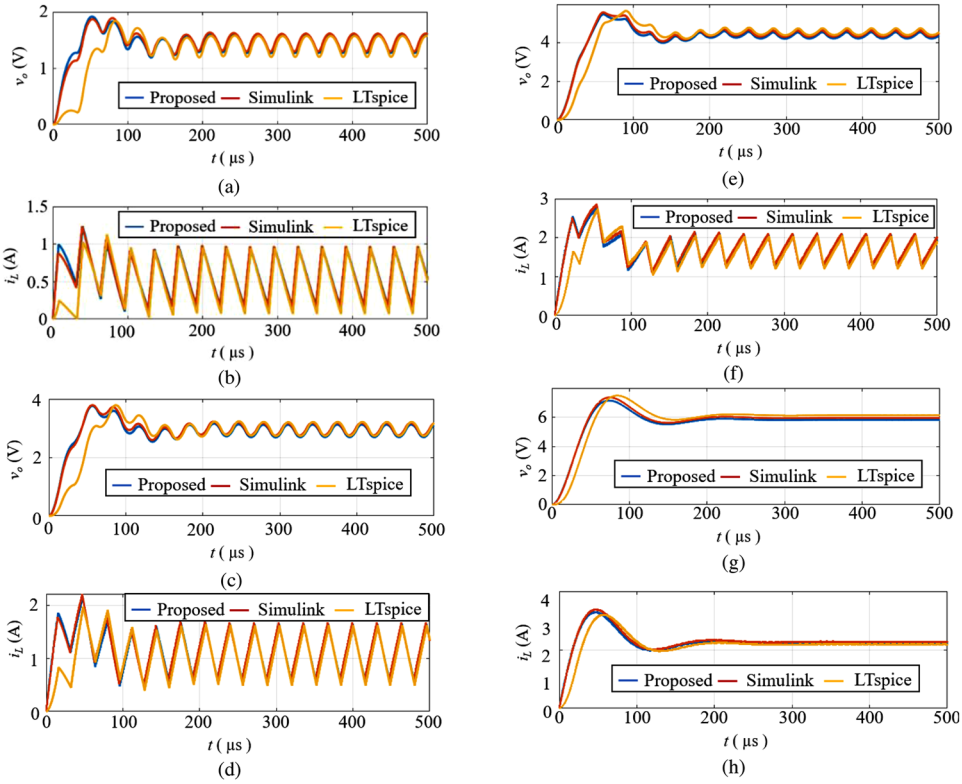

FIGURE 6 Inductor current and output voltage waveforms for different operating conditions. (a) Output voltage for $n = 8$. (b) Inductor current for $n = 8$. (c) Output voltage for $n = 16$. (d) Inductor current for $n = 16$. (e) Output voltage for $n = 24$. (f) Inductor current for $n = 24$. (g) Output voltage for $n = 31$. (h) Inductor current for $n = 31$

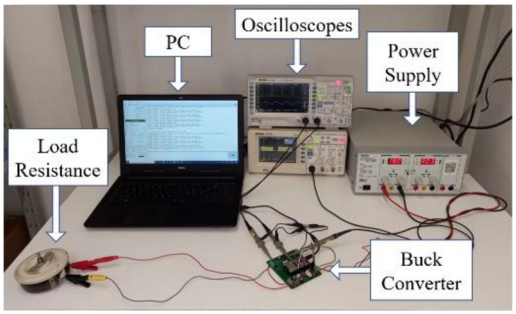

FIGURE 7 Experimental setup and measurements instrumentation

4 | SMALL SIGNAL MODEL

In this section, the small signal equivalent circuit for a PSM operated Buck converter is derived. While several efforts have been performed for the small signal modelling (SSM) of Buck converter with PWM [26, 27], the SSM under PSM is missing in literature.

4.1 | Steady-state and small signal average model

According to Figures 1 and 10, the steady-state value of the current through MOSFET Q_1 is

$$I_{Q1} = \frac{1}{(n+m)T}\left[n\int_{DT} I_L dt + m\int_{(1-D)T} 0\ dt\right] = \frac{nD}{n+m} I_L \tag{38}$$

By using the same approach, the steady-state values of V_{DS2} and I_{Q2} are derived as

$$V_{DS2} = \frac{1}{(n+m)T}\left[n\int_{DT} V_i dt + m\int_{(1-D)T} 0\ dt\right] = \frac{nD}{n+m} V_i = (1-M)DV_i \tag{39}$$

$$I_{Q2} = \frac{1}{(n+m)T}\left[n\int_{DT} 0\ dt + m\int_{(1-D)T} I_L dt + m\int_{T} I_L dt\right] = \left[1-(1-M)D\right] I_L \tag{40}$$

Thus, in steady-state condition, the average current flowing though the MOSETs is related to the averaged values of the inductor current as follows:

$$I_L = \frac{n+m}{nD} I_{Q1} = \frac{n+m}{n+m-nD} I_{Q2} \tag{41}$$

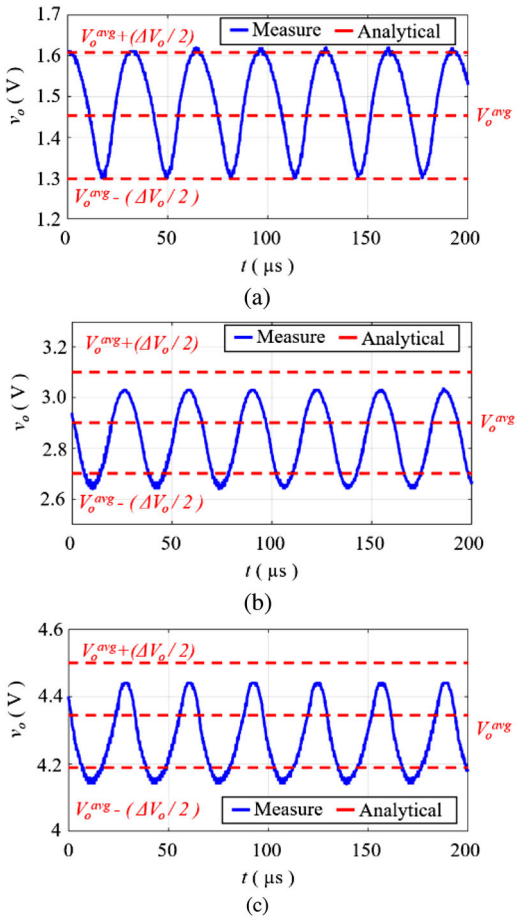

FIGURE 8 Comparison between the measured output voltage and the proposed DC output voltage V_o^{avg} and ripple equations ΔV_o. (a) Case A, $n = 8$. (b) Case B, $n = 16$. (c) Case C, $n = 24$

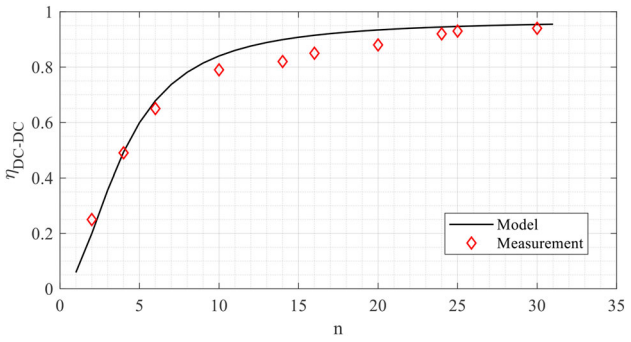

FIGURE 9 DC–DC Buck conversion efficiency. Theoretical efficiency by the model (black line) is compared with experimental measurements for different numbers of pulses n. The total number of pulses n_{max} is 32

The RMS currents through MOSFETs Q_1 and Q_2 are

$$I_{Q1}^{rms} = \sqrt{\frac{1}{(n+m)T}\left[n\int_{DT} I_L^2 dt + m\int_{(1-D)T} 0dt\right]}$$
$$= I_L\sqrt{\frac{nD}{n+m}} \tag{42}$$

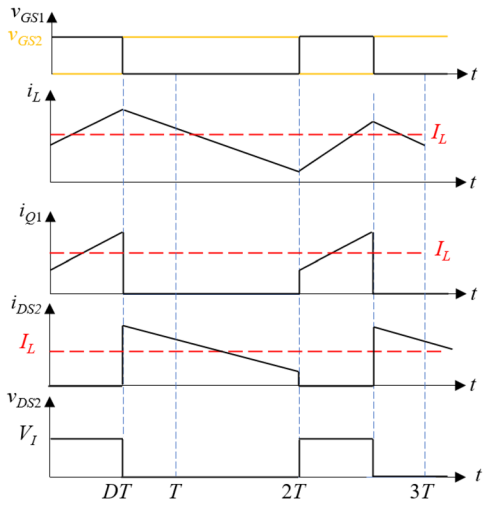

FIGURE 10 Current and voltage waveforms assuming $M = 3$, $n = 2$ and $m = 1$

$$I_{Q2}^{rms} = \sqrt{\frac{1}{(n+m)T}\left[n\int_{DT} 0dt + m\int_{(1-D)T} I_L^2 dt\right]}$$
$$= I_L\sqrt{\frac{n(1-D)+m}{n+m}} \tag{43}$$

Therefore, the power losses due to the parasitic resistances r_{DS1}, r_{DS2} are

$$P_{rDS1} = r_{DS1}\left(I_{Q1}^{rms}\right)^2 = r_{DS1}\left(I_L\sqrt{\frac{nD}{(n+m)}}\right)^2$$
$$= \frac{nD}{(n+m)} r_{DS1} I_L^2 \tag{44}$$

$$P_{rDS2} = r_{DS2}\left(I_{Q2}^{rms}\right)^2 = r_{DS2}\left(I_L\sqrt{\frac{m(1-D)}{(n+m)}}\right)^2$$
$$= \frac{n(1-D)+m}{n+m} r_{DS2} I_L^2 \tag{45}$$

Thus, in the small-signal model, the effect of the conduction resistances of the MOSFETs can be considered through two equivalent resistances

$$r_{DS1}^{eq} = (1-M)Dr_{DS1} \tag{46}$$

$$r_{DS2}^{eq} = (1-M)Dr_{DS2} \tag{47}$$

These two resistances are in series with the inductance L and, therefore, flowed by the current i_L, as shown in Figure 11a.

To extrapolate the small-signal model, perturbations close to the operating point, that is, $i_L = I_L + i_l$ and $v_I = V_I + v_i$ and $d_T = D + d$ are considered. To obtain a linear model, it is assumed that higher order terms, such as $i_l \cdot v_i$, $i_l \cdot d$ and $v_i \cdot d$, are negligible. Under this assumption, the current through Q_1

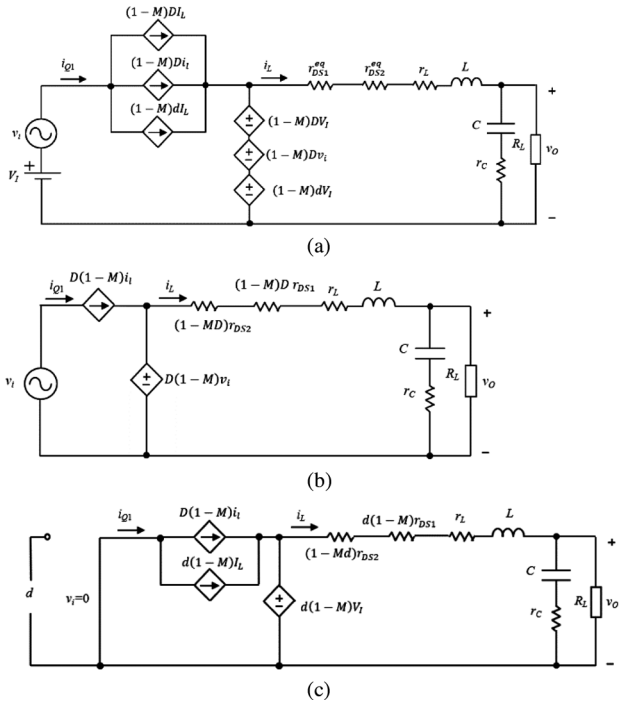

FIGURE 11 Small signal models diagrams. (a) Small signal model. (b) Equivalent circuit for voltage transfer function M_v. (c) Equivalent circuit for control transfer function T_p

is expressed as

$$\begin{aligned} i_{Q1} &= (1-M)d_T i_L = (1-M)(D+d)(I_L+i_l) \\ &\cong (1-M)DI_L + (1-M)Di_l + (1-M)dI_L \end{aligned} \quad (48)$$

Thus, MOSFET Q_1 is replaced with three controlled current sources in parallel, as shown in Figure 11a. Using the same approach, the drain-to-source voltage of Q_2 is

$$\begin{aligned} v_{DS2} &= (1-M)d_T v_I = (1-M)(D+d)(V_I+v_i) \\ &\cong (1-M)DV_I + (1-M)Dv_i + (1-M)dV_I \end{aligned} \quad (49)$$

Thus, the voltage across Q_2 can be modelled by three controlled voltage sources in series as shown in Figure 11a.

The linear equivalent circuit shown in Figure 11a contains the information both during the steady-state and under perturbations close to the operating condition.

4.2 | Voltage transfer function $M_V(s)$

Starting from the small-signal model shown in Figure 11a, the voltage transfer function M_V can be calculated letting the perturbations $d = 0$. The equivalent network is shown in Figure 11b. To compute the transfer function, the KVL is applied to the circuit in Figure 11b in the Laplace domain,

TABLE 1 Operating conditions

Ref.	Description
[16]	Comparison of conversion efficiency of a Flyback converter operating with PWM and PSM.
[17]	Analysis of Buck converter operating with PSM. Derivation of voltage transfer function and output voltage ripple and efficiency. All the parasitic of passive components are neglected.
[18]	Voltage mode digital control. Particular attention is placed on the stability analysis and the small signal model derivation. A derivation of the output voltage ripple is provided as a function of the reference voltage of the closed loop.
[19]	A Buck converter operating with variable duty cycle PSM is presented. The discrete time model is derived and the associated small-signal model is carried out.
[20]	PSM digital control of Buck converter. Derivation of the output voltage ripple neglecting the parasitic components.

TABLE 2 Operating conditions

Parameter	Value
Operating frequency f	1 MHz
Duty cycle D	0.5
Number of pulses n_{tot}	32
Input voltage V_I	12 V
Load resistance R_L	2.62 Ω

obtaining

$$D(1-M)V_i(s) = \left(r_{DS1}^{eq} + r_{DS2}^{eq} + r_L + sL\right) I_L(s) + V_o(s) \quad (50)$$

Applying the KCL to Figure 11b

$$I_L(s) = \frac{V_o(s)}{r_C + \frac{1}{sC}} + \frac{V_o(s)}{R_L} = \frac{1 + s(R_L + r_c)}{R_L(1 + sr_cC)} V_o(s) \quad (51)$$

Substituting (51) into (50), the voltage transfer function expression is derived

$$M_v(s) = \frac{V_o(s)}{V_i(s)} = \frac{D(1-M)R_L(1+sr_CC)}{s^2\tau L + s(L + R_Lr_CC + \alpha\tau) + R_L + \alpha} \quad (52)$$

where $\alpha = (1-MD)(r_{DS1}+r_{DS2})$ and $\tau = (R_L+r_C)C$.

The validation of the obtained transfer function has been performed using the operating conditions shown in Table 1 and the parasitic resistances shown in Table 2.

The magnitude and the phase Bode plots of the predicted and simulated output voltage transfer functions are shown in Figures 12a and 12b, respectively. The Mv poles and the zero are summarized in Table 7.

Since the frequency of a single pulse is $f = 1$ MHZ, while the number of periods of the PSM is $n + m = 16$, the Buck effective operating frequency is $f_{PSM} = f/(n + m) = 62.5$ kHz. Since the SMM ensures accurate results until $f/2$ [28, 29], the Bode plots

TABLE 3 Mounted components on the developed board

Parameter	Description	Value
Inductor L	NS12575T470MN By Taiyo Yuden	$L = 46.3\ \mu$H $r_L = 62.3\ \text{m}\Omega$ at 1 MHz
Output capacitor C	GRM32ER7YA106KA By Murata	$C = 9.84\ \mu$F $r_C = 12.2\ \text{m}\Omega$ at 1 MHz
MOSFETs Driver	TPS28225 By Texas Instruments	–
PWM/PSM Controller	ESP32-WROOM-32D	Dual-Core SoC $f_{clk} = 240$ MHz Flash 4 MB Wi-Fi Bluetooth
Current sensor	INA219	12 Bits I^2C Protocol
MOSFETs Q_1, Q_2	BSO150N03 By Infineon	$r_{DS} = 18.2\ \text{m}\Omega$
Load resistance R_L	RT055AS3300KB By Vishay	$R_L = 2.62\ \Omega$

TABLE 4 Analysed operating conditions

Case	Operating condition	Load resistance	Pulses
A	$V_I = 12$ V	$R_L = 2.62\ \Omega$	$n = 8$ $m = 24$
B	$V_I = 12$ V	$R_L = 2.62\ \Omega$	$n = 16$ $m = 16$
C	$V_I = 12$ V	$R_L = 2.62\ \Omega$	$n = 24$ $m = 8$
D	$V_I = 12$ V	$R_L = 2.62\ \Omega$	$n = 31$ $m = 1$

TABLE 5 Comparison of DC and ripple output voltage

Par.	Case	Proposed	Ref. [17]	Ref. [18]	LTspice	Exp.
ΔV_o	A	0.31 V	0.23 V	0.29 V	0.32 V	0.32 V
	B	0.42 V	0.21 V	0.38 V	0.43 V	0.41 V
	C	0.33 V	0.08 V	0.25 V	0.32 V	0.28 V
	D	0.05 V	0.03V	0..03 V	0.05 V	0.05 V
$\Delta V_o\%$	A	21.3%	15.3%	19.5%	21.6%	21.9%
	B	14.4 %	7.0%	12.8%	14.4%	14.5%
	C	7.6%	1.7%	5.6%	7.2%	6.5%
	D	1.02%	0.06%	0.51%	0.89%	0.94%
V_o	A	1.45 V	1.50 V	1.49 V	1.48V	1.46 V
	B	2.90 V	3.00 V	2.98 V	2.97 V	2.82 V
	C	4.34 V	4.50 V	4.46 V	4.46 V	4.31 V
	D	5.60 V	5.81 V	5.80 V	5.76 V	5.56 V

of the transfer functions are shown until the frequency $f_{max} = 100$ kHz. This frequency is sufficient to properly design a controller. To further validate the voltage transfer function, a time domain simulation was performed considering the three cases $\{n = 12, m = 4; n = 8, m = 8; n = 4, m = 12\}$ and compared against the step response of the small signal transfer function shown in (52). The comparison can be seen in Figure 13.

TABLE 6 Inductor current ripple

Parameter	Case	Estimated by (24)	Simulated
ΔI_L	A	750 mA	800 mA
	B	1010 mA	1100 mA
	C	790 mA	840 mA
	D	178.8 mA	186.6 mA

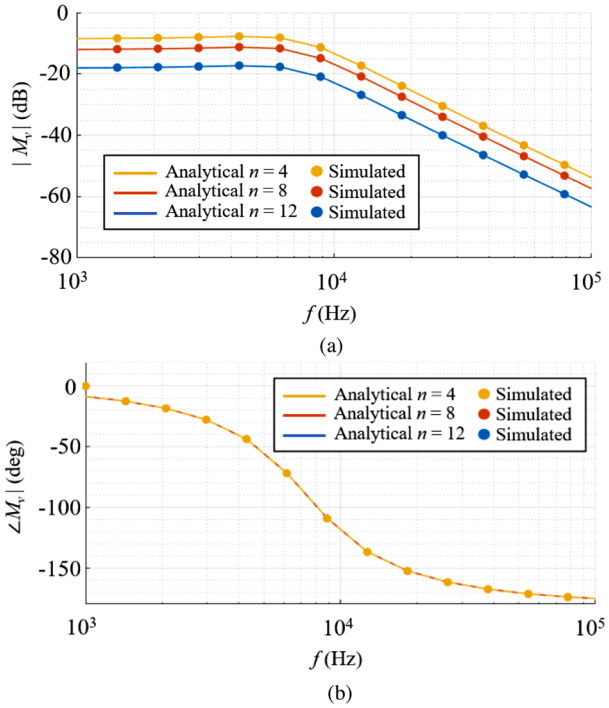

FIGURE 12 Bode plots of the input-to-output voltage transfer function $M_v = v_0/v_i$. (a) Magnitude plot. (b) Phase plot

TABLE 7 Zero and poles of voltage transfer function

Zero and poles	Operating condition
Zero Z_1	-8.1967×10^6
Pole P_1	$(-2.5640 + 3.9028\text{i}) \times 10^4$
Pole P_2	$(-2.5640 - 3.9028\text{i}) \times 10^4$

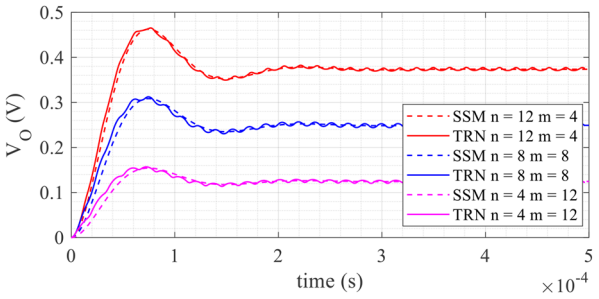

FIGURE 13 Comparison of the unitary step response for the small signal voltage transfer function (dashed line) and time domain transient simulation (continuous line) of the converter

TABLE 8 Zero and poles of control transfer function

Zero and poles	Operating condition
Zero Z_1	-8.1967×10^6
Pole P_1	$(-2.5834 + 3.9147i) \times 10^4$
Pole P_2	$(-2.5834 - 3.9147i) \times 10^4$

4.3 | Control transfer function $T_p(s)$

The control-to-output transfer function is calculated letting the $v_i = 0$. The linear model is shown in Figure 11c. Applying the KVL to the circuit one obtains

$$D(s)(1-M)V_I = \left[(1-M)D(s)r_{DS1} + (1-MD(s))r_{DS2} + r_L + sL\right]I_L(s) + V_o(s) \quad (53)$$

Using (49) in (51)

$$D(s)(1-M)V_I = \left\{\left[(1-M)D(s)r_{DS1} + (1-MD(s))r_{DS2} + r_L + sL\right]\frac{1+s\tau}{R_L(1+sr_CC)} + 1\right\}V_o(s) \quad (54)$$

Neglecting the higher order terms $V_o(s) \cdot D(s)$, the control-to-output voltage transfer function is obtained as follows:

$$T_d(s) = \frac{V_o(s)}{D(s)} = \frac{(1-M)V_IR_L(1+sr_CC)}{s^2\tau L + s\left[(r_{DS2}+R_L)\tau + L + r_CR_LC\right] + r_{DS2} + R_L + r_L} \quad (55)$$

The poles and the zero using the values shown in Tables 1 and 2 are summarized in Table 8. The magnitude and the phase Bode plots of the predicted and simulated transfer function are shown in Figures 14a and 14b respectively.

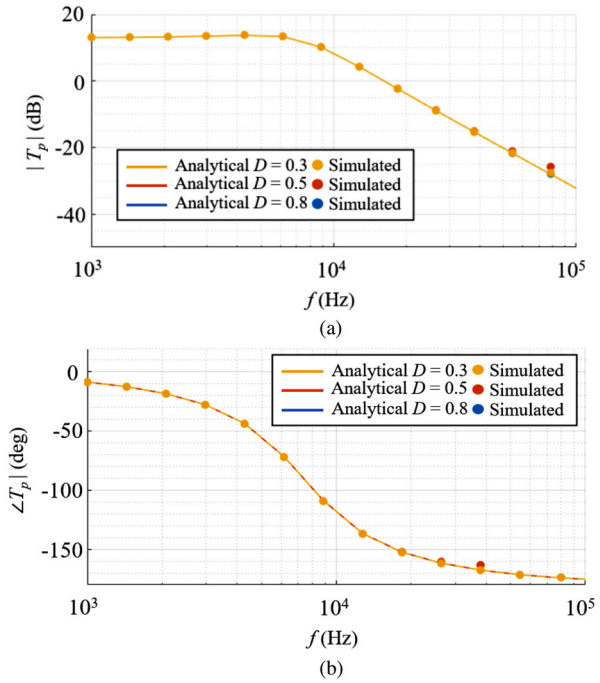

FIGURE 14 Bode plots of the control transfer function $T_p = v_0/d$. (a) Magnitude plot. (b) Phase plot

5 | CONCLUSIONS

In this work, an accurate model representing a buck converter driven by PSM is presented. The major contributions of the paper are summarized as follows:

a. An analytic derivation of the voltage transfer function considering the parasitic elements.
b. A state-space representation of the system to describe the transient and steady-state responses by using numerical integration.
c. An accurate estimation of the output voltage and inductor current, in terms of both ripple and DC values. From these results, design equations for the converter are proposed and extensively validated through experimental results, highlighting the improvements of the proposed model with respect to the approaches found in literature.
d. Derivations of the average DC and AC small-signal linear time-invariant model of the PWM Buck converter in continuous conduction mode by the circuit averaging technique.
e. Derivations of the small-signal input voltage-to-output voltage and duty-cycle-to-output voltage transfer functions.

As future development, the proposed analysis will be used to analyse different converter topologies operating with PSM.

CONFLICT OF INTEREST

The authors declare no conflict of interest.

DATA AVAILABILITY STATEMENT

Data sharing not applicable – no new data generated.

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