GaAs MMIC switch for high speed applications

show the best performance with a DC-current gain of 5.3 and an f_t of ~18GHz at 18K. The analysis of the DC and high-frequency data of the THETA structure at cryogenic temperatures indicate a lower output conductance, lower leakage current, higher current gain, and lower base-emitter capacitance.

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GaAs MMIC switch for high speed applications

G.F. Avitabile and A. Cidronali

Indexing terms: MMIC, Gallium arsenide, Switches

An MMIC switch for fast sampling applications is described. The proposed structure, along with the design procedure are discussed. MESFET based prototype measurements are reported.

Introduction: Fast sampling circuits are widely used in sampling oscilloscopes, digital receivers [1], and so on. Common requirements for these applications are low insertion loss, fast recovery time and high isolation. These requirements are normally met with a design based on a diode bridge sampling gate, which is always arranged in a balanced configuration. In fact, a fully differential command of the sampling gate minimises the feedthrough, reducing the jitter aperture, the commutation pedestal and the settling time all at the same time.

A number of different passive and active configurations which provide an adequate driving signal may be found [2, 3]. The use of passive baluns suffers several limitations, mostly due to their intrinsic passband response (i.e. the output has non-DC content) and due to the troublesome integration of such structures. Conversely, active structures usually rely on digital circuits for balanced pulse generation. As a consequence, problems can be expected where a sample-to-hold ratio different from unity is required.

In this Letter, a fast sampling MMIC switch is described which is based on an original active transformer that accepts as sampling trigger an unbalanced pulse with arbitrary duty cycle.

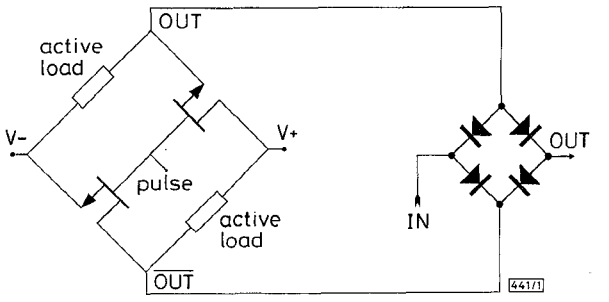

Fig. 1 *Schematic diagram of MMIC switch*

Basic operations: A schematic diagram of the switch is shown in Fig. 1. The upper block is a standard MES-diode sampling gate, $D_{1,2,3,4}$, that ensures, as stated before, good isolation and fast switching characteristics if driven by an accurately balanced pulse.

Because the switch is mainly conceived for digital receiver applications, an ON-to-OFF ratio of much less than unity must be assumed, thus requiring the use of pulse sources which have a typically unbalanced output. As a consequence, proper switch operations require a pulse transformer to drive the bridge. This transformer must cover a multiple octave bandwidth with a low-pass transfer function, in order to preserve the DC content of the pulse signal, which, in turn, ensures correct balance of the diode bridge.

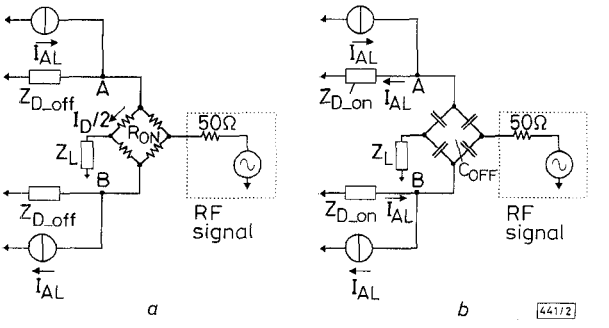

Fig. 2 *Equivalent circuit of switch*

a During ON state
b During OFF state

A schematic diagram of the balanced pulse transformer is sketched in the lower block of Fig. 1. The four MESFETs are arranged in a classical Wien bridge configuration. The bridge is anti-symmetrical with respect to the vertical diagonal; the two elements driven by the driving pulse unbalance the bridge and generate a differential voltage which appears across the opposite diagonal of the bridge. The active pulse transformer requires two active loads each implemented by a single MESFET with the gate shorted to the source or by two MESFETs in single-cascode self bootstrapped configuration [4].

Typical diode bridges are efficiently driven with a few milliampere current, I_D, and without offset pedestal. In the sample mode (Fig. 2*a*), the diode bridge can be modelled using four resistors, R_{ON}, whose value is determined by the $I_D/2$ current supplied by the generator.

Let us consider, in the ON mode, that the pulse transformer active loads are represented by ideal current generators, I_{AL}. The two driver MESFETs are biased in their pinch-off regions. In such conditions, I_D equals I_{AL}. As a consequence, the equivalent impedance seen by the bridge diodes is several orders of magnitude

higher than their dynamic impedance. No feedthrough from the radio frequency source to the transformer is theoretically expected, thus minimising the insertion loss. I_{AL} defines the active load MESFET size. Assuming that I_D is the value needed to drive in the sample mode, the diode bridge and I_{DSS} is the drain to source saturation current, then

$$N_{AL}W_{AL}I_{DSS} = I_D \quad (1)$$

where N_{AL} = number of fingers and W_{AL} = gatewidth.

During the OFF mode (Fig. 2*b*), the active loads work in their saturation region and the current flows through the two driver MESFETs, now biased in their linear region. The potential of B is forced to zero with respect to A. The diodes are off and replaced by their junction equivalent capacitances, C_{OFF}. The driver MESFETs are designed to work in their linear region and could be represented by an equivalent impedance, Z_{D_OFF}, which is negligible with respect to the impedance of the diode bridge, due to C_{OFF}. Following the above technique, the residual feedthrough is shunted to ground via the small drive impedance increasing the RF port to IF port isolation. The size of the driver MESFETs must satisfy the following relation:

$$N_{DRIVE}W_{DRIVE}I_{DSS} > I_D \quad (2)$$

Design and experiments: Some prototypes of the switch have been designed and tested using the GEC-Marconi F20 process. Active loads have been implemented by using a single MESFET with the source shorted to the gate. Transistor sizes were determined using eqns. 1 and 2. Assuming a 10mA total bridge current and I_{DSS} = 150mA/mm, the active load size is defined by: N_{AL} = 2 and W_{AL} = 33μm, while for the two driver MESFETs the parameters are: N_{DRIVE} = 2 and W_{DRIVE} = 50μm. The diode bridge has been implemented by four MES-diodes with a 2 × 20μm size (the equivalent circuit values are: R_{ON} = 10Ω and C_{OFF} = 40fF). The performance of the proposed circuit has been tested using a chip-and-wire technology to connect the MMIC prototype to a 254μm RT/Duroid 6502 plastic substrate test fixture. In Fig. 3*a*, the insertion loss in the ON mode is compared with the theoretical results reported in [5] for a conventional FET switch. Fig. 3*b* reports the same comparison for isolation during the OFF state. The experiments show an isolation better than –25dB, up to 20GHz. This result represents a significant improvement in the isolation characteristics in comparison to single stage (i.e. nonmultiple cascaded switch cells) conventional designs. To test the active pulse transformer, an input unbalanced pulse was used, with 4ns period, 7% duty cycle and a 100ps rise-time (–50 to –950mV) and 9 × 10^3 mV/ns slew rate. The characterisation was obtained using the HP54121T (17.5p rise time) sampling oscilloscope, and a couple of active high-impedance probes sensing the two diode bridge control points, A and B in Fig. 2*b*. Fig. 4 shows the balanced waveform; the rise time is 50ps and the voltage swing is consistent with the diode threshold. The output waveform has a very low offset bias (<50mV) determined by the presence of two further diodes, connected to the negative bias supply. These diodes prevent the circuit to be damaged by the typical overshot generated by the SRD pulse sources.

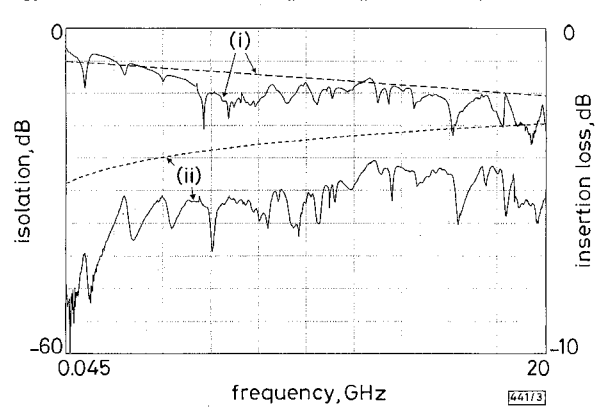

Fig. 3 *Comparison between measures and data in* [5]

(i) insertion loss in ON state
(ii) isolation in OFF state
——— measured
– – – – data in [5]

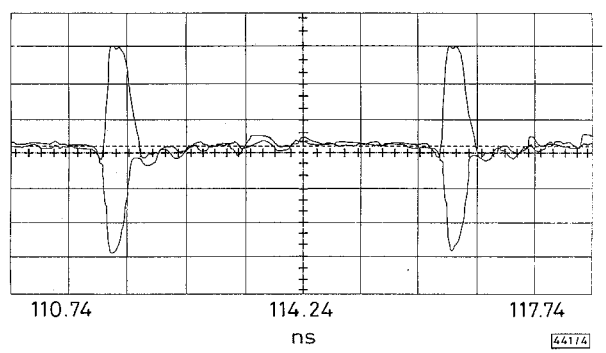

Fig. 4 *MMIC pulse transformer output waveforms*

200mV/div vertical scale, 700ps/div. horizontal scale
Ch.2: 200mV/div., Ch. 3: 200mV/div.
Timebase: 700ps/div., delta V = 565mV, Vmarker 1 = 40mV
Offset = 0V, delay = 110.74ns, Vmarker 2 = 605mV
Trigger on external pos. edge at 714mV

Conclusion: The MMIC proposed exhibits an enhanced isolation up to 20GHz during the OFF state, preserving those characteristics which are consistent with conventional FET designs during ON state. This improved performance is obtained while maintaining a reduced chip area (0.778 × 0.778mm for the prototype reported).

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High frequency GaInP/GaAs heterostructure-emitter bipolar transistor with low offset voltage

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Indexing terms: Bipolar transistors, Heterojunction bipolar transistors

A carbon doped GaInP/GaAs heterostructure-emitter bipolar transistor (HEBT) grown by MOCVD is reported with high RF performance. A cutoff frequency of 50GHz and maximum oscillation frequency of 90GHz were obtained for the device. An offset voltage as low as 90mV was achieved. It is shown that the GaInP/GaAs HEBT with a high frequency and a low offset voltage is a good candidate for low battery power device applications.

Introduction: Heterojunction bipolar transistors (HBTs) are attractive for microwave and power applications because of their high