Ultra Low-Power Vco Based On InP-Hemt And Heterojunction Interband Tunnel Diode For Wireless Applications

Ultralow DC Power VCO Based on InP-HEMT and Heterojunction Interband Tunnel Diode for Wireless Applications

Alessandro Cidronali, *Member, IEEE*, Giovanni Collodi, *Member, IEEE*, Matteo Camprini, Vijay Nair, *Fellow, IEEE*, Gianfranco Manes, *Senior Member, IEEE*, J. Lewis, *Member, IEEE*, and Herb Goronkin, *Fellow, IEEE*

***Abstract*—The monolithic integration of tunneling diodes (TDs) with other semiconductor devices such as high electron-mobility transistors (HEMTs) or HBTs, creates novel quantum functional nonlinear devices and circuits with unique properties: the negative differential resistance and the extremely low dc power consumption. In this paper, we present a family of InP-HEMT-TD-based voltage-controlled oscillators operating in the 4–6-GHz band suitable for wireless applications, along with an effective analytical treatment of the stability issues. Prototypes having different circuit topologies of HEMT-TD devices have been designed and fabricated. The circuits generated an output power in the range of −11 to −18 dBm when operated at a bias current of 1.75 mA at 500 mV. Phase noise characteristics and tuning capability of the circuit configuration have been experimentally determined. The maximum tuning range of 150 MHz and the maximum single sideband-to-carrier ratio of −97 dBc/Hz at 200 kHz have been achieved.**

***Index Terms*—Microwave voltage-controlled oscillator (VC), monolithic microwave integrated circuit (IC), quantum-well device.**

I. Introduction

THE increasing demand for smaller, faster, and low-power consumption systems has created a remarkable opportunity for innovative semiconductor devices, integrated circuits (ICs), and wireless systems. One of the new technologies capable of to meeting such requirement is based on the incorporation of quantum devices (QDs) in the circuits [1]. QDs like tunneling diodes (TDs) have demonstrated the potential for highest speed–lowest power consumption operation. Several microwave circuits using QDs have been demonstrated: bidirectional amplifier [2], mixer [3], [4], frequency multiplier [5], and oscillator [6]. A fundamental building block that has received high consideration since the earliest microwave system development is the sinewave oscillator. Solid-state three-terminal device-based oscillators were not optimized and tunnel diode oscillators represented a good choice. However, these circuits are not quite suitable for wireless products due to their high power consumption and large physical size. On the contrary, low-power consumption monolithic voltage-controlled oscillators (VCOs) are required for portable communication products. A second very important issue is that the phase noise characteristic of free-running oscillators based on tunnel devices reported up to now are slightly worse than those reported with conventional technology. Systematic theoretical investigation of phase noise mechanism of negative differential resistance (NDR) devices and experimental data on tunnel diode VCOs incorporating a phase-locked loop (PLL) system are not yet available. Significant research effort in this field is expected in the coming years. This paper introduces the relevant issues related to the design of VCOs by the use of three-terminal NDR-devices for low-power applications along with an experimental demonstration of the technology capability. It is demonstrated that the unique features of such class of devices enable the realization of signal sources with the lowest bias voltage and dc power consumption with a reasonable high efficiency and with a fairly good level of phase noise. Due to excellent maximum operative frequencies as previously reported, the three-terminal NDR device appears as a suitable alternative to conventional implementation of ultra low power signal source.

This paper is organized as follows. The description of the quantum microwave monolithic integrated circuit (QMMIC) technology, which is the basis of the developments presented here, is given in Section II. In Section III, an effective analytical treatment concerning the mechanism generating instability and undesired or spurious oscillations on the basis of a simple equivalent circuit model is discussed. The guidelines for the proper use of such devices in microwave oscillators and other negative resistance circuits are also given. Finally, in Section IV, the microwave performance of two different topologies of ultralow-power VCOs is reported. The VCOs consisted of an InP heterojunction interband tunneling diode (HITD) monolithically integrated with an HEMT forming the heterojunction interband FET (HITFET). In particular, the two VCO prototypes were implemented by using the same HITFET in common-drain and in common-source configurations. The experimental results are compared with respect to the tuning capability, the output power, and the phase noise.

II. QMMIC Technology

There are many types of tunnel diodes such as interband homojunction type diodes, interband heterojunction tunnel diodes [7] or intraband resonant tunneling diodes [8]. They have been

Manuscript received April 5,2002; revised August 26, 2002.

A. Cidronali, G. Collodi, M. Camprini, and G. Manes are with the Department of Electronics and Telecommunications, University of Florence, Firenze 50139, Italy (e-mail: acidronali@ing.unifi.it).

V. Nair, J. Lewis, and H. Goronkin are with the Physical Sciences Research Laboratory, Motorola Laboratories, Tempe AZ 85284 USA.

Digital Object Identifier 10.1109/TMTT.2002.805288

TABLE I
HITFET LAYER STRUCTURE

p^+ InGaAs	Top Contact Layer (Anode)	HITD
nid InAlAs	Barrier	
nid InGaAs	Well	
n^{++} InAlAs	Barrier	
n^+ InGaAs	Bottom HITD Contact Layer (Cathode), HFET Ohmic	
nid InAlAs	Schottky contact (Gate)	HFET
n InGaAs	Si δ-doping	
nid InAlAs	Spacer	
nid InGaAs	Channel	
nid InAlAs	Buffer	
InP	Substrate	

realized in many different material systems. The basic device characteristics of all of them, however, are similar. HITDs allow the highest peak–valley current ratio and an excellent cut-off frequency and HFET on lattice-matched structure on InP offers high-frequency operation at low voltages.

The semiconductor layer structure of the HITD and HEMT which give rise to the QMMIC technology adopted here is shown in Table I. It is grown by the MBE technique and wafers are selectively etched to obtain the two devices. They can be realized in an integrated version, realizing the HITD directly on the drain contact of the HEMT obtaining a vertical monolithically integrated transistor like the one in [6]–[9]. Although in principle the HITD can be placed directly on either the gate or the source electrodes, these solutions give a difficult control of the *I-V* characteristic, making them not suitable for practical circuit applications and will not be considered further.

The solution adopted in this work consists of interconnecting the two devices, i.e., the HITD and the HEMT, as it is conventionally made for two or more elements of the same circuit. The result is a novel NDR device having three terminals called HITFET. The third terminal is used as gate control [6]. The integration of the HITD in series to the drain electrode realizes the drain-HITFET. Without any further specification, in this paper the HITFET's drain voltage is defined as the voltage applied to the anode of the HITD, while its cathode is connected to the drain of the HFET.

The HEMTs used in this study operated at an Id_{ss} of about 200 mA/mm at $V_{ds} = 2.0$ V. They achieved cut-off frequencies in the range of 70 GHz. The HITDs have shown very high current densities (50-60 KA/cm^2) and peak-to-valley ratios between 10 and 15 [7]. Analysis of microwave performance shows a maximum frequency of oscillation to be around 60 GHz for a 2.5×2.5 μm^2 diode. Since the HITFET operates as a three-terminal voltage-controlled NDR, the maximum operative frequency is not related to the power gain but to the NDR cut-off. The devices used in the design of the prototype circuits exhibited a maximum frequency of about 30 GHz at the bias point of $Vd = 500$ mV and $Vg = 0$ V.

The current–voltage characteristics of a drain-HITFET is shown in Fig. 1. The bias voltage spans from 0 to 1 V while the gate control voltage spans from 0 to -0.8 V (at steps of 100 mV). The shift of the NDR region toward higher drain bias voltage is observed as the gate bias magnitude is increased. For gate voltages close to 0 V, an increase in the magnitude of the NDR region is also observed. This results in a cut-off frequency decrease as the gate bias changes from 0 V to a

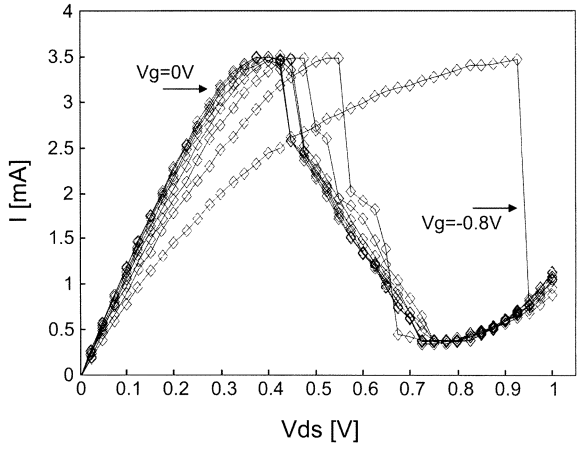


Fig. 1. *I–V* characteristic of the HITFET. $V_g = 0$ to -8 V in steps of 100 mV.

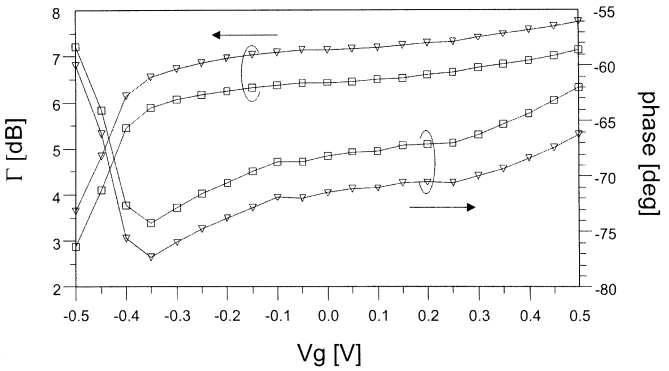


Fig. 2. Drain-HITFET's reflection coefficient as seen from the source terminal for the common-drain (square) and from the drain for the common-source (triangle) configuration at 6. 2 GHz, V_d =500 mV, as a function of the gate control voltages.

pinch-off voltage due to the increase in drain-source resistance of the HEMT that is in series with the HITD. The HEMT also introduces reactive components that modify the self-resonant frequency slightly. At the gate bias voltage of $Vg = -0.8$ V, the characteristic becomes strongly discontinuous and the NDR vanishes completely. The increasing value of the drain-source resistance associated with the HEMT device, which is in series with the HITD, moves the onset of the HITFET NDR region to a higher drain voltage. The overall effect is a reduction of the peak–valley voltage range. As the NDR voltage range decreases, the negative differential resistance approaches zero and the HITFET is no longer functional.

In Fig. 2, the dependence of reflection coefficient Γ of the drain-HITFET as seen from the source terminal, i.e., in common-drain configuration, and from the drain terminal, i.e., in common-source configuration, is plotted as a function of the gate control voltages. The measured Γ is greater than 1 due to the NDR associated with the diode. The two configurations exhibit a slight difference in the magnitude of roughly 1 dB, and this is due to the effect of the HEMT capacitance between the gate and source which is responsible for a signal leakage that is more effective in the common-drain configuration. In fact, it is possible to tailor the size of the HITD or, equivalently, to increase the peak current by increasing the doping profile in order to reduce the NDR magnitude. A higher value of Γ

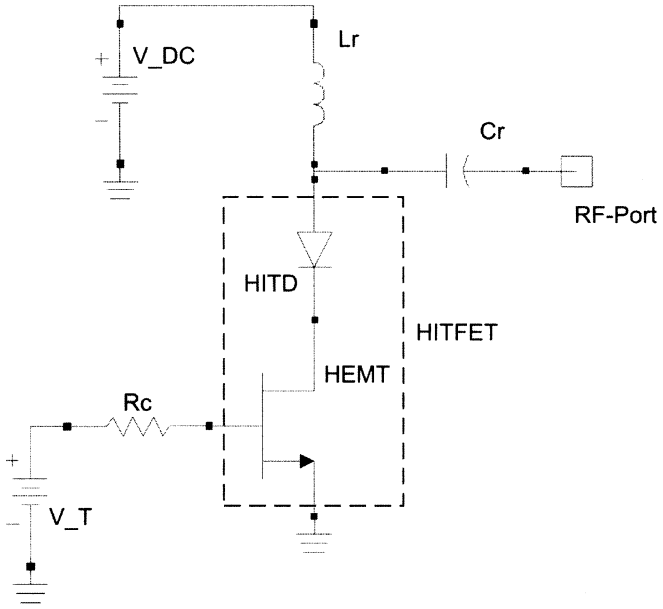


Fig. 3. Common-source HITFET-based VCO circuit schematic.

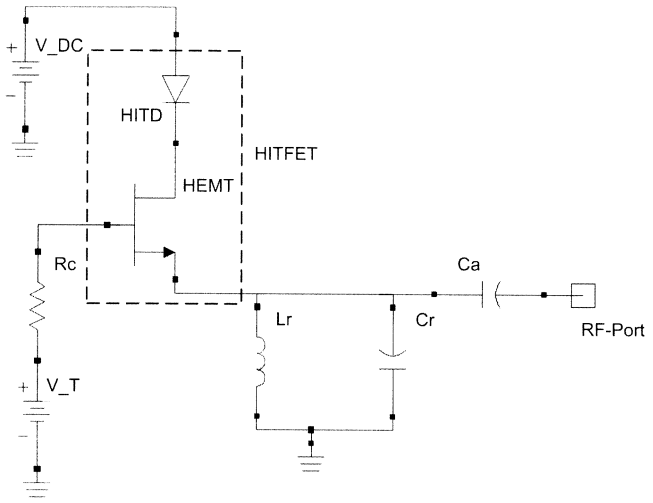


Fig. 4. Common-drain HITFET-based VCO circuit schematic.

could be achieved at the expense of an increased parasitic junction capacitance and reduced cut-off frequency. A proper choice of the NDR is necessary to meet the requirement of high-frequency operation and a high Γ value that provides enough margins to satisfy the oscillation condition. The phase swing of Γ depends mainly on the variation in the drain-source to channel capacitance. The effect due to the HITD junction capacitor is minimal since it is an order of magnitude lower.

III. Analytical Treatment of the HITFET Stability

The HITFET-based VCOs are implemented by introducing a lumped element resonator in the two possible configurations: common-source (CS) or common-drain (CD). The schematics of the two configurations are shown in Figs. 3 and 4, respectively. In both, the topologies the HITFET is tuned by an external control voltage V_T, while a simple *LC* resonator fixes the oscillation frequency.

The insertion of external impedance in series to a tunnel diode faces a number of problems in terms of low frequency and short circuit stability [10], [11], which are discussed below with the help of a simple but effective analytical treatment. For this purpose, the drain-HITFET represented in Fig. 5(a) is modeled as shown in Fig. 5(b). The model has been derived under the assumption that the HEMT within the HITFET, as the effect of the series connection with the HITD, is biased at a drain-source voltage of a few tens of millivolts; this makes the transconductance negligible with respect to the HEMT output conductance. The drain-gate and gate-source capacitances are also neglected because they are in series with a 1-KΩ gate resistance. The HITDs used in the circuit had an area of 2.5×2.5^2 μm and the HEMT had two gate fingers of 25-μm unit width. The operating bias voltages were $Vg = 0$ V and $Vd = 0.5$ V for the gate and the drain of the HITFET, respectively, and the corresponding drain current was 1.7 mA. The complete model parameters are $R_s = 6.4\ \Omega$, $L_s = 0.187$ nH, $R_{ds} = 17.3\ \Omega$, $C_{ds} = 0.2$ pF, $R_d = 190\ \Omega$, and $C_d = 0.11$ pF. In the Laplace domain, the voltage-Kirchoff law of the circuit in Fig. 5(b) is $V_d(s) = Z_H(s) \cdot I_d(s)$. The HITFET is short-circuit stable if the impedance $Z_H(s)$ has no zeros in the right half of the s plane. After mathematic manipulation, the impedance can be expressed as

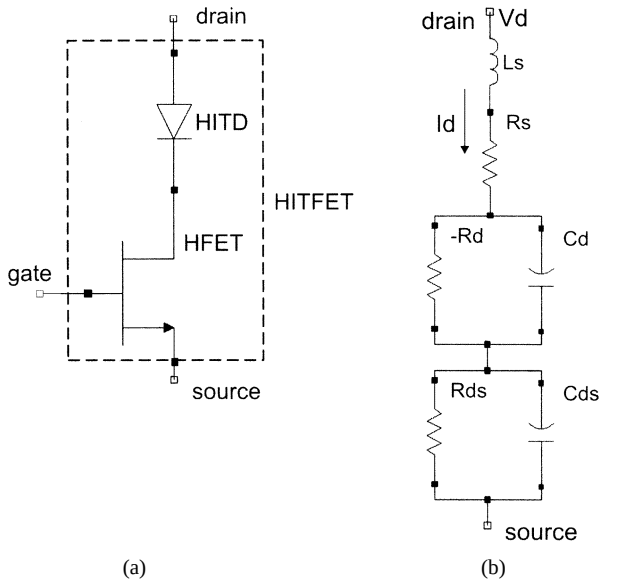


Fig. 5. (a) Schematic representation of the HITFET. (b) Equivalent circuit model adopted for the analytical treatment of the stability.

$$Z_H(s) = (-L_s R_d C_d R_{ds} C_{ds}) \frac{N(s)}{D(s)} \tag{1}$$

where $D(s) = (1 - R_d C_d s)(1 + R_{ds} C_{ds} s)$. It turns out that the stability condition can now be imposed on $N(s)$ which can be written in the form

$$N(s) = s^3 + a_2 \cdot s^3 + a_1 \cdot s^2 + a_0. \tag{2}$$

The polynomial coefficients a_i are evaluated by the inherent time-constants and the self-resonance frequencies of the devices as follows:

$$\begin{aligned} a_0 &= \frac{\omega_d^2}{\tau_{ds}} - \frac{\omega_{ds}^2}{\tau_d} - \frac{1}{\tau_s \tau_{ds} \tau_d} \\ a_1 &= \omega_d^2 + \omega_{ds}^2 + \frac{1}{\tau_s \tau_{ds}} - \frac{1}{\tau_s \tau_d} - \frac{1}{\tau_{ds} \tau_d} \\ a_2 &= \frac{1}{\tau_s} + \frac{1}{\tau_{ds}} - \frac{1}{\tau_d} \end{aligned} \tag{3}$$

where

$$\begin{aligned} \tau_s &= \frac{L_s}{R_s} \quad \tau_d = R_d C_d \quad \tau_{ds} = R_{ds} C_{ds} \\ \omega_d^2 &= \frac{1}{L_s \cdot C_d} \quad \omega_{ds}^2 = \frac{1}{L_s \cdot C_{ds}}. \end{aligned} \tag{4}$$

From the analysis of (2), it is possible to write the necessary and sufficient conditions for the HITFET short-circuit asymptotical stability as

$$\begin{aligned} a_2 &> 0 \\ a_1 - \frac{a_0}{a_2} &> 0 \\ a_0 &> 0. \end{aligned} \tag{5}$$

Once the equivalent circuit parameters are evaluated, (5) determines whether the stability of a particular device is critical or not. The conditions in (5) are also useful if we want to investigate the stability issues with respect to variations of the equivalent circuit parameters or when a particular network is added to the circuit. Four cases are worth investigating.

A. Effect of Series Inductor

In circuits of practical interest, it is significant to assess the influence of a series choke inductor that is normally required to bias the device. It can be easily taken into account by substituting L_s with $\hat{L}_s = L_s + L$ in the above treatment, where L is the additional series inductor. In a state-of-the-art InGaAs-InAlAs HITFET, the capacitors C_d and C_{ds} have very close values; moreover, R_d for a well-designed device has to be much higher than R_{ds} and R_s, therefore the following further conditions are usually fulfilled:

$$R_d C_d - R_{ds} C_{ds} > 0; \qquad R_d > R_s + R_{ds}. \tag{6}$$

In the hypothesis that the HITFET itself (i.e., with $L = 0$) is short-circuit stable, only the second condition of (5) can be changed by the presence of an additional series inductor. The critical value of $\hat{L}_s$ is given by that equation: if L is further increased, the circuit becomes unstable and the frequency of oscillation decreases for increasing values of L. The calculation, comprising a load termination of 50 Ω, leads to a critical value of $L = 1.39$ nH. The output spectrums obtained through transient CAD simulations with different values of L_c are reported in Fig. 6. The simulations make use of previously developed nonlinear models of the HITD and HEMT [3]–[7]. The additional series inductor values were, respectively, L =1, 1.3, 1.5, and 1.8 nH. The absence of a significant spectral content in the case $L = 1$ nH demonstrates the accuracy of the analysis, since in this case the inductor value is lower than the critical value.

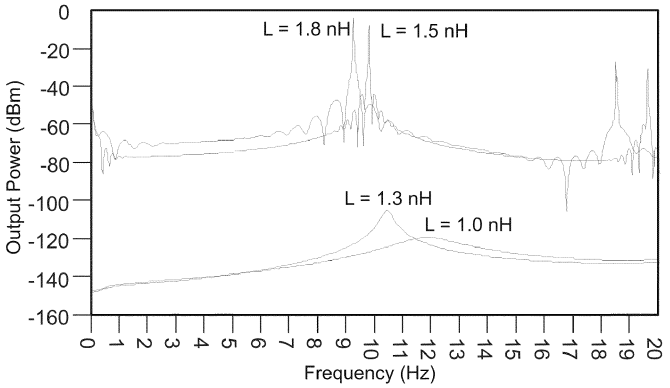


Fig. 6. Simulated output spectrum for L =1 and 1.3 nH (stable) and L = 1.5 and 1.8 nH (unstable).

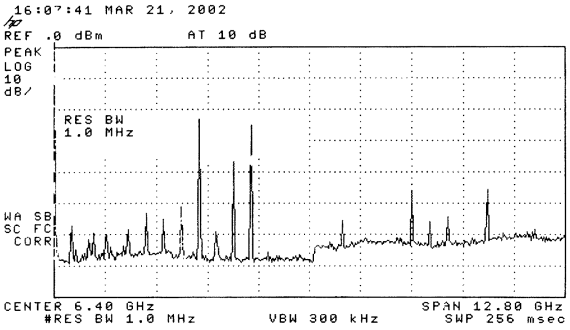


Fig. 7. Example of low-frequency unstable VCO output spectrum.

Fig. 7 reports the typical spectrum that arises from a low-frequency unstable HITFET if a resonator at the frequency of 6 GHz is connected to the device with the objective to obtain a single-tone generation: the intermodulation and the frequency shift of the main spectral content are the results of a described effect.

B. Effect of a Series Resistor

This case represents the practical situation of an uncertain ohmic loss evaluation or the presence of a resistive load termination. Equivalently to the previous case, R_s is replaced with $\hat{R}_s = R_s + R_l$, where R_l represents the additional resistance in the network. If the first condition of (6) is verified, the insertion of the series resistance increases both a_2 and a_1 while decreasing a_0. The circuit is then stable until a_0 becomes negative; this occurs when $R_l > R_d - R_{ds} - R_s$; for the devices under consideration, this value is 167 Ω. This condition leads to a growing exponential functions solution for a time-domain device current, which is a kind of instability like the one discussed in [10] and [11]. Fig. 8 shows the transient simulation of the output signal with a series resistance of 180 Ω. The waveform is the periodic repetition of a growing exponential limited by the extent of the NDR region. The fundamental frequency is 133 MHz and its spectrum content is broadly spread over a large frequency range. In conclusion, if the resistive termination is not designed in accordance with the discussed guidelines, the resulting VCO can show this behavior

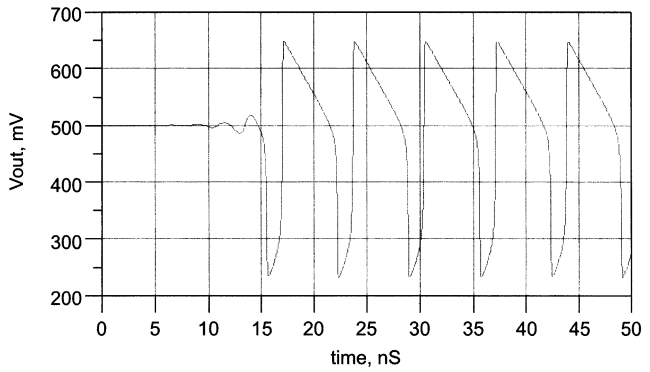


Fig. 8. Simulated output waveform and spectrum with a series resistor of 180 Ω.

superimposed to the sinusoidal oscillation, and the overall effect is a strong degradation of the phase noise performance. In addition, the NDR region is decreased with the insertion of a series resistor R_l; eventually it completely vanishes with an increasing value of R_l. This limits the maximum value of R_l. It can also be demonstrated that, if both a series resistance R_l and series inductor L_c are introduced, the circuit is more stable for higher values of L_c than when only the inductance was present, but when the circuit becomes unstable the oscillation frequency is not affected by the resistance R_l

C. Effect of a Parallel Capacitance With the HITD

This case represents the incorrect evaluation of the diode junction capacitance. Adding a parasitic contribution C_p, we obtain $\hat{C}_d = C_d + C_p$. In this case, the stability is critical only for very low values of $\hat{C}_d$, therefore if the HITFET itself is stable (i.e., the conditions of (5) are verified for $C_p = 0$), it can be demonstrated that stability conditions are not changed by C_p. The most relevant effect associated with this case is a reduction of the diode negative resistance cut-off frequency.

D. Effect of a Parallel Capacitance With the HEMT

As in the previous case, this case considers an incorrect estimation of the drain-source capacitance; moreover, it gives also a guideline for the correct choice of the HEMT size. Introducing $\hat{C}_{ds} = C_{ds} + C_h$ and supposing that the condition $R_d > R_{ds} + R_s$ is always true, it is possible to identify three different situations on the basis of the value of R_d. Defining C_{z1} and C_{z2} as the zeros of $a_1 - (a_0/a_2) = 0$, we obtain the following situations.

1) $R_d < (L_s/C_d\,(R_{ds} + R_s))$: the circuit is stable only if there are real zeros for $a_1 - (a_0/a_2) = 0$ and $C_{z1} < \hat{C}_{ds} < C_{z2}$.
2) $(L_s/C_d\,(R_{ds} + R_s)) < R_d < (L_s/C_d R_s)$: the circuit is stable only if $\hat{C}_{ds} < C_{z2}$, being $C_{z1} < 0$.
3) $(L_s/C_d R_s) < R_d$: the circuit is always stable.

IV. HITFET-Based VCO: Experimental Results

Three prototypes of HITFET-based VCOs have been designed in accordance with the guidelines discussed above. The prototype "A" is implemented in the common-drain configuration and the prototypes "B" and "C" in the common-source configuration. The photo of the prototype "A" fabricated chip is shown in Fig. 9. The overall chip size is around $450 \times 550\ \mu\text{m}^2$.

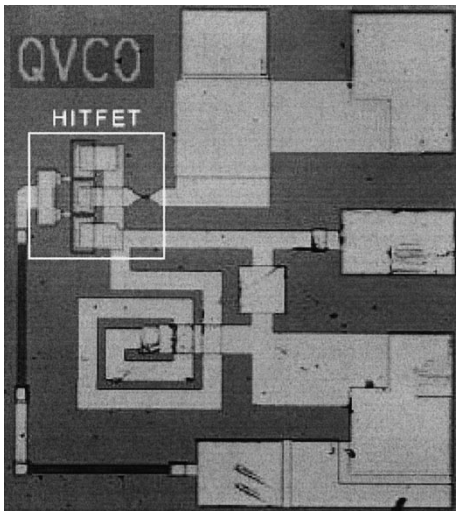


Fig. 9. Chip photograph of the common-source HITFET-based VCO, prototype "A."

The design method adopted is the well-known technique commonly used for reflection oscillators. The HITFET is considered to be the negative resistance element, which must resonate with a proper load to obtain the oscillation. To achieve this, the reflection coefficient (Γ^{LC}) of the *LC* resonator and reflection coefficient (Γ^{HITFET}) of the HITFET must obey the equation

$$\Gamma^{\mathrm{HITFET}} \cdot \Gamma^{\mathrm{LC}} = 1. \tag{7}$$

All the prototypes are biased at 500 mV through the HITD's anode while the tuning potential is applied to the HEMT's gate through a 1-KΩ resistor. The current drawn by the circuit at the drain for a bias voltage of 500 mV and for a control voltage in the range from −0.5 to 0.5 V is in the range of 1.7 to 1.85 mA, with a corresponding dc power consumption of about 850 μW. This value, to the best of our knowledge, is the lowest dc power consumption for a MMIC VCO operating in this frequency range. This feature enables applications in the area of RF-TAG for ID or distributed remote sensor networks where the low power consumption and the low data rate are common required features. Moreover, the extremely low-power supply makes this technology interesting for battery-less solar cell powered equipments. The tuning characteristic of the free-running VCO prototype "A" is shown in Fig. 10 for a wide range of tuning voltage. A frequency swing in the 6.1–6.2-GHz range with a nearly constant power level has been observed. The graph shows a range between −0.4 and −0.1 V in which the frequency changes sharply. This is due to the combined effects of the parabolic shape in the phase of the reflection coefficient and the presence of the lumped *LC* resonator. For a higher level of tuning voltage, the reflection coefficient has a linear behavior in magnitude and phase, and this produces a linear frequency swing, as shown in Fig. 10. The resulting tuning range is 150 MHz. The power output is about −16 dBm, which leads to an efficiency of around 3%. For this calculation, the losses of the measurement test-set

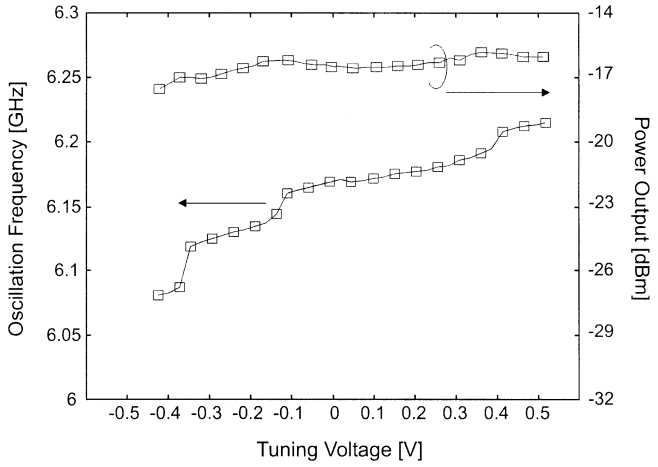


Fig. 10. Common-drain VCO (CD-VCO). Tuning characteristic prototype "A" working at 6.18 GHz.

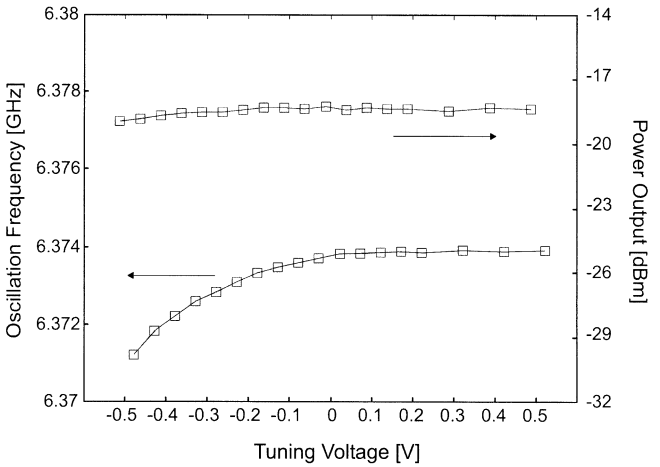


Fig. 12. Common-source VCO (CS-VCO). Tuning characteristic prototype "B" working at 6.37 GHz.

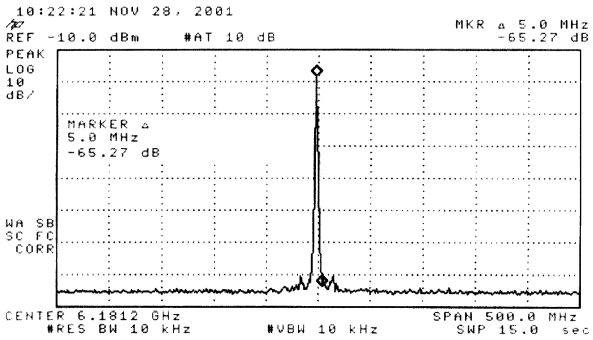


Fig. 11. Output spectrum of the prototype "A": SSCR is -105 dBc/Hz at 5 MHz.

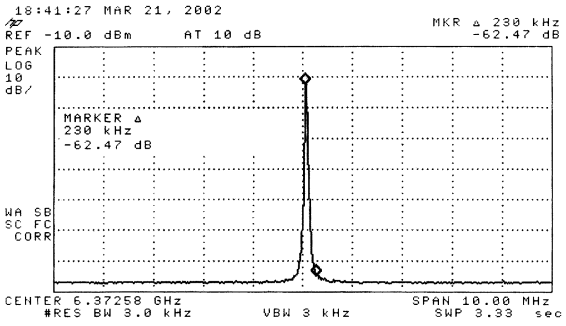


Fig. 13. Output spectrum of the prototype "B": the SSCR is -97 dBc/Hz at 230 kHz.

were deembedded. A relatively constant value of the output power is a direct consequence of the *I–V* characteristic of the HITFET. The effect of the tuning on the bias drain current is small, limited to few tens of microamperes. The power level and consequently the efficiency could be improved by choosing a larger ac-coupling capacitor Ca. This option may make (7) more stringent and could reduce the tuning range. The phase noise performance of the oscillator was estimated from spectrum analyzer measurements (see Fig. 11). At 5-MHz offset from the center frequency, a single-sideband-to-carrier ratio (SSCR) of -105 dBc/Hz was obtained. A study at system level has shown that, for microwave data links which adopt a GFSK modulation with a $BT = 0.5$ and a modulation index of 0.3, the measured phase noise enables a bit error rate (BER) of 10^{-3}, assuming a carrier-to-noise ratio at the receiver input of 24 dB. The phase noise can be improved if the VCO is inserted in a PLL system.

Prototype "B" operates at 6.37 GHz with a much more reduced tuning range, on the order of 2 MHz, and similar output power with respect to prototype "A." The tuning characteristic is shown in Fig. 12. The reduced tuning range may be explained by observing the topology of the two VCOs. The tuning control in the CD- and CS-VCO is obtained mainly by the interaction between the HEMT source-to-gate capacitance and the *LC* resonator. In the CD-VCO, this interaction is much more effective than in the CS-VCO since the *LC* resonator inserted directly in the gate–source network. However, this has an important drawback: the increase of the phase noise. In fact, the output signal modulates the gate–source capacitance and in turn modifies the instantaneous oscillation frequency. The adoption of a CS-VCO allows decoupling the output signal from the control voltage to obtain a better phase noise as experimentally demonstrated by the output spectrum reported in Fig. 13. At 230-kHz offset from the center frequency, an SSCR of -97 dBc/Hz was obtained. Prototype "C: has an *LC* resonator with a higher value of inductance than prototypes "B," making the operative frequency lower, namely, 4.62 GHz.The remaining part of the circuit is the same. The performance in terms of tuning range and output power is similar to that of prototype "B" (see Fig. 14). The main difference consists of higher output power of about -11 dBm, which gives an efficiency of 9.3%. This latter parameter is supposed to be related to the lower operative frequency and to the lack of a design optimization for all the prototypes. Also, in this case, the improved phase noise figure is confirmed by the output spectrum measurement reported in Fig. 15. At a center frequency of 4.6255 GHz, it exhibits an output level of -10.5 dBm and produces an SSCR of -97 dBc/Hz at an offset frequency of 200 kHz. At this point, a comparison with the prior art and different technologies can be conveniently made. Fig. 16 sketches the comparison of the VCO performances presented in this work with the ones reported in literature for both Si and

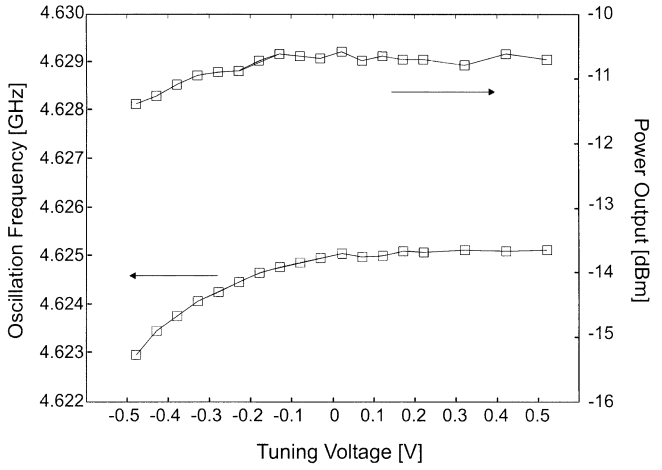


Fig. 14. Common-source VCO. Tuning characteristic prototype "C" working at 4.62 GHz.

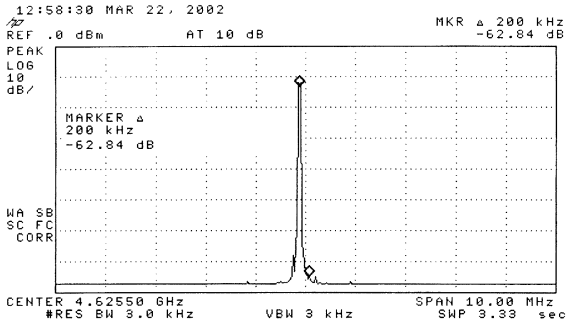


Fig. 15. Output spectrum of the prototype "C": the SSCR is −98 dBc/Hz at 200 kHz.

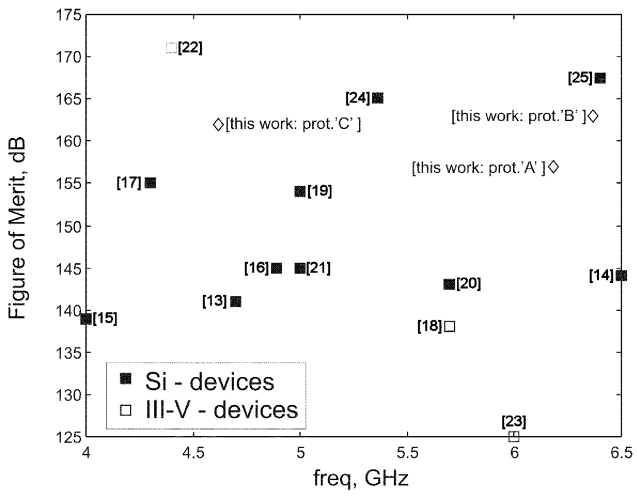


Fig. 16. FOM computed on recently reported VCOs implemented in Si and III-V technologies.

III-V semiconductor technologies. The figure of merit (FOM) adopted for the comparison is the widely used

$$\text{FOM} = \left(\frac{f_0}{f_n}\right)^2 \frac{1}{P \cdot \text{SSCR}(f_n)}. \tag{8}$$

The VCOs presented in this work rank in a very high position although the designs have been optimized neither for phase noise nor for output power. The circuits take advantage of the extremely low power supply and satisfactory phase noise. The circuit in [24] adopted a sophisticated synchronization scheme while the one in [25] employed SiGe BiCMOS technology and a PLL at 6 GHz to obtain an out-band phase noise value of −110 dBm/Hz at 1 MHz. The VCO in [22] used an original configuration derived from the class-E amplifier and was optimized for low-power supply applications. All the VCOs considered for this comparison operated with dc power consumption at least ten times higher than the prototypes presented in this work.

V. Conclusion

A MMIC InP-HEMT\HITD-based VCO circuits operating in the 4–6-GHz bands has been presented. An effective analysis treatment to determine low-frequency stability conditions and range of useful operations of drain-HITFET VCOs are discussed. Three prototypes implemented in common-source and common-drain configurations have been fabricated and tested. The two 6-GHz VCOs demonstrated an output power ranging from −15 to −18 dBm with SSCRs of −105 dBc/Hz at an offset frequency of 5 MHz and −97 dBc/Hz at an offset frequency of 230 kHz for the common–drain and the common-source configurations, respectively. The 4-GHz VCO exhibited an output power of −11 dBm and an SSCR of −98 dBc/Hz at 200 KHz away from the center frequency. The VCOs exhibited very good phase noise characteristics and tuning capability. The unique feature of the circuits is the ability to operate at very low supply voltage. The dc power consumption of the circuits was only about 850 μW. This feature makes the prototypes suitable for RF-TAG as well as for an ID beacon or as a signal source for data links for remote sensor networks where the low-power consumption and extremely low voltages are essential requisites.

Acknowledgment

The authors wish to acknowledge the assistance and support the wafer fabrication team at Motorola Laboratories.

References

[1] Seabaugh and R. Lake, "Tunnel diodes," in *Encyclopedia of Applied Physics*. New York: Wiley, 1997, vol. 22, pp. 335–359.

[2] Cidronali *et al.*, "A proposal of a bi-directional amplifier based on tunneling diodes for RF tagging system," in *Proc. Eur. Gallium Arsenide and Related III-V Compounds Application Symp.–GAAS 2001*, London, U.K., Sept. 24-25, 2001, pp. 89–92.

[3] Cidronali, G. Collodi, M. Deshpande, N. El-Zein, V. Nair, G. Manes, and H. Goronkin, "A highly linear single balanced mixer based on heterojunction interband tunneling diode," *IEEE Trans. Microwave Theory Tech.*, vol. 49, pp. 2437–2445, Dec. 2001.

[4] Y. Liu and P. D. Steenson, "Investigation of subharmonic mixer based on a quantum barrier device," *IEEE Trans. Microwave Theory Tech.*, vol. 48, pp. 787–763, Apr. 2000.

[5] U. Auer, G. Janssen, M. Agethen, R. Reuter, W. Prost, and F. J. Tegude, "A novel 3-D integrated HEMT/RTD frequency multiplier," *IEEE J. Solid-State Circuits*, vol. 32, pp. 650–654, Feb. 1997.

[6] V. Nair, N. El-Zein, J. Lewis, M. Deshpande, G. Kramer, M. Kyler, G. Maracas, and H. Goronkin, "X-band heterostructure interband tunneling FET (HITFET) VCO's," in *IEEE GaAs IC Tech. Dig.*, 1998, pp. 191–194.

[7] N. El-Zein, M. Deshpande, G. Kramer, J. Lewis, V. Nair, M. Kyler, S. Allen, and H. Goronkin, "DC and RF characterization of different heterojunction interband tunneling diodes," in *Proc. Int. Conf. Indium Phosphide and Related Mat.*, May 2000, pp. 146–149.

[8] P. See, D. J. Paul, B. Hollander, S. Mantl, I. V. Zozoulenko, and K. F. Berggren, "High performance $Si/Si_{1-x}/Ge_x$ resonant tunneling diodes," *IEEE Electron Device Lett.*, vol. 22, pp. 182–184, Apr. 2001.

[9] Stock, J. Malindretos, K. M. Indlekofer, M. Pottgens, A. Forster, and H. Luth, "A vertical resonant tunneling transistor for application in digital logic circuits," *IEEE Trans. Electron Devices*, vol. 48, pp. 1028–1032, June 2001.

[10] Kidner, I. Mehdi, J. R. East, and G. I. Hadda, "Power and stability limitations of resonant tunneling diodes," *IEEE Trans. Microwave Theory Tech.*, vol. 38, pp. 864–872, July 1990.

[11] A. Cidronali, "Stability and tradeoffs of tunnel diodes and their microwave applications," in *Proc. IEEE MTT-S Int. Microwave Symp. Dig.*, Phoenix, AZ, May 20–25, 2001.

[12] P. Fay, J. Lu, Y. Xu, G. H. Bernstein, D. H. Chow, and J. N. Schulman, "Microwave performance and modeling of InAs/AlSb/GaSb resonant interband tunneling diodes," *IEEE Trans. Electron Devices*, vol. 49, pp. 19–24, Jan. 2002.

[13] P. Kinget, "A fully integrated 2.7 V 0.35 μm CMOS VCO for 5 GHZ wireless applications," in *Proc. IEEE ISSCC Conf.*, 1998, pp. 226–227.

[14] T. Liu, "A 6.5 GHz monolithic CMOS VCO," in *Proc. IEEE ISSCC Conf.*, 1999, pp. 404–405.

[15] T. Ahrens and T. Lee, "A 3 V 4 GHZ NMOS voltage-controlled oscillator with integrated resonator," in *Proc. ISSCC*, 1996, pp. 393–395.

[16] A. H. Mostafa, M. N. El-Gamal, and R. A. Rafla, "A sub 1 V 4 GHz CMOS VCO and a 12.5 GHz oscillator for low-voltage and high frequency applications," *IEEE Trans. Circuits Syst. II*, vol. 48, pp. 919–926, Oct. 2001.

[17] Väänänen, M. Metsänvirta, and N. T. Tchamov, "A 4.3 GHz VCO with 2 GHz tuning range and low phase noise," *IEEE J. Solid State Circuits*, vol. 36, pp. 142–146, Jan. 2001.

[18] S. A. Yu, C. C. Meng, and S. S. Lu, "A 5.7 GHz interpolative VCO using InGaP/GaAs HBT technology," *IEEE Microwave Wireless Comp. Lett.*, vol. 12, pp. 37–38, Feb. 2002.

[19] P. Van de Ven, J. Van der Tang, D. Kasperkovitz, and A. Van Roermund, "An optimally coupled 5 GHz quadrature *LC* oscillator," in *VLSI Circuits Tech. Symp. Dig*, 2001, pp. 115–188.

[20] Y. Loo, B. G. Colpitts, and D. M. Luke, "Fully integrated bipolar differential VCO's at 2.95 and 5.7 GHZ," in *Proc. Can. Elect. Comput. Eng. Conf.*, vol. 2, 2000, pp. 797–801.

[21] A. H. Mostafa, M. N. El-Gamal, and R. A. Rafla, "CMOS 5–10 GHz oscillators for low voltage RF applications," in *Proc. 43rd IEEE Midwest Circuits Syst. Symp.*, vol. 1, 2000, pp. 478–481.

[22] F. Ellinger, U. Lott, and W. Bächtold, "Design of a low supply voltage high efficiency class E voltage controlled MMIC oscillator at C – band," *IEEE Trans. Microwave Theory Tech.*, vol. 49, pp. 203–206, Jan. 2001.

[23] J. B. Shealy, J. A. Smart, and J. R. Shealy, "Low phase noise AlGaN/GaN FET – Based voltage controlled oscillators (VCO's)," *IEEE Microwave Wireless Components Lett.*, vol. 11, pp. 244–245, June 2001.

[24] Y. Deval, "HiperLAN 5.4 GHZ low power CMOS synchronous oscillator," *IEEE Trans. Microwave Theory Tech.*, vol. 49, pp. 1525–1530, Sept. 2001.

[25] Klepser, M. Scholz, and J. Kucera, "A 5.7 GHz HiperLAN SiGe BiCMOS VCO and PLL frequency synthesizer," in *RFIC Symp. Dig.*, 2001, p. 61, 64.

Alessandro Cidronali (M'89) was born in Florence, Italy, in 1965. He received the Laurea and Ph.D. degrees in electronic engineering from the University of Florence, Florence, Italy, in 1992 and 1998, respectively.

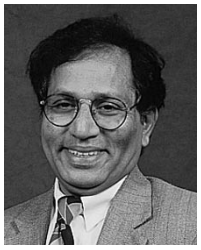
In 1993, he joined the Department of Electronics Engineering, University of Florence, where he became an Assistant Professor in 1999. During his academic career, he has been a lecturer in courses of Applied Electronics and Solid State Electronics and he now teaches Microwave Electronics. His research activities cover the study of active and passive compact structures for monolithic microwave ICs (MMICs), the design of multifunction MMICs for low-power wireless applications, CAD, and numerical modeling of HBTs and HEMTs for microwave and high-speed applications. He is currently working on basic research on quantum functional devices and their applications to microwave circuits.

Giovanni Collodi (M'99) was born in Florence, Italy. He graduated with a degree in electronic engineering in 1996. He received the Ph.D. degree in electronic engineering from the University of Florence, Florence, Italy, in 2000.

After graduation he began working with the Microelectronic Laboratory of the Department of Electronic and Telecommunication of the University of Florence in the field of MMIC and MMMIC application. His main interests concern the characterization and modeling of devices for MMMIC and MMIC application, which include circuit design.

Matteo Camprini was born in Florence, Italy, in 1973. He received the Laurea degree in electronic engineering from the University of Florence, Florence, Italy, in 2000.

After graduation he joined as a Ph.D. student the Microelectronics Laboratory, Department of Electronics and Telecommunications, University of Florence. His research activities concern the study and characterization of tunneling effects in quantum NDR devices and the application of such class of devices to the design of QMMIC circuits.



Vijay Nair (M'01) received the M.S. degree in physics and in electrical engineering from the University of Minnesota, Minneapolis-St. Paul.

His current research responsibilities at Motorola Laboratories, Tempe, AZ, include development of state-of-the art devices and monolithic integrated circuits for wireless communication applications. He holds 10 U.S. patents and has published over 50 papers.

Mr. Nair is a member of The IEEE Electron Device, Vehicular Technology, and Microwave Theory and Techniques Societies. He served as TPC chairman RFIC symposium and VTS conference in 1997. He was the general chairman of the RFIC Symposium 1998. He is the chairman of the Technical Program Committee of the 2001 Microwave Symposium, Phoenix, AZ. He was the receipient of the 1999 Motorola Distinguished Innovator Award. IEEE Phoenix section selected him as "Senior Engineer of the Year-1998."

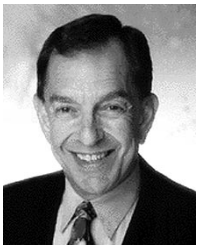
Gianfranco Manes (SM'02) was born in Florence, Italy, on November 16, 1944.

He became Associate Professor in 1980 and Full Professor in 1985 at the University of Florence, Florence, Italy. He has contributed, since the early stages, to the field of surface-acoustic-wave (SAW) technology for radar signal processing and ECM applications. Major contributions were in introducing novel FIR synthesis techniques, fast analog spectrum analysis configurations, and FH waveform synthesis. Since the early 1980s, he has been active in the field of microwave modeling and design. In the early 1990s, he founded and is currently leading the Microelectronics Lab of the University of Florence, committed to research in the field of microwave devices. In 1982, he was committed to starting a facility for the design and production of SAW and MIC/MMIC devices, as a subsidiary of a Florence radar company, SMA Spa. In 1984, the facility became a stand-alone, privately owned, microwave company, Micrel SpA, operating in the field of defence electronics and space communications. During 1996–2000, he was involved in IV FW projects, in the field of information technology applied to the cultural heritage and was invited to orientation meetings and advisory panels for the Commission. His current research interest is in the field of RITD devices for microwave applications in a scientific collaboration with the Group at the Physical Science Research Labs, Motorola Corporation, Tempe, AZ. He was founder and is currently President of MIDRA, a research Consortium between the University of Florence and Motorola. He is Director of the Italian Ph.D. School in Electronics. In November 2000, he was appointed Deputy Rector for the Information System of the University of Florence. He authored more than 100 scientific papers in learned society journals and presentations at International Conferences.

Dr. Manes is member of the Board of Italian Electronics Society.

J. Lewis (M'99) received the B.S. degree in electrical engineering from North Caroline Agricultural and Technical State University, Greensboro, in 1988, and the Ph.D. degree in electrical engineering from Howard University, Washington, DC, in 1991. His doctoral dissertation was related to molecular-beam epitaxy (MBE) growth of strained superlattice and their electrical transport properties.

He is currently with Motorola Laboratories, Tempe, AZ, where he is involved with epitaxial growth of quantum functional device (tunnel diodes) and their applications to RF millimeter-wave circuits. This work focuses on device fabricated in the II–V materials system and specifically InP.



Herb Goronkin (M'75–SM'83–F'89) received the B.A., M.A., and Ph.D. degrees in physics from Temple University, Philadelphia, PA.

He is Vice President and Director of the Physical Research Laboratories within Motorola Laboratories, Tempe, AZ. Following research assignments in the areas of compound semiconductors, silicon ICs, optical sensors, and microwave semiconductor devices, he joined Motorola in 1977 to build their GaAs electronics program. His lab developed Motorola's early versions of heterostructure transistors and circuits for low-power, low-noise wireless applications and high-efficiency power transistors for cellular telephones. More recently, his lab developed DNA biochips for analysis of genetic defects and spun the effort into a newly formed division in 1998. The lab continues development of microfluidic chips for biological sample preparation and analysis. The Physical Research Labs are developing quantum and molecular devices for future logic, wireless, and biosensor applications. The Labs recently transferred its world leadership MRAM technology to the Semiconductor Products Sector who continues its development for product introduction. Motorola's MRAM is based on tunnel junction magnetic devices for universal nonvolatile memory (MRAM) applications. Meanwhile, he and his staff continue the investigation of radical scaling of MRAM memory elements as well as new device applications of spin dependent structures and materials. The labs are rapidly approaching world parity in the area of molecular electronics which will be used in future integrated circuits as well as sensing and analysis of biological molecules. He has served on numerous conference committees and professional organizations. He has over 65 patents and numerous publications.

Dr. Goronkin is a member of the American Physical Society and Sigma Xi. He is a member of Motorola's Science Advisory Board Associates. He is a Motorola Dan Noble Fellow. He was the recipient of the 1992 Motorola Distinguished Innovator Award and the 1995 Master Innovator Award. He was selected as Senior Engineer of the Year in 1993 by the Phoenix Section of the IEEE.