A S-band digital down converter for radar application based on GaAs MMIC fast sample&hold

S-band digital downconverter for radar applications based on a GaAs MMIC fast sample-and-hold

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Abstract: A digital coherent-downconverter configuration is described whose operation principle is based on the theory of subharmonic sampling for narrowband waveforms. This configuration uses a fast sampler, operating at microwave frequencies, for directly demodulating the in-phase and quadrature components of a complex input waveform, yielding a sampled sequence in a suitable format for subsequent analogue-to-digital conversion. Unlike the conventional double-conversion coherent-superheterodine architecture, the proposed configuration offers attractive features in terms of cost and complexity and appears particularly suitable for the implementation of the front-end unit in a coherent receiver. An experimental prototype, based on a very fast GaAs MMIC sample-and-hold (SH) circuit, has been implemented for validating the operation principle. Complex demodulation of a 1 GHz input waveform is demonstrated, with 6-bit equivalent accuracy.

1 Introduction

Radar and communication systems often require complex waveform detection to be implemented for separately processing the in-phase (I) and quadrature (Q) components of the received complex waveform. Subsequent conversion in numeric form, if requested, requires that the sampling and holding operation to be performed after demodulation. The resulting downconverter architecture represents a critical and costly unit of the receiver. This paper describes a new digital downconverter configuration which performs complex detection by means of the sample-and-hold (SH) in a single step by using a single-channel configuration. The key element of the down-converter is a very fast sampling circuit directly operating within the S-band.

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2 Basic operation

Complex signal demodulation is a processing scheme which transforms a one-channel, bandpass formatted RF waveform in a two-channel, lowpass formatted pair of baseband components. The analogue mechanisation of this scheme consists in detecting the in-phase (I) and quadrature (Q) components of the complex waveform by quadrature mixing. Extension to the digital-processing field can be easily achieved, when the lowpass-filtered I and Q components are digitised in two analogue-to-digital (A/D) converters. The analogue configuration has the major drawback of requiring two separate detection channels, whose possible phase and amplitude imbalances must be carefully avoided to ensure successful operation. Coherent demodulation which avoids the need of quadrature mixing can be achieved for a bandpass signal by using a very fast sampling circuit which also performs the holding function requested for subsequent A/D conversion. A digital coherent downconverter architecture is then implemented which offers a number of significant advantages with respect to the analogue mechanisation.

The operation principle of the digital downconverter is based on a particular application of the sampling theorem for bandpass signals, sometimes referred to as subharmonic sampling. The application of the subharmonic sampling to quadrature sampling of bandpass signals has been considered in [1].

Accordingly, let

$$x(t) = p(t)\cos\omega_0 t - q(t)\sin\omega_0 t \tag{1}$$

be the representation of a bandpass signal, where $p(t)$ and $q(t)$ are lowpass bandlimited functions, and B is the RF signal bandwidth. $F_0 = \omega_0/2\pi$ represents the centre frequency. Assume the condition that the upper cutoff frequency of the signal of eqn. 1 is an integer multiple of the bandwidth B,

$$F_0 + \frac{B}{2} = mB \tag{2}$$

According to [1], let the signal described by eqn. 1 be sampled at a uniform rate $T = k/2B$, where k is a positive integer. The resulting sampled sequence $\{x(nT)\}_{-\infty}^{\infty}$, takes the form

$$x(nT) = p(nT)\cos\pi n\frac{2k-1}{2} - q(nT)\sin\pi n\frac{2k-1}{2} \tag{3}$$

It is immediately recognised that the sine/cosine terms at the right-hand side in eqn. 3 can only assume the values +1 or −1. Considering separately the two interleaved sequences obtained for n even, say $n = 2v$

and n odd, say $2v + 1$, in eqn. 3, yields

$$x(vT_1) = (-1)^v p(vT_1)$$
$$x\left(vT_1 - \frac{T_1}{2}\right) = (-1)^{v+k+1} q\left(vT_1 - \frac{T_1}{2}\right) \quad (4)$$

where $T_1 = 2T$.

In [1] it is shown that the two sequences of eqn. 4 express in a sampled form the p and q components of the passband signal eqn. 1. The only additional process required consists in reformatting the sampled sequence in two separate channels, i.e. alternately selecting the odd or even sample, and multiplying the samples by +1 or −1, according to the coefficients appearing in the right-hand side in eqn. 3. As it can be easily met, by properly increasing the bandwidth of the passband signal, the constraint imposed by the condition of eqn. 2 does not represent a limitation.

3 Digital downconverter configuration

The procedure described above is very suitable for quadrature demodulation of complex waveforms, as pointed out in [2]. A relevant limitation could be represented by the inherent sample time misalignment between the p and q components, which are necessarily sampled at different instants. For a general communication application, the time-misalignment problem must necessarily be overcome. In fact, one is interested in reconstructing both the amplitude and the phase of the modulating signal. Several approaches have been proposed for solving the above problem [3, 4]. Nevertheless in those applications, however, where one is basically concerned with a frequency analysis of the I and Q components, the time misalignment problem becomes unessential. It results, in fact, in a different phase term, which does not affect the spectral harmonic content.

This is, in particular, the case of a Doppler radar receiver, where the two I and Q components are postprocessed in a FFT processor after detection. Based on the previously described subharmonic sampling technique, the complex demodulation requested in a Doppler-radar receiver can be easily performed. The digital downconverter can be used directly at the antenna front-end, or at an intermediate frequency sufficiently high for preventing intermodulation interferences. For that reason, operation around 1GHz or more is particularly well suited.

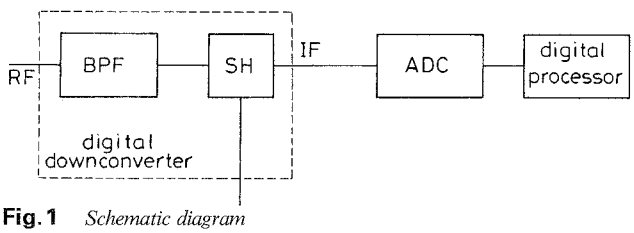

Fig. 1 *Schematic diagram*

The schematic diagram of the digital-downconverter configuration is represented in Fig. 1 [5]. The incoming RF waveform, after bandpass filtering and low-noise amplification, is fed to the RF port. A second bandpass filter is requested, after amplification, for outband thermal-noise filtering. Complex sampling takes place at this stage, according to the procedure discussed above. The input waveform is fed, after sampling, to an A/D converter for digital conversion and subsequent processing. As the digital conversion requires each sample to be held to a fixed value during the conversion interval, it is convenient to perform both sampling and holding operations in one step at this point. Both operations can be performed by using an SH circuit. A clock waveform is fed to the LO port, determining the sampling interval T.

According to the condition described by eqn. 2, T is related to the RF input-waveform bandwidth B through a positive integer k. Obviously, minimum sampling rate is achieved when $k = 1$. In the present implementation this condition is chosen to minimise the A/D conversion-speed requirement. After A/D conversion, as stated above, the data are postprocessed in a digital form. The reformatting and weighting operations, previously discussed, can then easily be performed at the post-processing stage, thus avoiding the need for any additional hardware.

4 System performance

In a practical realisation of the digital downconverter, the most critical element is represented by the SH circuit, which is operated at microwave frequencies. An open-loop SH structure was chosen for its ability to provide shorter acquisition times than the closed-loop configuration. The circuit could be operated in a SH or in the track-and-hold (TH) mode, for the downconverter application. A brief discussion of the main errors affecting the circuit performances is now presented.

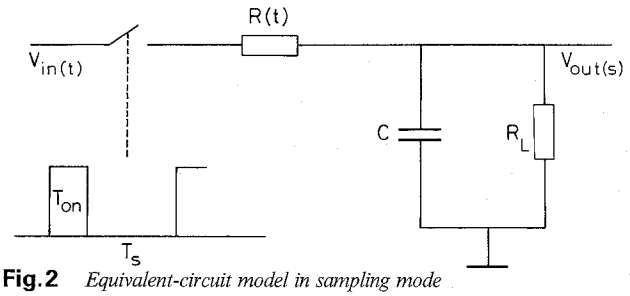

Fig. 2 *Equivalent-circuit model in sampling mode*

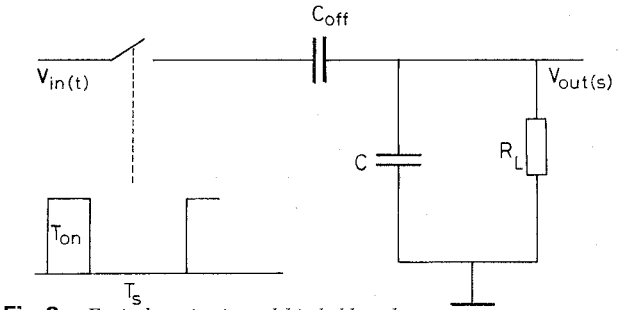

Fig. 3 *Equivalent-circuit model in hold mode*

4.1 Sample interval

The models represented in Figs. 2 and 3 are used for error analysis. In the circuit of Fig. 2, C and R_L represent, respectively, the hold capacitor and the load of the buffer stage following the SH circuit. The sampler is modelled as an ideal switch with a time-variable resistor in series, which represents the switch internal resistance. Consider first the SH-operation mode. The switch is turned on for a very short time interval t_{on} whose duration is inversely proportional to the RF bandwidth. According to [6], only a fraction ε_A of the

input signal is stored in the hold capacitor, resulting in a sampler efficiency which can be of the order of 10%, at microwave frequencies. The effect of the finite turn-on time results in a lowpass behaviour.

In the TH mode the input RF signal is sampled after a convenient acquisition time t_{ac} defined as the time to settling within 1/2 LSB of steady-state at full-speed input signal. Thus, at the time the switch is turned off, nominally the whole of the input waveform drops across the hold capacitor. As a consequence the TH mode exhibits a better signal-to-noise (S/N) ratio than the SH mode. In the analysis carried out in [6], the switch operation has been described under the assumption of a perfectly rectangular switch on-resistance as a function of time. When a very high-speed signal is sampled, the switch turn-off time cannot be neglected with respect to the variation of the input waveform. To evaluate the effect of the turn-off time, a linear variation of the time-variable resistor $R(t)$ is considered between the values r_{on} and r_{off} during a time interval t_a corresponding to the switch aperture time:

$$R(t) = r_{on} + \left(\frac{r_{off} - r_{on}}{t_a}\right) t \tag{5}$$

During t_a, the maximum variation of the input voltage, a sine wave of amplitude A and period T, is

$$V_{in}(t) = V_{in}(t_0) + 2\pi\frac{A}{T}t \tag{6}$$

where t_0 is the nominal sampling instant. The voltage-equilibrium equation of the circuit in Fig. 2 is

$$V_{in}(t_0) + 2\pi\frac{A}{T}t = i(t)\left(r_{on} + \frac{\Delta r}{t_a}t\right) + V_H(t) \tag{7}$$

As a first order of approximation let us assume that $V_H(t) \simeq V_{in}(t_0)$. The current flowing in the circuit of Fig. 2 can easily be determined by using eqn. 7. Integrating between t_0 and t_a, yields the additional charge due to the finite aperture time. Dividing by C results in the hold-voltage variation, i.e. the maximum voltage error, which is expressed by

$$\delta V_H = 2\pi A\frac{t_a}{T}\frac{1}{r_{off}C}\left\{t_a - \frac{1}{k}t_a\log(1+k)\right\} \tag{8}$$

where $k = r_{off}/r_{on}$. Letting $k >> 1$, the associated relative error is

$$\varepsilon_S \cong \frac{2\pi}{k}\frac{t_a^2}{T}\frac{1}{r_{on}C} \tag{9}$$

Eqn. 9 defines the value of the maximum aperture time as a function of the desired system accuracy, technological process, switch resistance and sampling rate.

As stated above, the other sources of error do not depend on the particular operating mode. They are considered individually below.

4.2 Hold interval

The equivalent circuit of Fig. 2 is representative of the switch dynamic operation. While in the hold mode $R(t)$ should be replaced by a C_{off} capacitor, in the switch equivalent circuit, according to the diagram in Fig. 3. The relative-output-voltage errors introduced by feedthrough ε_F and drop rate ε_D are then

$$\varepsilon_F = \frac{C_{off}}{C} = \frac{\tau_p}{r_{on}C} \tag{10}$$

$$\varepsilon_D = \frac{T_{conv}}{R_L C} \tag{11}$$

where T_{conv} is the conversion time of the A/D converter.

4.3 Clock-waveform jitter

A last source of error, which should be considered when defining the performance of a SH circuit, is the effect of clock-waveform jitter. When a high-speed signal is sampled, any deviation of the sampling time from a precise interval T will appear as an error of the reordered voltage. The clock-jitter error, evaluated at the maximum slew rate of a sine-wave input signal, can be shown to be

$$\varepsilon_J = 2\pi\frac{\delta t}{T} \tag{12}$$

where δt is the clock jitter

The SH design basically involves defining the values of r_{on} and C, with R_L, T and τ_p as system parameters. The desired value of C is stated by eqn. 11 as a function the maximum allowable drop, during the A/D-conversion interval, for a given bit number N:

$$C = 2^{N-1}\frac{T_{conv}}{R_L} \tag{13}$$

On the other hand, r_{on} is obtained according to eqns. 10 and 11:

$$r_{on} = R_L\frac{\varepsilon_D}{\varepsilon_F}\frac{\tau_p}{T_{conv}} \tag{14}$$

where $\tau_p = r_{on}C_{off}$ is a figure of merit of the process.

5 Sample-and-hold circuit implementation

A number of different high-speed SH configurations have been proposed in the literature for the application to A/D converters and digitising oscilloscopes. A diode-bridge sampling gate has been chosen in the present implementation, as it offers a greater dynamic range and a better RF-to-LO-port isolation. This results, however, in increased complexity as the bridge necessarily requires two complementary driving pulses for its operation. If a single-phase clock pulse is available, a microwave balun [6, 7], or differential amplifier [8, 9] is required to generate the complementary pulses needed for the diode-bridge operation.

For the implementation of the digital downconverter discussed in this paper, two different prototypes of the SH circuit have been designed and tested, referred to as SH1 and SH2, respectively. The prototype SH1 uses a single MESFET as switching element, thus avoiding the need of two complementary pulses for switching the bridge. The prototype SH2 uses an original active-pulse-transformer configuration, implemented by the F20 GEC–Marconi process which is a 0.5μm gate length with a 20GHz unit gain frequency f_T. The operation of the digital downconverter will be demonstrated for input waveforms up to the S-band with a signal bandwidth up to 50MHz. According to the previous discussion, the main requirements of the SH circuit for fulfilling the above specifications are:

Switching time < 100ps

Holding time ≃ 4ns

Bandwidth < 62.5MHz

RF-to-IF port isolation > 30dB @ 1GHz

5.1 SH1 prototype

A very simple SH configuration, particularly suitable for a hybrid prototype, has been designed and

implemented. The circuit diagram is shown in Fig. 3. The sampling gate is a diode bridge connecting the RF input to the hold capacitor and the switching element is represented by the MESFET, whose drain and source are connected to the two other bridge nodes. The sampling-pulse amplitude varies between 300mV (hold interval), and –900mV (sample interval) and is fed to the MESFET gate. The operation is very easily illustrated with reference to Fig. 4. In the sample mode, the switching MESFET is turned off and the diodes of the bridge are directly biased, letting the input waveform drop across C_H. In the hold mode, the MESFET is turned on. The voltage difference between drain and source drops to about 0.5V. Consequently the two series-connected diodes in the two arms of the bridge become inversely biased and the hold capacitor is disconnected by the RF source. The circuit was fabricated on a soft substrate in two versions. The former is based on four beam-lead Schottky diodes and the latter on a surface-mount bridge quad in a SOT-143 plastics case. Owing to the relatively low frequency of operation, similar performances were reported in both cases. A plastics-case MESFET with f_T = 16GHz was used. The sampling pulses were generated starting from a 175 PS-snap-time RF, and obtaining a 400ps aperture time. A –10dBm 1030MHz tone was used as RF input, simulating an SSB-SC AM signal with F_c = 1GHz and B = 30MHz. Fig. 5 shows the control currents measured in the bridge and in the MESFET, as depicted in Fig. 3. The sampled waveform is shown in Fig. 6. A 20dB-gain IF buffer was inserted to prevent loading effects from the oscilloscope. The estimated conversion loss of the SH circuit is 26dB, being the peak-to-peak amplitude of the sampled signal equal to 91mV. Fig. 7 illustrates an expansion of the sampled signal. The 1.6ns hold time measured is consistent with the acquisition time of several commercially available A/D converters.

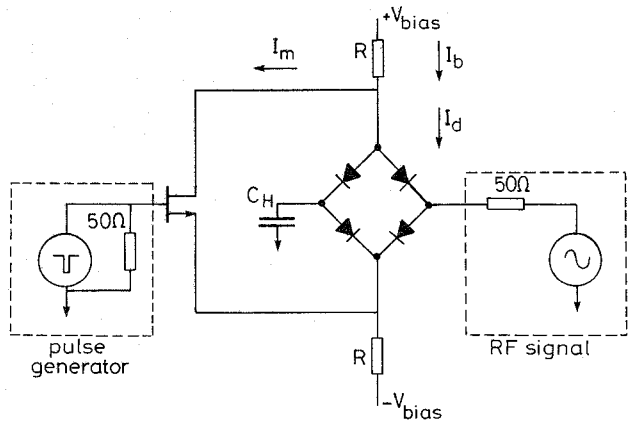

Fig. 4 *Schematic diagram of SH1 sample-and-hold circuit*

5.2 SH2 prototype

A second version of the SH circuit has been designed and implemented in a monolithic form. The schematic diagram is represented in Fig. 8. The sampling gate is arranged in a balanced configuration to reduce feedthrough, jitter aperture, commutation pedestal and settling time. The generation of the balanced pulse is a critical factor in the implementation of the sampling circuit. In the previously illustrated configuration this problem was circumvented by using a floating MESFET to switch the bridge. As a result, a very simple implementation has been obtained, at the expense of a limited efficiency of the configuration.

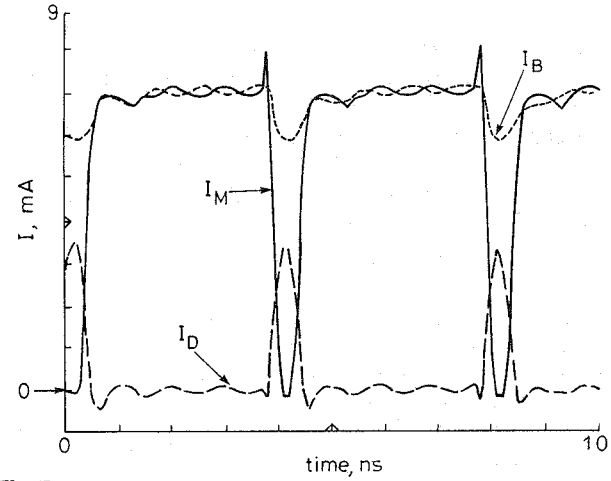

Fig. 5 *Measured currents in the bridge (I_D), in the MESFET (I_M) and in the power supply (I_P)*

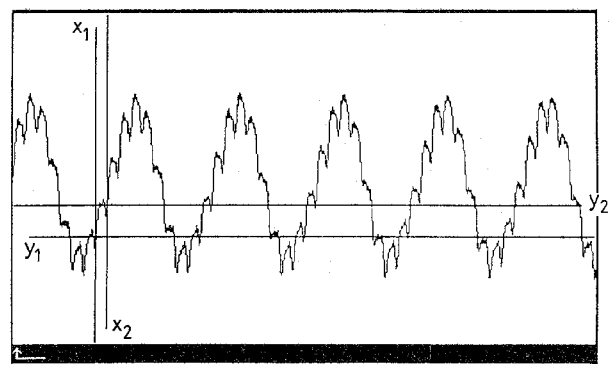

Fig. 6 *Sampled signal obtained by SH1*
x_1 = 28ns; y_1 = –23mV; x_2 = 32ns; y_2 = –7.4mV
Horizontal scale: 20ns/div.

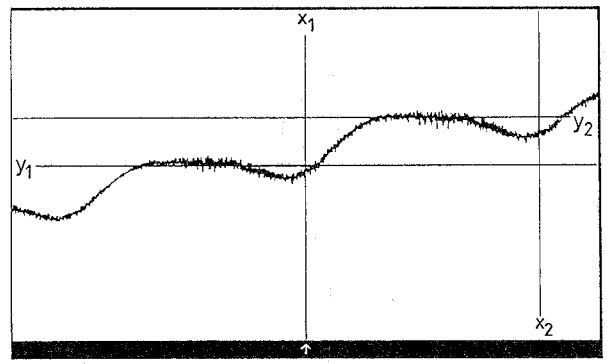

Fig. 7 *Hold time and 'droop off' of the sampled signal*
x_1 = 0; y_1 = 11 mV; x_2 = 4ns; y_2 = 33.4mV
Horizontal scale: 1ns/div.

In the present case a pulse transformer is needed. A MESFET differential pair can be proposed for this purpose [9, 10], assuming that two complementary logic waveforms are available. The function of the amplifier is simply to buffer the sampling gate with respect to the logic waveforms.

In our case, the driving generator is implemented by a step-recovery diode (SRD) for achieving very fast switching times. As the SRD produces an unbalanced pulse, a wideband transformer is necessarily requested. A classical hybrid implementation of a wideband transformer is based on a passive balun using various microstrip/slotline transitions, basically originated by the Marchand balun [7, 8]. Passive baluns are very

suitable in applications requiring very fast switching times (< 100ps) and very fast sampling rates (> 1GHz). On the other hand, they exhibit an intrinsic bandpass behaviour, while in our case a lowpass transfer function is needed. The problem can be approached by using an original active-pulse-transformer configuration represented by the broken-line block in Fig. 8. The four MESFETs are arranged in a classical Wien-bridge configuration. The down-converter operation can be understood making reference to Fig. 9. The bridge is antisymmetrical with respect to the vertical diagonal; the two elements, driven by the RF pulse, unbalance the bridge and generate a differential voltage appearing across the opposite diagonal of the bridge. The SH2 prototype has been tested using an SSB-SC AM test signal with a 1GHz centre frequency, and a 44.92MHz bandwidth was used. The downconverter accuracy was evaluated by using two different methods: the fast Fourier transform and the sinewave-curve-fitting (SCF) test [11]. For that purpose the sampled data were converted by a commercial 8-bit A/D with a maximum 300Msa/s capability.

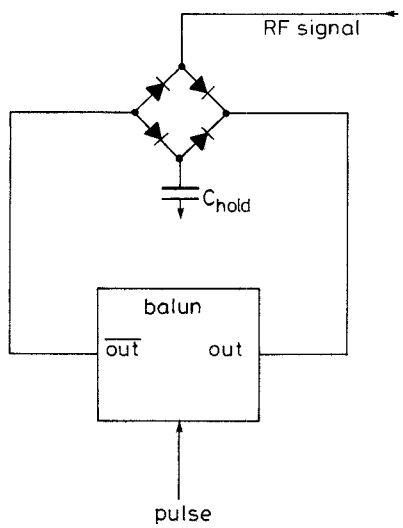

Fig. 8 *Downconverter schematic diagram*

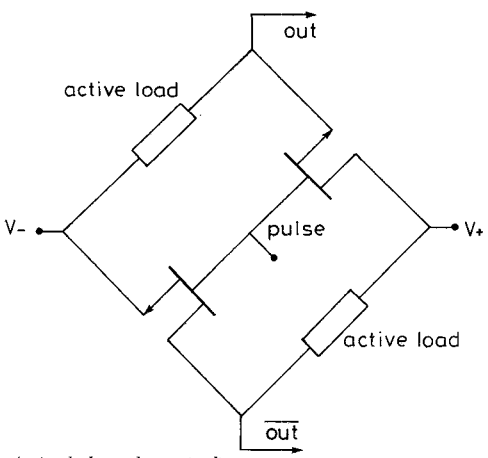

Fig. 9 *Active-balun schematic diagram*

Fig. 10 reports the FFT of the converted signal: the intrinsic low harmonic content is observed, demonstrating the low distortion introduced by the undersampling operation. As previously discussed, the downconverter accuracy is determined by sampling time, drop rate, feedthrough and clock jitter and depends on design/foundry process parameters. In the present case, the design parameters are load resistor R_L = 100kΩ, hold capacitor C_H = 5pF, A/D-conversion time T_{CONV} = 1.6ns, aperture time T_a = 100 ps and an aperture jitter δt = 2ps. The F20 GEC–Marconi foundry-process parameters are: $K = r_{off}/r_{on} = 3 \times 10^3$, $\tau_p = r_{on}\, C_{off} = 0.25$ps.

The worst case relative error is given by

$$E_r = \sum_{i=1}^{4} |\varepsilon_i| \qquad (15)$$

where ε_i represent the relative errors, as defined in eqns. 9–12. The calculation predicts an accuracy which is good agreement with the 5.8-bit accuracy experimentally evaluated by the SCF test. The same evaluation shows a value of 4.5 bit at 3GHz.

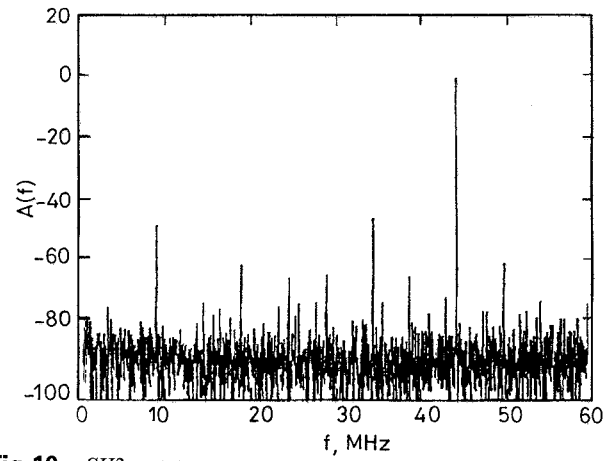

Fig. 10 *SH2 prototype*
FFT response to a 1GHz centre frequency and a 44.92MHz bandwidth SSB-SC AM input test signal sampled by 4ns and 7% duty-cycle waveform
B_W = 44.92MHz
$F_{sampling}$ = 249.85MHz
4096 FFT samples

6 Conclusions

A new digital coherent downconverter has been discussed. The architecture proposed avoids the inherent problems related to the use of quadrature mixing, by replacing the coherent detection architecture, needed in the conventional superetherodyne configuration, with a single, fast SH circuit.

Two SH prototypes were designed and tested. The former was a very simple and effective configuration implemented in hybrid topology, and the latter was based on an original GaAs MMIC. The MMIC was designed using the F20 GEC–Marconi process.

An extensive time-domain and frequency characterisation of each component of the system has been carried out. The experimental results on an SSB-SC AM test signal show a digital intermediate-frequency signal format with 5.8-bit equivalent accuracy at a frequency of 1GHz. Downconverter operation up to 3GHz is feasible using the proposed SH configuration with 4.5 bit accuracy.

7 Acknowledgment

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