Small-Signal Modeling of PWM Dual-SEPIC DC-DC Converter by Circuit Averaging Technique

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***Abstract*—This paper presents the small-signal modeling of a dual-SEPIC dc-dc converter power stage operating in continuous-conduction mode using the circuit averaging technique. The converter component parasitic resistances are taken into account. From the small-signal model, the following expressions of the converter required to design the outer voltage loop are derived: duty cycle-to-output voltage and input-to-output voltage transfer functions, input impedance, and output impedance. A design example is given and the characteristics of these transfer functions are analyzed. Simulations are performed to verify the correctness of the theoretically obtained transfer functions. The dual-SEPIC converter has four reactive components and yields transfer functions of order two. A brief discussion on this aspect is also provided.**

I. Introduction

A dual-SEPIC (zeta) converter is the dual to the SEPIC (single ended primary inductance converter) converter [1]. These topologies have found its application in various areas such as electronic ballasts, power factor correctors, battery chargers, etc. [1] - [5]. Designing control circuits for SEPIC converters is a challenge since their transfer functions are of fourth order [3] - [5]. However, by inspecting the operation of the dual-SEPIC converter, state equations of order two were obtained, forming a motive to develop its small-signal model and hence derive the network functions.

The dual-SEPIC dc-dc converter shown in Fig. 1 is considered in this paper. The main objectives of this paper are: (a) to develop the dc model using circuit averaging technique by averaging the steady-state switch current and diode voltage waveforms [6] - [8], (b) to develop a small-signal linear model, (c) to derive the expressions for the open-loop small-signal power stage transfer functions, input and output impedances, (d) to validate the theoretical predictions through simulations, and (e) to justify how a circuit with four reactive components is described by second-order transfer functions.

This paper is organized as follows. In Section II, the fundamental steady-state equations required for circuit averaging is presented. The dc, averaged model, the large-signal model, and the low-frequency small-signal linear equivalent model are developed in this Section. Using the small-signal model, the relevant transfer functions are derived in Section III. Section IV presents a design example of the dual-SEPIC dc-dc converter and the theoretical results are validated using simulations. Finally, a few concluding remarks are presented in Section V.

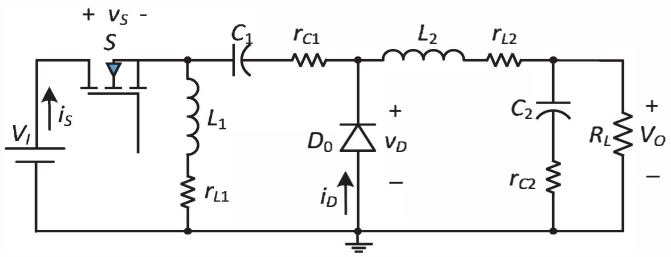

Fig. 1. Circuit of the dual-SEPIC dc-dc converter including inductor and capacitor parasitic resistances.

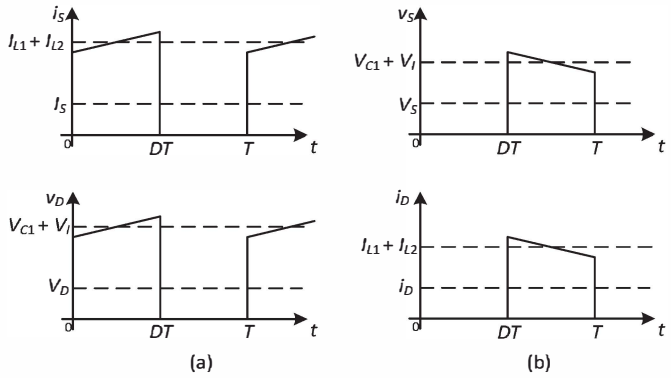

Fig. 2. Key waveforms of the switching network. (a) Switch current and diode voltage during $0 < t \leq DT$. (b) Switch voltage and diode current waveforms during $DT < t \leq T$.

II. Model Development

A. Averaged Circuit Model

Fig. 2 shows the waveforms of the MOSFET current i_S, diode current i_D, MOSFET voltage v_S, and diode voltage v_D. The waveforms comprise of both dc or averaged and a switching frequency components. Using the circuit averaging technique, the dc or low-frequency equivalent of the dual-SEPIC converter shown in Fig. 1 is obtained. The circuit averaging technique involves averaging the switch currents and

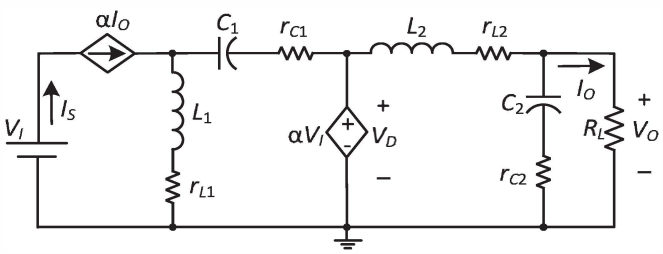

Fig. 3. Averaged, dc equivalent model of the dual-SEPIC converter in CCM, where $\alpha = \frac{D}{D'}$.

voltages over a single switching time period. The expression for average current through the MOSFET S is

$$I_S = \frac{1}{T}\int_0^T i_S dt = \frac{1}{T}\int_0^{DT} (I_{L1} + I_{L2})dt = D(I_{L1} + I_{L2}), \tag{1}$$

where D is the duty cycle of the MOSFET. The expression for average current through the diode D_0 is

$$I_D = \frac{1}{T}\int_0^T i_D dt = \frac{1}{T}\int_{DT}^T (I_{L1} + I_{L2})dt = D'(I_{L1} + I_{L2}), \tag{2}$$

where $D' = 1 - D$. Therefore, from (1) and (2), the average MOSFET current is

$$I_S = \frac{D}{D'} I_D = \frac{D}{D'} I_{L2}. \tag{3}$$

During the diode conduction interval, the average diode current I_D is equal to the average current through the inductor L_2 is I_{L2} equal to the dc load current I_O [1], i.e.,

$$I_D = I_{L2} = I_O = \frac{V_O}{R_L}. \tag{4}$$

Similarly, the expression for average voltage across the diode D_0 is

$$V_D = \frac{1}{T}\int_0^T v_D dt = \frac{1}{T}\int_{DT}^T (V_{C1} + V_I)dt = D'(V_{C1} + V_I) \tag{5}$$

and the average voltage across the MOSFET is

$$V_S = \frac{1}{T}\int_0^T v_S dt = \frac{1}{T}\int_0^{DT} (V_{C1} + V_I)dt = D(V_{C1} + V_I). \tag{6}$$

Thus, from (5) and (6), we have

$$V_D = \frac{D}{D'} V_S = \frac{D}{D'} V_I. \tag{7}$$

Equations (3) and (7) are the expressions for the averaged MOSFET current and diode voltage. The switching network can be replaced by controlled current and voltage sources [6], [7]. Fig. 3 shows the averaged, dc equivalent model of the dual-SEPIC converter with its MOSFET replaced by a current-controlled current source and the diode by a voltage-controlled current source. The load resistance can be represented as a constant current sink with an average value I_O.

B. Small-Signal Equivalent Model

The averaged current and voltage in (3) and (7) can be expressed as slowly varying and time-dependent large-signal quantities. The large-signal quantities relevant to the averaged switching network are d_T, i_D, i_S, v_D, v_S and represented as

$$\begin{aligned} d_T &= D + d, \\ i_{L2} &= I_{L2} + i_{l2}, \\ i_S &= I_S + i_s, \\ v_D &= V_D + v_d, \\ v_I &= V_I + v_i, \end{aligned} \tag{8}$$

where D, I_D, I_S, V_D, and V_I are the dc components, while d, i_d, i_s, v_d, and v_i are the small-signal ac components. Thus, the expressions for the large-signal MOSFET current and the large-signal diode voltage are

$$\begin{aligned} i_S &= \frac{d_T}{d'_T} i_{L2}, \\ v_D &= \frac{d_T}{d'_T} v_I, \end{aligned} \tag{9}$$

where $d'_T = 1 - d_T = D' - d$. Substituting (8) into (9), we get

$$D'I_S + D'i_s - I_S d - di_s = DI_{L2} + Di_{l2} + I_D d + di_{l2} \tag{10}$$

and

$$D'V_D + D'v_d - V_D d - dv_d = DV_S + Dv_i + V_I d + dv_i. \tag{11}$$

Using (3) and (7) in (10) and (11) yields

$$D'i_s = I_S d + di_s + Di_{l2} + I_D d + di_{l2} \tag{12}$$

and

$$D'v_d = V_D d + dv_d + Dv_i + V_I d + dv_i. \tag{13}$$

The principle of *linearization* can be applied to the expressions in (12) and (13), if and only if the following small-signality conditions are satisfied:

$$\begin{aligned} d &<< D, \\ v_s &<< V_S, \\ i_s &<< I_S, \\ v_d &<< V_D, \\ v_i &<< V_I. \end{aligned} \tag{14}$$

Thus, (12) and (13) can be approximated to obtain the linear small-signal MOSFET current i_s and small-signal diode voltage v_d as

$$i_s = \frac{I_S}{D'} d + \frac{D}{D'} i_{l2} + \frac{I_{L2}}{D'} d = \frac{I_{L2}}{D'^2} d + \frac{D}{D'} i_{l2} \tag{15}$$

and

$$v_d = \frac{V_D}{D'} d + \frac{D}{D'} v_i + \frac{V_I}{D'} d = \frac{V_I}{D'^2} d + \frac{D}{D'} v_i. \tag{16}$$

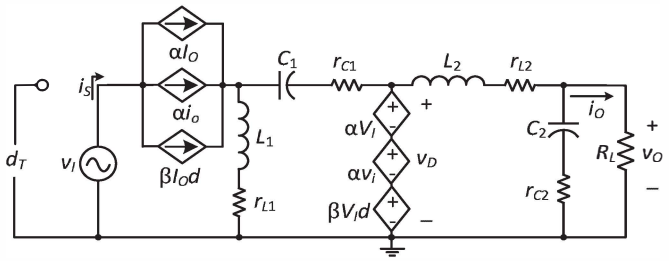

Fig. 4. Large-signal linear model of the dual-SEPIC converter in CCM, where $\alpha = \frac{D}{D'}$ and $\beta = \frac{1}{D'^2}$.

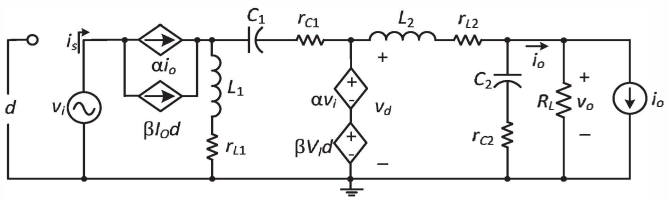

Fig. 5. Small-signal linear model of the dual-SEPIC converter in CCM, where $\alpha = \frac{D}{D'}$ and $\beta = \frac{1}{D'^2}$.

A complete large-signal linearized model is shown in Fig. 4, where the MOSFET is replaced by both dc and ac current sources, while the diode is replaced by the dc and ac voltage sources. The dc model can be obtained by removing all the ac components in Fig. 4 and was shown in Fig. 3. Fig. 5 shows the small-signal linear model and is used to derive the expressions for the various power stage transfer functions of the dual-SEPIC converter in CCM.

III. Small-Signal Transfer Functions

The power stage transfer functions can be derived using the small-signal model shown in Fig. 5. The main transfer functions required for the outer loop design are: (a) duty cycle-to-output T_p, (b) input-to-output M_v, (c) input impedance Z_i, and output impedance Z_o. The impedances in the model can be lumped and expressed as follows:

$$Z_{L1} = r_{L1} + sL_1,$$
$$Z_{C1} = r_{C1} + \frac{1}{sC_1},$$
$$Z_{L2} = r_{L2} + sL_2,$$
$$Z_L = R_L || \left(r_{C2} + \frac{1}{sC_2} \right) = \frac{R_L(sr_{C2}C_2 + 1)}{(R_L + r_{C2})C_2 s + 1}. \quad (17)$$

A. Duty Cycle-to-Output Voltage Transfer Function

The control transfer function can be determined by letting v_i and i_o to zero in the small-signal model shown in Fig. 5. Using the voltage divider principle, we get

$$v_o = \frac{V_I}{D'^2} \frac{Z_L}{Z_L + Z_{L2}} d \quad (18)$$

to yield the duty cycle-to-output voltage transfer function as

$$T_p = \frac{v_o}{d} = \frac{V_I}{D'^2} \frac{Z_L}{Z_L + Z_{L2}}. \quad (19)$$

Substituting (17) into (19), the expression for T_p in the standard second-order form is

$$T_p = T_{px} \frac{s + \omega_{zn}}{s^2 + 2\xi\omega_o s + \omega_o^2} = T_{p0} \frac{1 + \frac{s}{\omega_{zn}}}{1 + \frac{2\xi s}{\omega_\bullet} + \frac{s^2}{\omega_\bullet^2}}, \quad (20)$$

where

$$T_{px} = \frac{V_I R_L r_{C2}}{D'^2 L_2 (R_L + r_{C2})}, \quad (21)$$

the gain at dc is

$$T_{p0} = \frac{V_I}{D'^2} \frac{R_L}{r_{L2} + R_L}, \quad (22)$$

the natural undamped corner frequency is

$$\omega_o = \sqrt{\frac{r_{L2} + R_L}{L_2 C_2 (r_{C2} + R_L)}}, \quad (23)$$

the frequency of the zero due to the filter capacitor branch is

$$\omega_z = \frac{1}{r_{C2} C_2}, \quad (24)$$

and the damping coefficient is

$$\xi = \frac{L_2 + C_2[R_L(r_{C2} + r_{L2}) + r_{C2} r_{L2}]}{2\sqrt{(R_L + r_{C2}) L_2 C_2}}. \quad (25)$$

B. Input-to-Output Voltage Transfer Function

The equivalent model shown in Fig. 5 can be used to evaluate the input-to-output voltage transfer function of the dual-SEPIC dc-dc converter. We arrive at the required model by setting the small-signal sources d and i_o to zero. Applying the voltage divider principle at the output stage, we get

$$v_o = \frac{D v_i}{D'} \frac{Z_L}{Z_L + Z_{L2}} \quad (26)$$

to yield the input-to-output voltage transfer function as

$$M_v = \frac{v_o}{v_i} = \frac{D}{D'} \frac{Z_L}{Z_L + Z_{L2}}. \quad (27)$$

Substituting for the impedances given in (17) into (27) results in the audio susceptibility as

$$M_v = M_{vx} \frac{s + \omega_z}{s^2 + 2\xi\omega_o s + \omega_o^2} = M_{v0} \frac{1 + \frac{s}{\omega_z}}{1 + \frac{2\xi s}{\omega_\bullet} + \frac{s^2}{\omega_\bullet^2}}, \quad (28)$$

where

$$M_{vx} = \frac{D R_L r_{C2}}{D' L_2 (R_L + r_{C2})}, \quad (29)$$

the gain at dc is

$$M_{v0} = \frac{D}{D'} \frac{R_L}{r_{L2} + R_L}. \quad (30)$$

The remainder of the parameters in (28) have been determined in (23), (24), and (25).

C. Input Impedance

The equivalent model shown in Fig. 5 can be used to determine the expression for the input impedance of the dual-SEPIC dc-dc converter. The small-signal perturbations d and i_o are reduced to zero. The current through the inductor L_2 is

$$i_{l2} = \frac{D}{D'(Z_{L2} + Z_L)} v_i. \tag{31}$$

The input current i_i is

$$i_i = \frac{D}{D'} i_{l2} = \left(\frac{D}{D'}\right)^2 \frac{v_i}{Z_L + Z_{L2}} \tag{32}$$

to yield the expression for the input impedance as

$$Z_i = \frac{v_i}{i_i} = \left(\frac{D'}{D}\right)^2 (Z_L + Z_{L2}) \tag{33}$$

$$= Z_{ix} \frac{s^2 + 2\xi\omega_o s + \omega_o^2}{s + \omega_{pz}} = Z_{i0} \frac{1 + \frac{2\xi s}{\omega_o} + \frac{s^2}{\omega_o^2}}{1 + \frac{s}{\omega_{zz}}}, \tag{34}$$

where

$$Z_{ix} = \left(\frac{D'}{D}\right)^2 L_2. \tag{35}$$

The input resistance at dc is

$$Z_{i0} = Z_i(0) = R_{i0} \approx \left(\frac{D'}{D}\right)^2 R_L \tag{36}$$

and the left-half plane pole is

$$\omega_{zz} = \frac{R_L}{(R_L + r_{C2})C_2}. \tag{37}$$

D. Output Impedance

A test voltage signal v_t is applied across the load resistance, which yields a small-signal current i_t. By setting the perturbations d and v_i to zero, we obtain the output impedance as

$$Z_o = \frac{v_t}{i_t} = \frac{Z_{L2} Z_L}{Z_{L2} + Z_L}. \tag{38}$$

Manipulating (38), one obtains a second-order transfer function for the output impedance, whose expression resembles that of a parallel resonant circuit. The dc gain is

$$Z_o(0) = R_{o0} = \frac{R_L r_{L2}}{R_L + r_{L2}}. \tag{39}$$

IV. Results

A. Theoretical Prediction

A dual-SEPIC converter with the following specifications was considered [1]: $V_I = 28$ V, $f_s = 100$ kHz, $P_O = 60$ W, and $V_O = 12$ V. Using the design equations presented in [1], the values of inductors and capacitors for a nominal duty ratio of $D = 0.3$ were: $L_1 = L_2 = 120$ μH to ensure continuous-conduction mode, $C_1 = 16$ μF, and $C_2 = 10$ μF. The dc and low-frequency winding resistances of the inductors L_1 and L_2 are respectively, $r_{L1} = r_{L2} = 10$ mΩ. The parasitic resistances of the filter capacitors C_1 and C_2, respectively, are $r_{C1} = r_{C2} = 30$ mΩ.

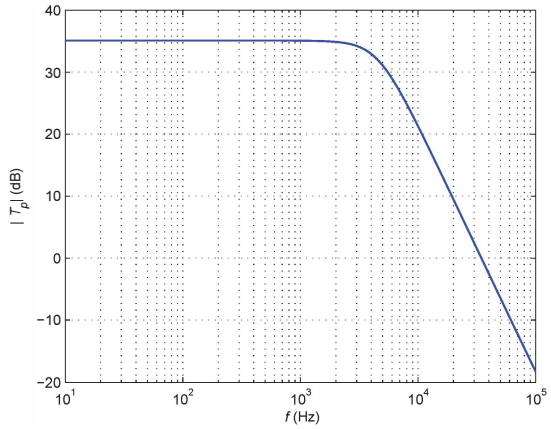

Fig. 6. Theoretically obtained magnitude plot of duty cycle-to-output voltage transfer function T_p.

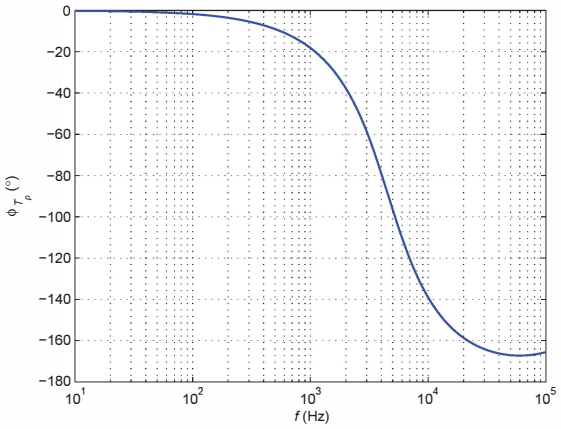

Fig. 7. Theoretically obtained phase plot of duty cycle-to-output voltage transfer function T_p.

The magnitude and phase plots of the duty cycle-to-output voltage transfer function using (20) as a function of frequency are as given in Fig. 6 and Fig. 7, respectively. A dc gain of $T_{p0} = 35.79$ dB$= 58.14$ V/V was obtained and the undamped natural frequency was observed at $f_o = \omega_o/2\pi = 4.5$ kHz. The frequency of the left-half plane zero was $f_z = \omega_z/2\pi = 530$ kHz. The assumed value of r_{C2} is very small yielding a high zero corner frequency. The damping coefficient calculated using (25) is $\xi = 1.12 > 1$. Therefore, the magnitude plot does not exhibit an overshoot at the natural frequency. The phase plot does not cross $-180°$ and is a characteristic of the minimum-phase systems such most of the buck-derived dc-dc converters. Therefore, establishing a control technique is relatively simple. The magnitude and the phase of input-to-output voltage transfer function M_v with respect to frequency as given in (28) are shown in Figs. 8 and 9. The response characteristics of M_v are similar to that of T_p and differ only in the values of the dc gain. Fig. 10 and Fig. 11 show the magnitude and phase of the input impedance Z_i as given in (34). At dc, the input resistance is governed by the load

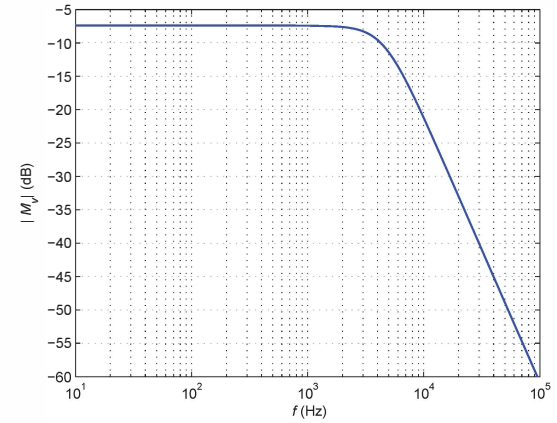

Fig. 8. Theoretically obtained magnitude plot of input-to-output voltage transfer function M_v.

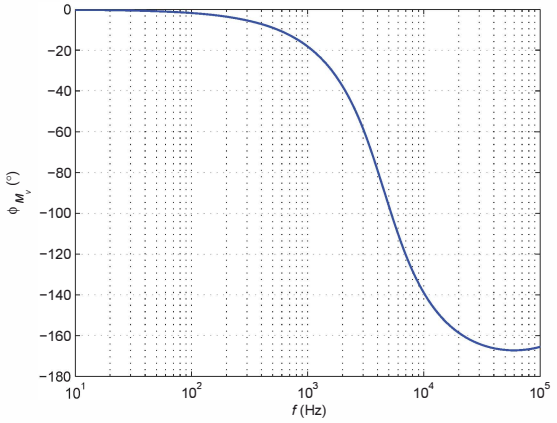

Fig. 9. Theoretically obtained phase plot of input-to-output voltage transfer function M_v.

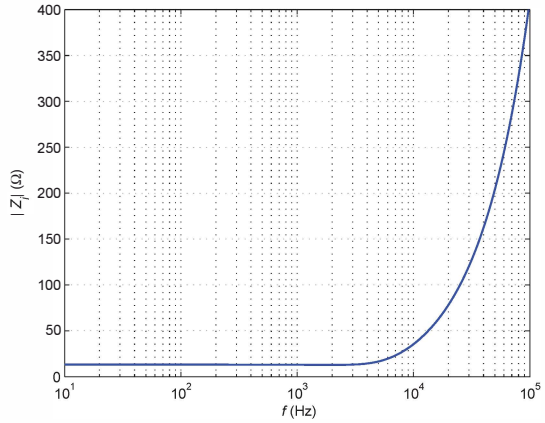

Fig. 10. Theoretically obtained magnitude plot of input impedance Z_i.

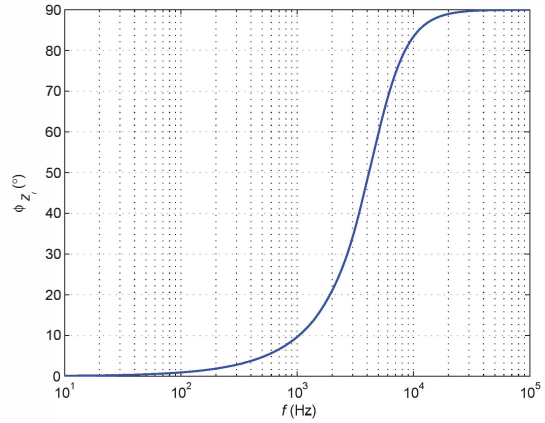

Fig. 11. Theoretically obtained phase plot of input impedance Z_i.

resistance as given in (36) and is equal to $R_{i0} \approx 13.06\ \Omega$. As the frequency increases, the input impedance increases, where the reactance of L_2 is significant. From the phase plot, one may observe that the phase is zero at dc and reaches 90° with increase in frequency showing the effect of the inductance L_2. The magnitude and phase of the small-signal output impedance of the dual-SEPIC dc-dc converter as provided in (38) are shown in Figs. 12 and 13. The value of the impedance at dc is $R_{o0} \approx 10\ \text{m}\Omega$ and agrees with (39). The output impedance increases with frequency and is inductive up to f_o. Beyond f_o, the output impedance decreases with increase in frequency and is capacitive.

B. Actual Circuit Simulations

The dual-SEPIC dc-dc converter shown in Fig. 1 was simulated on Saber circuit simulator for the values given in Section IV-A. A basic pulse-width modulator circuit was constructed. The carrier sawtooth voltage waveform with an amplitude of $V_{Tm} = 5$ V and a control voltage of $V_C = 1.5$ V were considered. A small-signal perturbation in the control voltage provided a small-signal variation in the duty cycle given by $d = v_c/V_{Tm}$ [2]. Fig. 14 shows a comparison of theory and simulations for T_p. Subsequently, the input voltage was perturbed about the operating point V_I by injecting a sinusoidal test voltage in series with V_I. Fig. 15 shows the comparison of theoretical and simulation results for M_v validating the predicted analysis.

C. Circuit with Four Reactive Components Described by Second-Order Transfer Functions

From the circuit of dual-SEPIC dc-dc converter shown in Fig. 1, one may speculate that the circuit is of fourth order due to the presence of two pairs of inductors and capacitors. However, the transfer functions derived in Section III are of second order. Based on the circuit operation [1], during the MOSFET ON interval, only one inductor and two series capacitors are present and the overall loop is of second order. Similarly, during MOSFET OFF interval, the loop presents two inductors and two capacitors both in series yielding second order state equations. Thus, the overall transfer function is that of the second order and the dominant effect is produced by the output stage comprising of the diode D_0 and the low-pass filter L_2, C_2, R_L. It must be noted that the reduction in the order is not inherent in the SEPIC converter and the transfer functions are of fourth order [3].

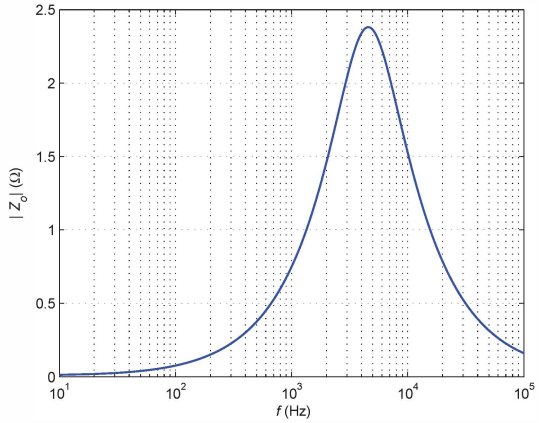

Fig. 12. Theoretically obtained magnitude plot of output impedance Z_O.

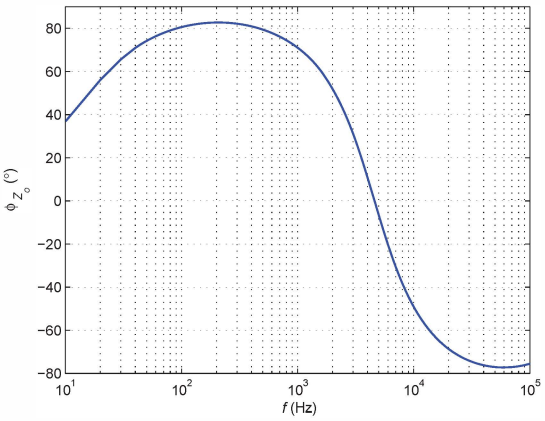

Fig. 13. Theoretically obtained phase plot of output impedance Z_O.

V. Conclusion

This paper has presented the derivation of a small-signal model of a dual-SEPIC dc-dc converter operating in continuous conduction mode. Using circuit averaging technique, the averaged and the large-signal models have also been developed. The following expressions have been derived: duty cycle-to-output voltage and input-to-output voltage transfer function, input impedance, and output impedance. The parasitic resistances have also been included in the model development. A design example has been considered and the properties of these transfer functions have been analyzed. Switched-circuit simulations have been performed on Saber circuit simulator to validate the correctness of the theoretically obtained transfer functions. Good agreement between the theoretical and simulation results was observed.

A practical explanation on how a dual-SEPIC dc-dc converter comprising of four reactive components yields second-order transfer functions has been discussed. It must be noted that this phenomenon does not occur in conventional SEPIC converters or Cuk converters, where fourth-order transfer functions are obtained. Therefore, designing closed-loop circuits for the dual-SEPIC converters is comparatively easier than those for the traditional SEPIC counterparts.

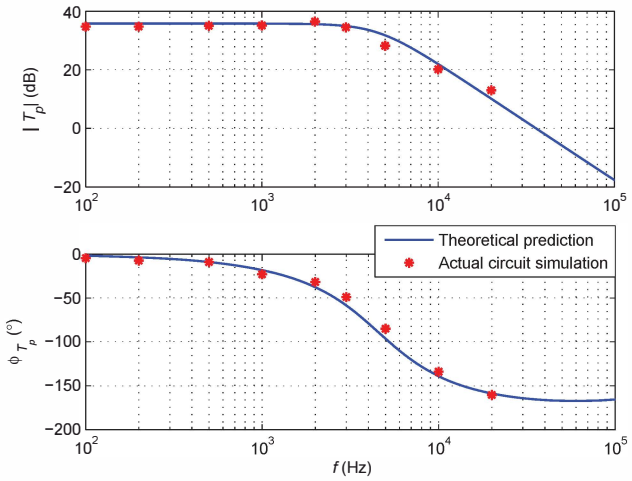

Fig. 14. Comparison of theoretical and simulation results for the duty cycle-to-output voltage transfer function.

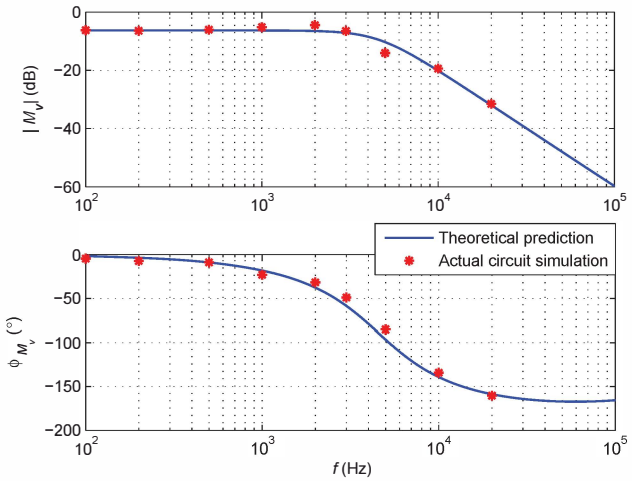

Fig. 15. Comparison of theoretical and simulation results for the input-to-output voltage transfer function.

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