A SIMPLIFIED I-Q DIGITAL MULTICARRIER DEMODULATOR

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ABSTRACT
Regenerative, on-board Processing FDMA/TDM payloads have been recently proposed as valid candidates for user-oriented satellite systems. Both business traffic for fixed service and mobile satellite systems can potentially take advantage of the peculiarities of such payloads, which substantially require multicarrier demodulation (MCD) of the uplink FDMA carriers to recover the individual modulating streams, which are in turn TDM-formatted to modulate a unique downlink carrier. Therefore two main functions are implemented by a MCD: the demultiplexing (DEMUX) and the demodulation (DEMOD). We focus here only on a digital implementation of the MCD looking at its advantages, flexibility, better performance and VLSI integrability. This paper is concerned with suitable digital techniques to implement on-board MCD. In particular the impact of the use of a kind of network clock synchronization on the overall MCD complexity is investigated in detail. The digital architecture of the proposed MCD can be adapted to different digital modulation techniques. However, we focus here only to the application for QPSK signals, considering the interest of this modulation scheme for digital satellite communications.

I INTRODUCTION

The evolution of satellite communications requires advanced satellite which can operate with earth stations with reduced complexity. This paper is concerned about satellite with on board processing capability. in particular, an on board processing system which receives an input FDMA signal and supplies an output to interface the TDM links is considered. Therefore it must accomplish the function of the separation of each individual radio channel and its demodulation and its correct switching to the appropriate downlink channel. An appropriate name for the on board processing system performing the first two operations is the "multicarrier demodulator" (MCD). Two main functions are implemented by a MCD: the demultiplexing (DEMUX) and the demodulation (DEMOD). The focus here is only on a digital implementation of the MCD [1],[2] because in perspective it offers several advantages such as flexibility, VLSI integrability, better efficiency.

II DEMULTIPLEXER WITH INTEGRATED I-Q SPLITTING

The demultiplexing of a FDMA signal can be performed following two basic approaches: block methods and per-channel methods. A complete survey of demultiplexing techniques is presented in [1]. The aim of this paper is to show that separation of I-Q components of the incoming QPSK signal can be efficiently performed in the DEMUX. Therefore, we focus here on the Analytic Signal (AS) approach, which is a per-channel approach able to exploit this possibility. A detailed description of the AS principle is given in [1]-[3] and for the sake of brevity it will not be recalled here. The structure of the DEMUX according to the AS method is shown in Fig. 1 (DEMUX section). The FDMA input signal, after appropriate analog down-conversion of the received signal to a low frequency range, is sampled according to the sampling theorem at the high-rate frequency $f_u=1/T_u$ and processed in order to obtain N_c TDM digital signals, each sampled at the low-rate frequency $f_d=1/T_d=f_u/N_c$, N_c being the number of multiplexed channels. In Fig. 1 $H_i(fT_u)$, $H'_i(fT_u)$ represent the conjugate symmetric and antisymmetric parts, respectively, of the high-rate complex bandpass filter $H_i(fT_u)$ which can be regarded as a frequency translated version of a low-pass prototype $H(fT_u)$ such that :

$$H_i(fT_u)=H_i(fT_u)+jH'_i(fT_u)=H[2\pi(f-iW-W/2)T_u] \qquad (1)$$

where W is the channel spacing. In the same figure, $G_i(fT_d)$ represents a real low-rate filter. which integrates the required pulse-shaping function. At the output of the high-rate filters $H_i(fT_u)$,$H'_i(fT_u)$ we have the real and imaginary part of the desidered QPSK signal. Through the decimation operation by a factor N_c equal to the number of the input channels a translation to baseband of these two signals is achieved. It is straighforward

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to verify that by performing the multiplications by the terms $\cos(n\pi/2)$, $\sin(n\pi/2)$ (which do not influence the DEMUX implementation complexity) shown in Fig. 1, after low pass filtering (filters $G(fT_d)$) the separation of I-Q components of the received QPSK signal is obtained. It is evident from Fig. 1 that the integration of the pulse-shaping filtering and separation into I-Q components of the QPSK signal into the low-rate stage of the DEMUX avoids the use of additional low pass filter in the DEMOD and therefore reduces the implementation complexity of the MCD. Another interesting feature of the implementation structure of Fig. 1 is that only processing of real quantities is required. The overall number of operations required per input channel and per second can be estimated as a function of the channel spacing W, the number of channels N_c and the filtering bandwidth B as [2]:

$$M_{DEMUX} = KW^2[W(N_c+4)-2B(N_c+2)]/[(W-B)(W-2B)]$$

(mults/ch/sec)

$$A_{DEMUX} = 4W\{ K[N_cW/(W-B)+W/(W-2B)] - 1\}$$

(adds/ch/sec)

where K is given by:

$$K = -2\mathrm{Log}[5\delta_1\delta_2]/3$$

The terms δ_1 and δ_2 denote the overall acceptable in band and the out-of-band ripples respectively derived according to given system specifications; for example a filter design procedure is reported in [2]. It results from the previous equations that for specified values of B and N_c an optimum value fo the channel spacing W_o can be found in order to achieve the lowest M_{DEMUX}. However, taking into account that for the subsequent demodulation operation an integer number of samples per symbol is convenient a suboptimum value of W closest to W_o is generally used. To this end, a suitable choice of the DEMUX output sampling frequency 2W=1.5 R turned out to be equal to 3 samples/symbol, with R the transmission rate.

III ALTERNATIVES FOR DEMODULATOR IMPLEMENTATION

This section considers two alternatives for the digital implementation of a demodulator suitable for QPSK signals. In particular, simplified carrier and clock recovery approaches necessary to perform a coherent demodulation of the demultiplexed QPSK signals are described. The benefits introduced by the possibility of network clock synchronication in terms of a reduction of the overall MCD implementation complexity are also investigated.

a1 Nonlinear estimation method of QPSK-modulated carrier phase.

The block diagram of the phase estimator considered here is shown in Fig.1. Its principle of operation is described in [4]. Interesting feature of this carrier phase estimator are that preambles can be usually avoided and a short and defined acquisition time is required. The influence of a finite arithmetic implementation on the carrier estimated value can be derived only by simulations. In Fig.2 the mean square error on the carrier phase is shown as function of E/N_o, with E the energy-per-bit and N_o the one-sided noise power density. A floating point implementation (curve a) and a finite arithmetic implementation with b_f = 6 bits (curve b) are considered. It can be noted from this figure that a carrier phase mean square error less than 5 degrees can be achieved for E/N_o greater than 5 dB with b_f =6 bits. This quantization loss can be significantly reduced by a more accurate quantization process. Naturally this has a direct impact on the size of the ROM. The implementation complexity of the proposed carrier phase estimator method, taking into account that the separation into I-Q components of the QPSK signal is performed in the DEMUX, can be derived as:

$$A_v = 2\ (3N+1)\ R \quad \text{adds/sec}$$

by considering three samples per symbol and with N_E=2N+1 the number of processed symbols.

a.2 A simplified QPSK timing-error detector

The simplified QPSK timing-error detector approach presented herein avoids the use of any interpolation /decimation and uses three samples per symbol to perform symbol detection. The outputs of the low-rate filters of the DEMUX (G_1) which also carry out the pulse shaping with an appropriate roll-off factor, are two real sequences $\{y_I(.)\}$ and $\{y_Q(.)\}$. Timing information must be recovered from these sequences. Symbols are transmitted synchronously, spaced by the symbol interval. Each sequence has three samples per symbol and the samples are time-coincident between the in-phase sequence $\{y_I(.)\}$ and the quadrature one $\{y_Q(.)\}$. The main goal of the proposed timing-error detector is to correctly select the set of three samples that belong to the same symbol; in other words the timing correction for the

considered timing error detector algorithm consists to correctly partitioning the received samples into sets of three samples, each set belonging to a unique symbol. The implementation complexity of the proposed timing estimation method can be derived as:

$A_c = 1.5\ R$ adds/sec

By comparing the implementation complexity of the proposed method with that of other digital approaches, as for example that proposed by Gardner in [5], it is evident that a considerable reduction is achieved. However, the method proposed by Gardner [5] introduces lower degradation than the simplified approach considered in this section. Lastly, it can be said that the simplified timing-error detector method represents a suitable choice for MCD systems in which the overall implementation complexity, and therefore the power consumption, is the primary concern and a tradeoff with the degradation introduced is possible.

b. Clock synchronous system

This section considers the benefits of the use of a network clock synchronization on the DEMUX and DEMOD design. Indeed, when all the carriers are clock synchronized at the satellite receiver, only one sample per symbol at the optimum decision time instant can be used at the DEMOD input. For the AS approach the use of a network clock synchronization results in a reduction in the implementation complexity. Indeed in this case only one sample per symbol is required at the DEMUX output. Therefore, by maintain unchanged the signal bandwidth and the channel spacing, a frequency sampling reduction by a factor of three can be included in the low-rate stage of the DEMUX. The number of multiplications required per channel and per second is now given by:

$$M_{DEMUX} = 2KW^2 \{ 2/[3(W-2B)] + N_c/[2(W-B)] \}$$

$$A_{DEMUX} = 4W\{ K[N_cW/(W-B)+W/3(W-2B)] - 2/3\}$$

From the previous equation it can be noted that a significant reduction for M_{DEMUX} and A_{DEMUX} is achieved making use of the network clock synchronization. Moreover, it can be pointed out that also the carrier recovery circuit can be simplified making use of a network clock synchronization. In fact, taking into account that the carrier phase estimation method presented in sect. a.1 can operate with only one sample per symbol, the implementation complexity results to be :

$A_{DEMOD} = 2N\ R$

For the clock recovery only one clock error estimator is required for all the N_c channels. It can estimate the clock error operating in time sharing on all the channels. Hence the contribution on the overall MCD implementation complexity due to the clock recovery circuit is pratically negligible.

IV SYSTEM DESIGN AND PERFORMANCE

The MCD design is discussed in this section. The two different DEMOD implementation techniques are considered. To this regard an important consideration to be made is that the number of channels processed by the DEMUX (N_c) influences the input sampling frequency and conseguently the processing rate and the complexity of the first stage of the MCD. In particular, a feasible constraint is to require that the input A/D converter sampling frequency (clock) should be close to its maximum possible value. Starting from these considerations, as the design goal, we have selected N_c=8 and N_c=10 at R=2048 Kbit/sec. The design of the DEMUX according to the AS approach is first presented. The high-rate and low-rate lowpass prototypes have been designed as a FIR linear phase filter by using the equiripple method [6]. It can be noted that the low-rate lowpass prototype has been designed to include the required pulse-shaping function with a 40% roll-off factor equally shared between the transmitter and the receiver. The implementation complexity in terms of multiplications per second and per channel is reported in tab.1 for the different considered values of N_c. A finite arithmetic implementation is necessarily required to implement any digital processing system. To this end, the filtering specifications and the DEMUX finite precision design has been derived to introduce at each demultiplexer output a suitable degradation, with respect to the input signal-to-noise ratio SNR_i [2]. The finite arithmetic wordlengths are reported in tab. 2. In Fig. 3 the degradations in dB for the output signal-to-noise ratio introduced by the digital implementation of the DEMUX are reported as function of E/N_0. It can be noted that there is a good agreement between the results derived through the theoretical analysis [2] and those obtained through computer simulations. Moreover, it should be said that the theoretical analysis considers the worst case degradation. The overall DEMOD implementation complexity results equal to 69.5 R (adds/ch/sec) with N_E=23 . The degradation of the DEMOD (DEMOD loss) are due to the phase jitter introduced by the carrier phase estimate and to a symbol timing offset introduced by the symbol timing estimate. In

order to obtain an evaluation of the loss due to the phase jitter and symbol timing offset, we have assumed them as two independent noise contributions. The loss due to a phase jitter can be derived through the following equation [7]:

$$Loss(dB) = 4.34\ (1+2\Omega)[1+(1+2\Omega)/2\alpha]/\alpha$$

where Ω is equal to E/N_o and α for moderate to high signal-to-noise ratios, can be assumed equal to $1/\sigma_\Theta^2$ with σ_Θ the root-mean-square (r.m.s.) value of the phase error. The degradation is reported in Fig. 4 as function of E/N_o with a finite precision implementation at 6 bits. In the same figure the degradation due to the symbol timing offset, also including the effect of a finite precision implementation at 6 bits, are also reported. The benefits of the use of a network clock synchronization on the MCD design are now illustrated. The resulting DEMUX and DEMOD implementation complexity (not including the common clock recovery circuit) in terms of number of multiplications per channel and per second is reported in Tab. 3 for N_c=8 and R=2048 Kbit/sec.. In the same table the achieved implementation complexity for DEMUX and DEMOD, without using network synchronization, is also reported for comparison purposes. From the previous results it can be pointed out that, when a network clock synchronization is used, a reduction for the overall MCD implementation complexity is achieved.

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N_c	R (kbit/s)	L_H	L_G	M_{DEMUX} XR (mults/ch/sec.)
8	2048	35	27	66.75
10	2048	44	27	73.5

Tab. 1 - Demux implementation complexity.
L_H = High-rate low-pass filter coefficients number;
L_G = Low-rate low-pass filter coefficients number.

N_c	R	Input Signal Quantization	Filters $H(fT_d)$			Filters $G(fT_d)$		
	(kbit/s)	b_q	b_c	b_m	b_a	b_c	b_m	b_q
8	2048	8	12	11	8	11	11	8
10	2048	8	12	11	8	11	11	8

Tab. 2 - Finite arithmetic DEMUX design.
b_q = input signal wordlengh;
b_c = filter coefficient wordlengh;
b_m = filter arithmetic wordlengh;
b_a = filter output wordlengh.

	DEMUX		DEMOD	
	A_{DEMUX}	M_{DEMUX}	A_{DEMOD}	M_{DEMOD}
With Net. Sync. XR	130	39.75	22	0
Without Net. Sync. XR	183	66.75	69.5	0

Tab. 3 - DEMUX and DEMOD implementation complexity for N_c=8 and R=2048 Kbit/sec.

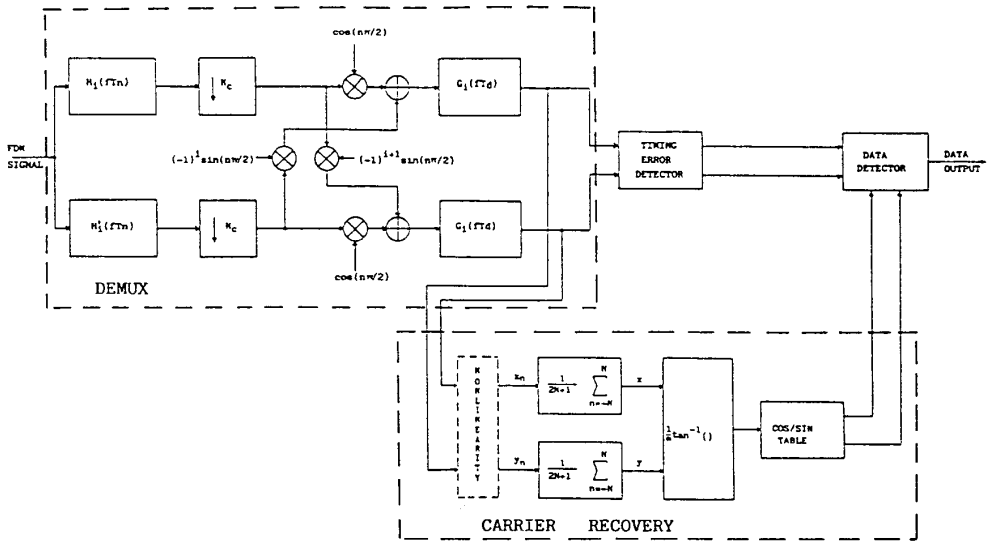

Fig. 1 - Implementation block diagram of the MCD.

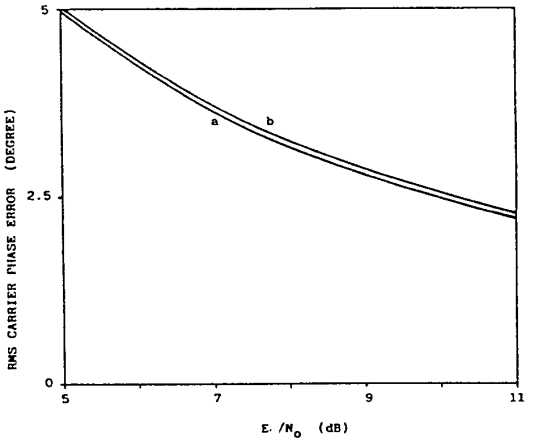

Fig. 2 - Carrier phase error as function of E/N_0.
a) floating point implementation;
b) finite precision implementation at 6 bits.

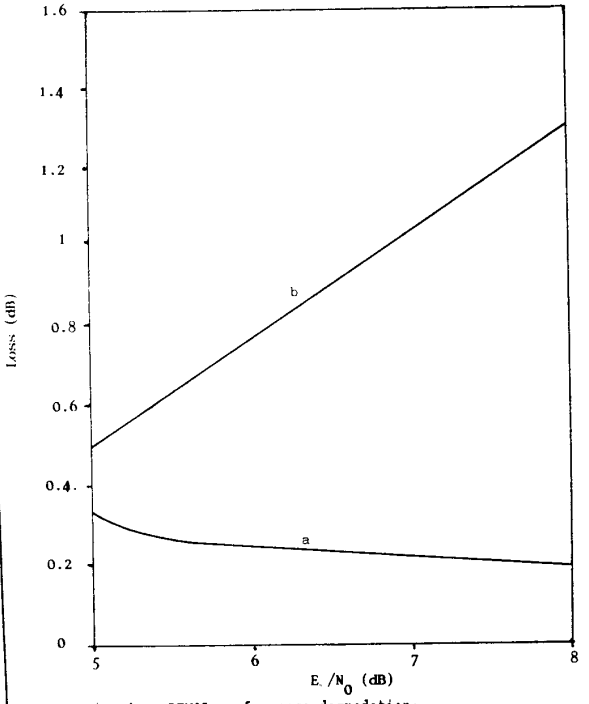

Fig. 4 - DEMOD performance degradation:
curve a) Carrier recovery loss with a finite precision implementation at 6 bits.
curve b) Symbol timing recovery loss with a finite precision implementation at 6 bits.

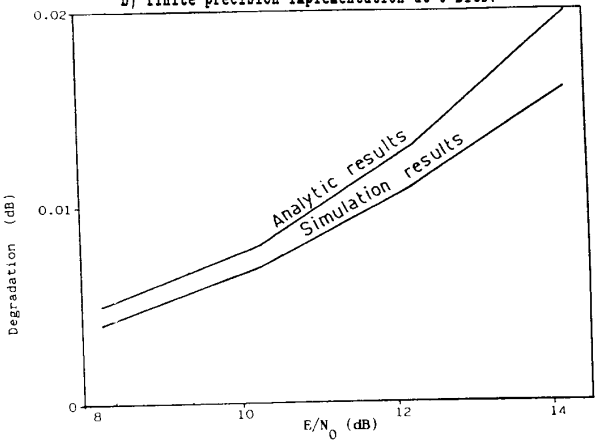

Fig. 3 - Performance degradation due to a finite precision implementation of the DEMUX (N_c=8,R=2048 Kbit/sec).