

# Duty Cycle and Input-to-Output Voltage Transfer Functions of Tapped-Inductor Buck DC-DC Converter

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**Abstract**—This paper presents a small-signal analysis of the power stage of a tapped-inductor pulse-width modulated (PWM) buck dc-dc converter, operating in continuous-conduction mode (CCM). Using the circuit averaging technique, the small-signal model of the power stage is developed. The derivation of duty cycle-to-output voltage and input-to-output voltage transfer functions are presented. An example tapped inductor buck dc dc converter is considered. The time-domain and frequency-domain characteristics of the converter are analyzed, illustrated, and discussed. The theoretical results are validated using circuit simulations.

## I. INTRODUCTION

Wide conversion ratio power electronic converters are attractive in a variety of applications, such as point-of-load power distribution system, data center power supplies, and solar photovoltaic modules. The tapped-inductor buck converter offers a higher voltage step-down than that of the traditional buck converter [1], [2]. The steady-state analysis of the common-diode tapped-inductor buck converter was analyzed in [3]. This paper presents the derivation of its small-signal model, and subsequently, its power stage transfer functions such as duty cycle-to-output voltage and input voltage-to-output voltage. The small-signal model of the converter has been derived using circuit averaging technique, where the nonlinear switching network is replaced by a linearized two-port network of controlled voltage and current sources [5]-[16]. The transient and frequency-domain characteristics of the converter are analyzed using the design of an example tapped-buck circuit topology and are verified through circuit simulations.

## II. AVERAGED, LINEAR, SMALL-SIGNAL MODEL

Fig. 1 shows the basic circuit of the PWM tapped-inductor dc-dc buck converter. The converter is supplied by a voltage source  $V_I$  to produce a dc output voltage  $V_O$ . The switching frequency is  $f_s$  and duty cycle is  $D$ . The load resistance is  $R_L$ . The tapped inductor comprises of an ideal transformer with turns ratio  $N = N_1/N_2$  and its magnetizing inductance  $L$  in parallel with secondary winding. The filter capacitor is  $C$  with equivalent series resistance  $r_C$ . The turns ratio of total number of turns to number of turns in the primary winding is

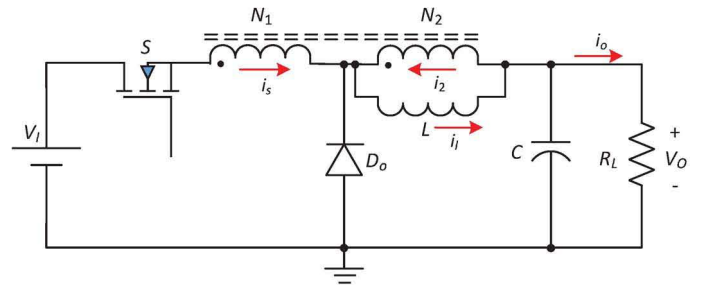


Fig. 1. Circuit of the PWM tapped-inductor buck converter.

$n = 1 + N$ . By the principle of circuit averaging, the switch current and diode voltage waveforms are averaged over one switching time interval. The average diode voltage is

$$V_D = \frac{DV_I}{D + n(1 - D)} \quad (1)$$

and the average switch current is

$$I_S = \frac{DI_O}{D + n(1 - D)}. \quad (2)$$

The switch can be replaced by a current-controlled current source and the diode by a voltage-controlled voltage source. A time-varying, nonlinear, large-signal model is obtained by perturbing the dc and low-frequency model [13] - [16]. The averaged linear small-signal model is obtained by eliminating the high-order non-linear terms from large-signal model. The linear small-signal model of tapped-inductor buck converter is shown in Fig. 2. The small-signal diode voltage is

$$v_d = k_1 d + k_2 v_i \quad (3)$$

and the small-signal switch current is

$$i_s = k_3 i_o + k_4 d, \quad (4)$$

where the coefficients  $k_1$ ,  $k_2$ ,  $k_3$ , and  $k_4$  are

$$k_1 = \frac{nV_I}{[D + (1 - D)n]^2}, \quad (5)$$

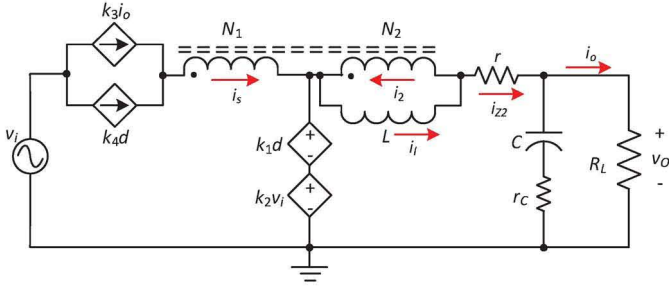


Fig. 2. Small-signal model of the PWM tapped-inductor buck converter obtained by circuit averaging technique.

$$k_2 = k_3 = \frac{D}{D + (1-D)n}, \quad (6)$$

and

$$k_4 = \frac{nI_O}{[D + (1-D)n]^2}. \quad (7)$$

The equivalent averaged resistance  $r$  connected in series with the secondary winding is [1], [2]

$$r = Dr_{DS} + (1-D)R_F + r_L, \quad (8)$$

where  $r_{DS}$  is the ON-resistance of the switch,  $R_F$  is the diode forward resistance, and  $r_L$  is the total parasitic resistance of the tapped inductor.

### III. DERIVATION OF TRANSFER FUNCTIONS

The small-signal model of the PWM buck-boost converter is shown in Fig. 2. The resulting state equations required to derive the transfer functions are as follows. The impedance in the inductor and capacitor branch are lumped and represented as

$$Z_1 = sL \quad (9)$$

and

$$Z_2 = R_L \parallel \left( r_c + \frac{1}{sC} \right) = \frac{R_L \left( r_c + \frac{1}{sC} \right)}{R_L + r_c + \frac{1}{sC}}. \quad (10)$$

The current through the parallel combination of the load resistor and the filter capacitor branch is

$$i_{Z2} = \frac{v_o}{Z_2} = i_l - i_2 = i_l - Ni_s. \quad (11)$$

Applying Kirchhoff's voltage law

$$k_1 d + k_2 v_i = i_l Z_1 + \left( \frac{r}{Z_2} + 1 \right) v_o. \quad (12)$$

Applying Kirchhoff's current law

$$i_s = k_3 i_o + k_4 d. \quad (13)$$

#### A. Duty Cycle-to-Output Voltage Transfer Function $T_p$

The duty cycle-to-output voltage transfer function is obtained by setting  $v_i = 0$  in Fig. 2. The control-to-inductor

current transfer function in s-domain is

$$\begin{aligned} T_p(s) &= \frac{v_o(s)}{d(s)} \Big|_{v_i=i_o=0} = T_{px} \frac{(s + \omega_{zn})(s - \omega_{zp})}{s^2 + 2\xi\omega_0 s + \omega_0^2} \\ &= T_{po} \frac{\left(1 + \frac{s}{\omega_{zn}}\right) \left(1 - \frac{s}{\omega_{zp}}\right)}{\left(\frac{s}{\omega_0}\right)^2 + \frac{2\xi s}{\omega_0} + 1}, \end{aligned} \quad (14)$$

where the dc gain  $T_{po}$  is

$$T_{po} = -\frac{R_L k_1}{R_L + r} = -\frac{R_L V_I}{R_L + r} \frac{N + 1}{[1 + (1-D)N]^2}. \quad (15)$$

From [4] the dc voltage gain is given by

$$M_{VDC} = \frac{V_O}{V_I} = \frac{D}{1 + N(1-D)}. \quad (16)$$

Substituting (16) into (15) results into

$$T_{po} = -\frac{R_L V_O}{R_L + r} \frac{N + 1}{D[1 + (1-D)N]} \quad (17)$$

The high-frequency gain  $T_{px}$  is

$$T_{px} = -\frac{k_4 N R_L r_c}{R_L + r_c} = -\frac{V_O r_c}{R_L + r_c} \frac{N(N + 1)}{[1 + (1-D)N]^2}, \quad (18)$$

the angular corner frequency or the angular undamped natural frequency is

$$\omega_0 = \sqrt{\frac{r + R_L}{LC(R_L + r_c)} \frac{1 + N(1-2D)}{1 + N(1-D)}}, \quad (19)$$

the damping ratio is

$$\begin{aligned} \xi &= \frac{L + C(1 - Nk_3)[rR_L + r_c(r + R_L)]}{2\sqrt{LC(R_L + r_c)(r + R_L)(1 - Nk_3)}} \\ &= \frac{L[1 + N(1-D)] + C[1 + N(1-2D)][rR_L + r_c(r + R_L)]}{2\sqrt{LC(R_L + r_c)(r + R_L)[1 + N(1-2D)][1 + N(1-D)]}}, \end{aligned} \quad (20)$$

the angular frequency of the left-half plane zero is

$$\omega_{zn} = \frac{1}{r_c C}, \quad (21)$$

and the angular frequency of the right-half plane zero is

$$\omega_{zp} = \frac{k_1(1 - Nk_3)}{LNk_4} = \frac{R_L [1 + N(1-2D)]}{L DN}. \quad (22)$$

where  $N = n - 1$ .

#### B. Input Voltage-to-Output Voltage Transfer Function $M_v$

The input voltage-to-output voltage transfer function is obtained by setting  $d = 0$  in Fig. 2. The input voltage-to-output voltage transfer function in s-domain as

$$\begin{aligned} M_v(s) &= \frac{v_o(s)}{v_i(s)} \Big|_{d=i_o=0} = M_{vx} \frac{s + \omega_{zn}}{s^2 + 2\xi\omega_0 s + \omega_0^2} \\ &= M_{vo} \frac{1 + \frac{s}{\omega_{zn}}}{\left(\frac{s}{\omega_0}\right)^2 + \frac{2\xi s}{\omega_0} + 1}, \end{aligned} \quad (23)$$

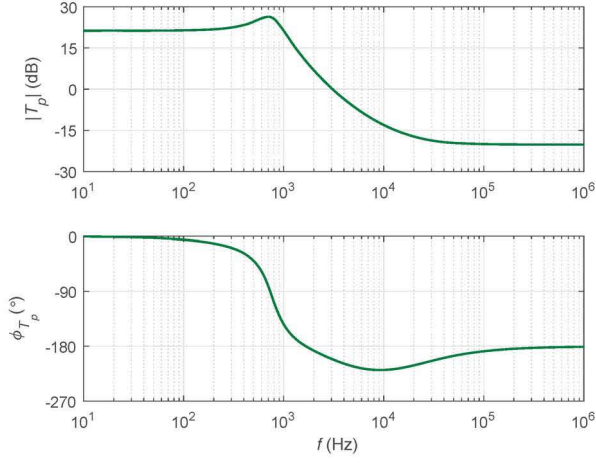


Fig. 3. Theoretically obtained magnitude and phase plots of  $T_p$  transfer function.

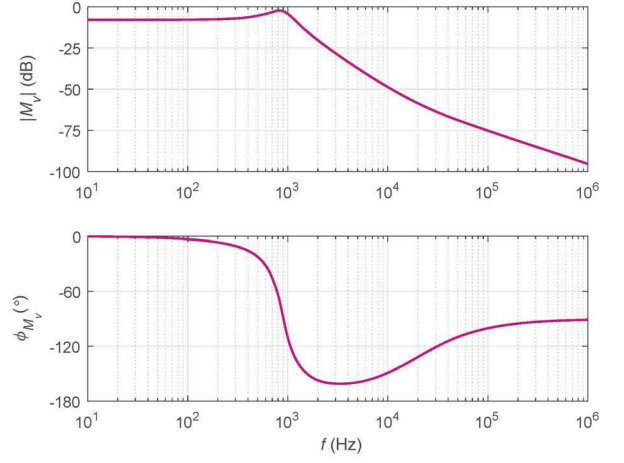


Fig. 5. Theoretically obtained magnitude and phase plots of  $M_v$  transfer function.

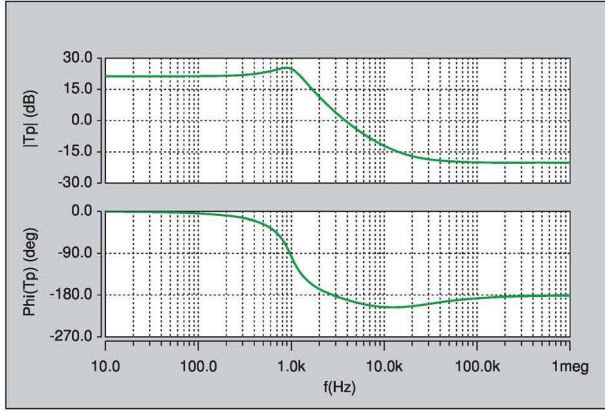


Fig. 4. Plots of magnitude and phase of  $T_p$  transfer function obtained using SABER simulator.

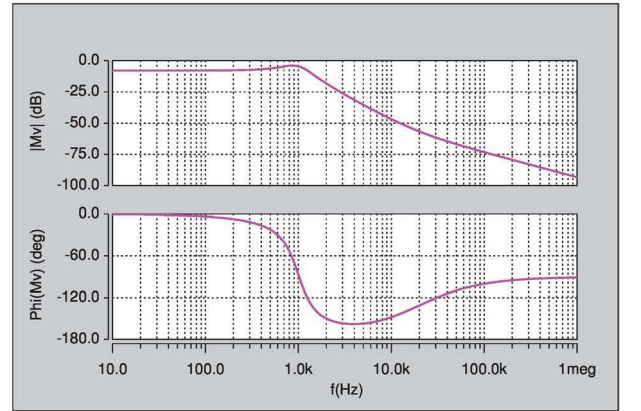


Fig. 6. Plots of magnitude and phase of  $M_v$  transfer function obtained using SABER simulator.

where

$$M_{vx} = \frac{(1 - Nk_3)k_2 R_L r_C}{L(R_L + r_C)} \quad (24)$$

$$= \frac{DR_L r_C}{L(R_L + r_C)} \frac{1 + N(1 - 2D)}{[1 + N(1 - D)]^2},$$

the dc gain  $M_{vo}$  is

$$M_{vo} = \frac{k_2 R_L}{r + R_L} = \frac{R_L}{r + R_L} \frac{D}{1 + N(1 - D)}, \quad (25)$$

and the angular frequency of the left-half plane zero is given in (21).

#### IV. RESULTS

The following specifications were considered for the analysis on the tapped-inductor buck converter: supply voltage  $V_I = 12$  V, output voltage  $V_O = 5$  V, output power  $P_O = 10$  W, load resistance  $R_L = 2.5 \Omega$ , switching frequency  $f_s = 100$  kHz, inductance to ensure CCM operation  $L = 150 \mu\text{H}$ , and filter capacitance  $C = 170 \mu\text{F}$ . Duty cycle  $D$  is 0.588. The turns ratio  $N = N_1/N_2 = 1$  to give  $n = 2$ . The equivalent series

resistance of the capacitor is  $r_C = 1 \text{ m}\Omega$  and the equivalent averaged resistance  $r \approx 0.1 \Omega$ .

Fig. 3 shows the theoretically obtained magnitude and phase plots of duty cycle-to-output voltage transfer function  $T_p$ . The gain at dc and low-frequencies is nearly  $T_{po} = 21.3 \text{ dB} = 11.6 \text{ V/V}$ . The natural corner frequency of the second-order low-pass filter formed by the inductor, capacitor, and load resistor is  $f_o = 767.6 \text{ Hz}$ . The left-half plane (LHP) zero is  $f_{zn} = \omega_{zn}/2\pi = 18.724 \text{ kHz}$ . The right-half plane (RHP) zero is  $f_{zp} = \omega_{zp}/2\pi = 3.7 \text{ kHz}$ . The circuit of tapped-inductor was constructed on SABER circuit simulator. The theoretical result was validated using the simulator. Fig. 4 shows the plots of magnitude and phase of  $T_p$  transfer function obtained using SABER circuit simulator.

Fig. 5 shows the theoretically obtained magnitude and phase plots of input voltage-to-output voltage transfer function  $M_v$ . The gain at dc and low-frequencies is nearly  $M_{vo} = -7.92 \text{ dB} = 0.4018 \text{ V/V}$ . The theoretical result was validated using SABER circuit simulator. Fig. 6 shows the plots of magnitude and phase of  $M_v$  transfer function obtained using

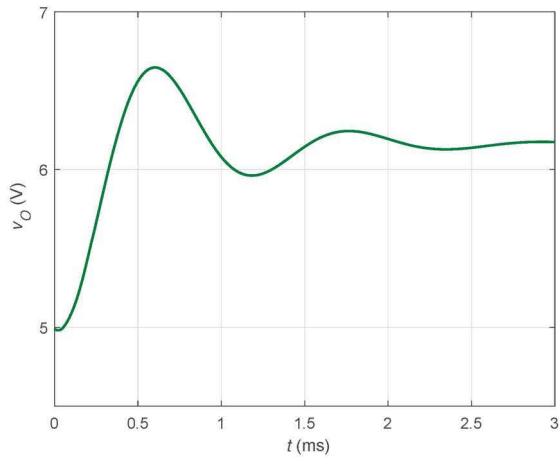


Fig. 7. Theoretical response of the output voltage  $v_O$  for a step change in duty cycle by  $\Delta D = 0.1$ .

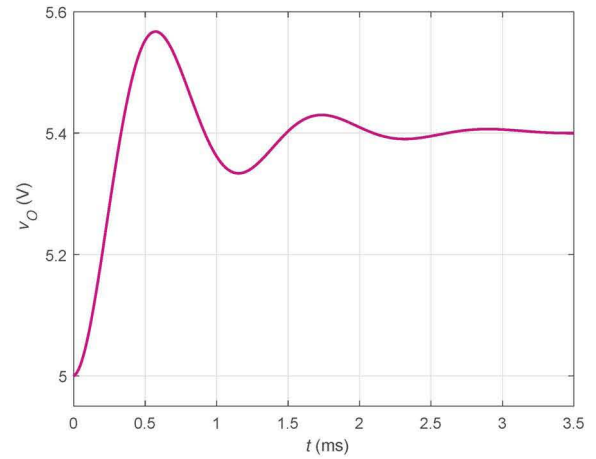


Fig. 9. Theoretical response of the output voltage  $v_O$  for a step change in input voltage by  $\Delta V_I = 1$ .

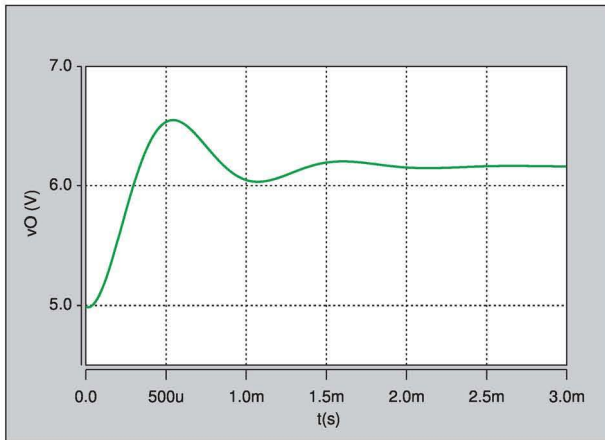


Fig. 8. Response of the output voltage  $v_O$  for a step change in duty cycle by  $\Delta D = 0.1$  obtained by SABER simulator.

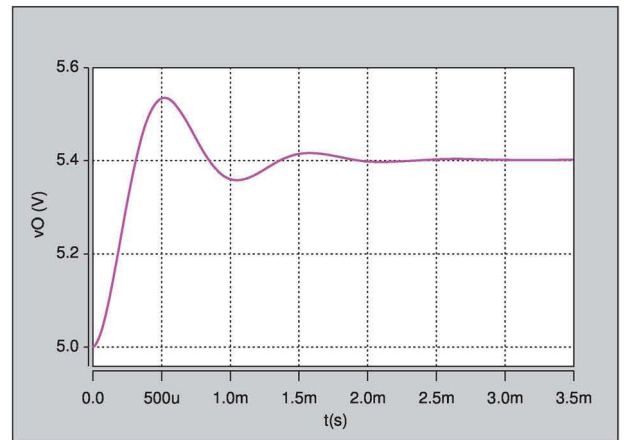


Fig. 10. Response of the output voltage  $v_O$  for a step change in input voltage by  $\Delta V_I = 1$  obtained by SABER simulator.

SABER circuit simulator.

Fig. 7 shows the theoretically obtained response of the output voltage  $v_O$  for a step change in duty cycle by  $\Delta D = 0.1$ . Fig. 8 shows the response of the output voltage  $v_O$  for a step change in duty cycle by  $\Delta D = 0.1$  obtained by SABER simulator. The undershoot in the output voltage response was observed due to the presence of the RHP zero at  $f_{zp} = \omega_{zp}/2\pi = 3.7$  kHz.

Similar analysis was performed for the input voltage-to-output voltage transfer function. The theoretically obtained and simulated responses of the output voltage for step change in the input voltage by  $\Delta V_I = 1$  V are shown in Figs. 9 and 10. A good agreement between theoretical and simulation results was observed.

## V. CONCLUSIONS

This paper has presented the derivation of the duty cycle-to-output voltage and the input voltage-to-output voltage transfer functions of the common-diode tapped-inductor buck

pulse-width modulated (PWM) dc-dc converter in continuous-conduction mode. The transfer functions have been derived using the small-signal model obtained by circuit averaging technique. An example converter was designed and simulated to validated the theoretically derived transfer functions. Excellent agreement between theoretical and simulations results were observed. The tapped-inductor buck converter is a non-minimum phase system as it exhibits a right-half plane (RHP) zero in its duty cycle-to-output voltage transfer function.

## REFERENCES

- [1] D. Czarkowski and M. K. Kazimierczuk, "Energy-conservation approach to modeling PWM DC-DC converters," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 29, no. 3, pp. 1059-1063, Jul. 1993.
- [2] M. K. Kazimierczuk, *Pulse-width Modulated dc-dc Power Converters*, 2nd Ed., John Wiley & Sons, Chichester, United Kingdom, 2015.
- [3] N. Kondrath and M. K. Kazimierczuk, "Analysis and design of common-diode tapped inductor PWM buck converter," in *Proc. Electrical Manufacturing and Coil Winding Conf.*, Nashville, TN, Sept. 2009.
- [4] A. Chadha, A. Ayachit, D.K. Saini, and M. K. Kazimierczuk, "Steady-state analysis of PWM tapped-inductor buck DC-DC converter in CCM,"

- in Proc. *IEEE Texas Power and Energy Conf.*, College station, TX, Feb. 2018.
- [5] B. Bryant and M. K. Kazimierczuk, "Voltage-loop power-stage transfer functions with MOSFET delay for boost PWM converter operating in CCM," in *IEEE Trans. Ind. Electron.*, vol. 54, no. 1, pp. 347-353, Feb. 2007.
- [6] B. Bryant and M. K. Kazimierczuk, "Voltage loop of boost PWM DCDC converters with peak current-mode control," *IEEE Trans. Circ. Systems-I: Regular Papers*, vol. 53, no. 1, pp. 99-107, Jan. 2006.
- [7] M. K. Kazimierczuk, "Transfer function of current modulator in PWM converters with current-mode control," *IEEE Trans. Circ. and Syst. I: Fundamental Theory and Applications*, vol. 47, no. 9, pp. 1407-1412, Sept. 2000.
- [8] R. D. Middlebrook, "Topics in multiple-loop regulators and current-mode programming," *IEEE Trans. Power Electron.*, vol. PE-2, no. 2, pp. 109-125, Apr. 1987.
- [9] F. D. Tan and R. D. Middlebrook, "A unified model for current-programmed converters," *IEEE Trans. Power Electron.*, vol. 10, no. 4, pp. 397408, Jul. 1995.
- [10] R. Redl and I. Novak, "Instabilities in current-mode controlled switching voltage regulators," in Proc. Power Electronics. Specialists. Conf., pp. 17-28, 1981.
- [11] —, "Small-signal duty cycle to inductor current transfer function for boost PWM dc/dc converter in continuous conduction mode," in *Proc. IEEE Intl. Symp. Circ. Syst.*, Vancouver, BC, Canada, May 23-26, 2004, pp. 856-859.
- [12] B. Bryant and M. K. Kazimierczuk, "Open-loop power-stage transfer functions relevant to current mode control of boost PWM converter operating in CCM," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 10, pp. 2158-2164, Oct. 2005.
- [13] A. Ayachit and M. K. Kazimierczuk, "Small-signal modeling of PWM boost dc-dc converter at boundary conduction mode by circuit averaging technique," in *IEEE Intl. Symp. Circ. and Syst.*, Lisbon, Portugal, May 2015, pp. 229-232.
- [14] A. Ayachit and M. K. Kazimierczuk, "Open-loop small-signal transfer functions of the quadratic buck PWM dc-dc converter in CCM," *IEEE Ind. Electron. Society Conf.*, Dallas, USA, November 2014, pp. 1643-1649.
- [15] D. K. Saini, A. Ayachit, and M. K. Kazimierczuk, "Small-signal analysis of closed-loop PWM boost converter in CCM with complex impedance load," in *IEEE Intl. Symp. Circ. and Syst.*, Montreal, Canada, May 2016, pp. 433-436.
- [16] D. K. Saini, A. Ayachit, M. K. Kazimierczuk, and T. Suetsugu, "Small-signal analysis of PWM boost converter in CCM with complex impedance load," in *IEEE Ind. Electron. Society Conf.*, Yokohama, Japan, November 9-12, 2015, pp. 3597-3602.