A Current-Source Sinusoidal Gate Driver for High-Frequency Applications

Hur Jedi and Marian K. Kazimierczuk
Department of Electrical Engineering
Wright State University, Dayton, OH 45435, USA
{jedi.2, marian.kazimierczuk}@wright.edu

Alberto Reatti
Department of Information Engineering
University of Florence, Florence 50139, Italy
alberto.reatti@unifi.it

***Abstract*—This paper proposes a new single-switch gate-driver circuit to drive a low-side power transistor at high frequencies with rapid turn-ON and turn-OFF transitions. The characteristics of the proposed topology include fast dynamic response, small energy storage requirements, and flexible design. Conventional gate drivers are used up to frequencies around 5 MHz and need at least two transistors. In this study, detailed description, design procedure, and power loss analysis of the proposed topology are presented. The introduced circuit exhibits fast switching speed and low gate-drive loss. Simulation and experimental results showing performance of the new topology are provided to validate the theory. The prototype of the gate driver for power transistors is designed, simulated, and tested at 20 MHz.**

***Index Terms*—Gate driver, power MOSFET driver, resonant gate driver, low switching loss, high-frequency ZVS operation.**

I. Introduction

With the advancement of the electronic industry, the demand for power converters with high density, high efficiency, and low cost is increasing [1]. The gate-driver circuit forms an important interface between a power electronic stage and a control stage [2]. Commonly used gate drivers such as class-D and class-DE, which have at least two transistors, can be used at frequencies up to about 5 MHz, [3], [4]. However, their suffering losses are very high. Many challenges encountered, while driving transistors at frequencies above 5 MHz. For example, in converter with multiple transistors, it is difficult to implement high-side gate driver and provide dead time on the order of a few nanoseconds [5], [6]. Therefore, a topology with a single switch such as that proposed in this paper has advantages, especially for operation at high switching frequencies [7]. The sizes of magnetic components and capacitors in the circuit are inversely dependent on frequency [8]. Therefore, the inductance in the proposed gate driver is reduced. Moreover, the output capacitance C_{oss} and the input capacitance C_{iss} of the power MOSFETs in the gate driver are small to minimize the switching energy loss [9], [10]. A soft-switching technique is utilized to reduce switching loss in the driving power MOSFET [11]. Thus, the switching loss is alleviated. Since high operation frequencies increase switching loss, a loss analysis of the gate driver is presented to predict the overall loss. The main objectives of this paper are to introduce a new topology of gate-drive circuit to drive power transistors at high frequency and to present its analytical equations. The operation of the proposed gate-drive circuit is explained in detail. The presented topology is based on Class-E circuit,

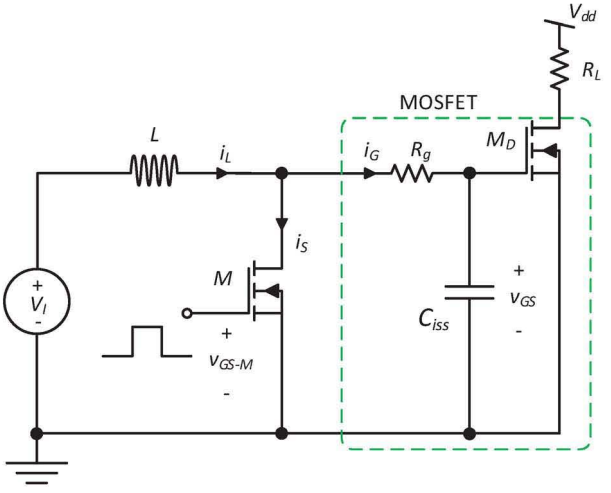

Fig. 1. Proposed single-switch gate-drive circuit.

which increases the output voltage with respect to the input voltage [12], [13]. Therefore, it can drive a power MOSFET even when low voltage is available. The new design achieves small passive energy storage components, fast response, and low design complexity. These advantages make the proposed gate-driver topology suitable for applications that require high frequency operation such as RF power converters and telecom power supplies.

II. Design of Proposed Gate Driver Topology

Fig. 1 shows the proposed single-switch gate-drive circuit. It consists of a DC input voltage V_I, a switch M, and an inductor L. The switch M is a power MOSFET and its source is connected to the ground. It is desirable that the drain-source voltage waveform of the driver switch M satisfies zero-voltage-switching (ZVS) and allows for variable duty ratio. The inductor L behaves like a current source to supply the charge to the power transistor input capacitance C_{iss}. The voltage v_{GS} is the gate-source voltage across the transistor input capacitance C_{iss}, which should be charged and discharged. We focus on identifying characteristic network in the circuit and provide a flexible value of duty cycle to the driven power MOSFET M_D to achieve a rapid turn-ON and turn-OFF of drain-source voltage. The analysis is based on the ON-state and the OFF-state of the switch M. For the ON interval, the transistor M behaves as a switch with a resistance

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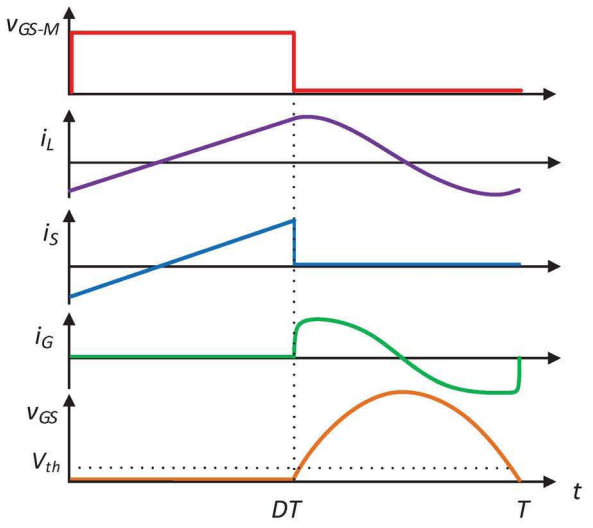

Fig. 2. Waveforms of the proposed gate driver. From top to bottom: drive signal, inductor current, switch current, gate current, and gate-source voltage.

r_{on}. It operates with an infinite resistance during the OFF interval. The current flowing through the capacitances C_{oss} and C_{iss} forms a soft-switching voltage at both transitions. The driving transistor M is operating under ZVS condition, eliminating the switching losses. The switch M can be driven at any duty cycle D, which is determined as switch ON time t_{on} divided by the total period T. The ideal waveforms of the proposed gate driver over one period are shown in Fig. 2. The circuit operation is explained in two operating modes depending on the switch M state.

A. Switch-ON $\quad 0<t \leq DT$

In this time interval, the power transistor M is ON and its drain-source voltage is zero. The output voltage across the capacitance C_{iss} is zero because the voltage across the switch M is zero. The switch current i_S is equal to the inductor current i_L, while the gate current i_G is zero. Therefore, the capacitance C_{iss} is discharged during this time interval and the power MOSFET M_D remains OFF. When the switch M is ON, the voltage across the inductor v_L is equal to the input voltage V_I. During this interval, the inductor current i_L increases linearly and its waveform starts from an initial value $i_L(0)$. Since the switch M is ON, the voltage across the inductor is equal to the input voltage V_I.

$$i_L(t) = \frac{1}{L}\int_0^t v_L(t)dt + i_L(0) = \frac{V_I}{L}t + i_L(0). \tag{1}$$

At the end of this interval, the inductor current i_L at DT is

$$i_L(DT) = \frac{V_I}{L}(DT) + i_L(0). \tag{2}$$

Hence, the peak-to-peak inductor current ripple over a time interval DT is

$$\Delta i_L = i_L(DT) - i_L(0) = \frac{V_I D}{f_s L} = \frac{2\pi D V_I}{a\omega_o L} = \frac{2\pi D V_I}{a Z_o}, \tag{3}$$

where f_s is the switching frequency and $a = f_s/f_o$. From (3),

$$i_L(0) = -\frac{\Delta i_L}{2} = -\frac{DV_I}{2f_s L} = -\frac{\pi D V_I}{aZ_o} = -i_L(2\pi D). \tag{4}$$

During this interval, the inductor current i_L is flowing through the switch M. In other words, the switch M supports a low-impedance path to the ground. Thus, the switch current i_S is

$$i_S(t) = \begin{cases} i_L(t) & 0<t \leq DT \\ 0 & DT<t \leq T. \end{cases} \tag{5}$$

B. Switch-OFF $\quad DT<t \leq T$

In this time interval, the power transistor M is OFF and its current i_S is zero. Thus, the gate-source voltage of the power switch M_D rises from zero to a maximum value and then decreases to zero as shown in Fig. 2. During this interval, the inductor operates as a current source that supplies the charge to the driven transistor input capacitance C_{iss} and the gate current i_G is equal to the inductor current i_L. The following assumptions are made: a) the capacitance C_{iss} is linear and its initial value is zero, b) the gate resistance R_g and the inductor resistance r_L are neglected. Since $i_C = i_L = i_G$,

$$(C_{iss} + C_{oss})\frac{dv_{GS}(t)}{dt} = \frac{1}{L}\int_{DT}^{t} v_L dt = \frac{1}{L}\int_{DT}^{t}\left[V_I - v_{GS}(t)\right]dt. \tag{6}$$

By taking the derivative of both sides with respect to time,

$$\frac{d^2 v_{GS}}{dt^2} + \frac{v_{GS}}{(C_{iss}+C_{oss})L} = \frac{V_I}{(C_{iss}+C_{oss})L}. \tag{7}$$

Equation (7) is a second-order non-homogenous differential equation. The solution of this equation has two components: general solution (homogenous) and particular solution, to give the total solution as

$$v_{GS}(t) = V_I + A\cos(\omega_o t) + B\sin(\omega_o t), \tag{8}$$

where the resonance angular frequency is

$$\omega_o = \frac{1}{\sqrt{L(C_{iss}+C_{oss})}}, \tag{9}$$

C_{oss} is the output capacitance of the driving transistor M, and C_{iss} is the input capacitance of the driven transistor M_D. A and B are arbitrary constants. To solve constants A and B, two initial conditions are needed. The gate-source voltage v_{GS} is known to be 0 at $t = DT^+$ because the transistor M turns OFF at $t = DT$. In other words, the gate driver provides $v_{GS} = 0$ just before the power MOSFET M_D turns ON. Thus,

$$\begin{aligned} v_{GS}(\omega_s t) = V_I\Big[1 - \cos\frac{1}{a}(\omega_s t - 2\pi D) \\ + \frac{\pi D}{a}\sin\frac{1}{a}(\omega_s t - 2\pi D)\Big], \end{aligned} \tag{10}$$

where

$$a = \omega_s/\omega_o \quad \text{and} \quad Z_o = \sqrt{\frac{L}{C_{iss}+C_{oss}}}. \tag{11}$$

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TABLE I
LIST OF COMPONENTS FOR GATE DRIVER AT $f_s = 20$ MHz

Components	Value
L, r_L	192.48 nH, 0.1 Ω
Si MOSFET M, M_D	VRF148A $C_{iss} = 160$ pF, $C_{oss} = 40$ pF, $C_{rss} = 2.6$ pF $V_{DS} = 170$ V, $I_{DS} = 6$ A, $R_g = 0.3$ Ω $Q_g = 3.2$ nC, $r_{DS} = 1.2$ Ω

As aforementioned, the gate current supplies the charge to the input capacitance C_{iss} and pulls the charge from the input capacitance when the switch M OFF. The gate current is expressed as

$$i_G(\omega_s t) = \frac{V_I}{Z_o}\Big[\sin\frac{1}{a}(\omega_s t - 2\pi D) + \frac{\pi D}{a}\cos\frac{1}{a}(\omega_s t - 2\pi D)\Big]. \tag{12}$$

Setting the ZVS condition $v_{GS}(2\pi) = 0$ in (10) yields the relationship between a and D

$$1 - \cos\frac{1}{a}2\pi(1-D) + \frac{\pi D}{a}\sin\frac{1}{a}2\pi(1-D) = 0. \tag{13}$$

This solution of this transcendental equation produces $a = 0.7742$ for $D = 0.5$. The maximum value of v_{GS} occurs at $\omega_s t_v = 4.6946$ rad $= 268.98°$ and it is $V_{GSmax}/V_I = 3.2629$ for $D = 0.5$. The specifications of the proposed gate-driver components are given in Table I.

C. Loss Analysis

Due to switch power on-resistance r_{on}, the conduction loss is determined by calculating the rms current $I_{S(rms)}$ of the switch current i_S. When the switch M is ON, the switch current i_S can be expressed

$$i_S = \frac{V_I}{L}t - \frac{V_I}{2L}DT, \tag{14}$$

yielding rms current $I_{S(rms)}$ of the switch

$$I_{S(rms)} = \sqrt{\frac{1}{T}\int_0^{DT} i_S^2(t)\,dt} = \frac{V_I}{\sqrt{12}f_s L}D\sqrt{D}. \tag{15}$$

The conduction power loss in the switch M is

$$P_{r_{on}} = I_{S(rms)}^2 r_{on} = \frac{D}{12}\left(\frac{V_I D}{f_s L}\right)^2 r_{on}. \tag{16}$$

To determine the loss dissipation in the internal gate resistance R_g of the power transistor M_D, assuming that I_G is the root-mean-square (rms) value of the gate current. It flows through the gate terminal of the power transistor during t_{on} and t_{off} respectively. According to (12), the rms value of the gate current i_G is

$$I_{G(rms)} = \sqrt{\frac{1}{T}\int_{DT}^{T} i_G^2(t)\,dt} = \frac{V_I(1-D)}{f_s L}\sqrt{\frac{1-D}{12}}. \tag{17}$$

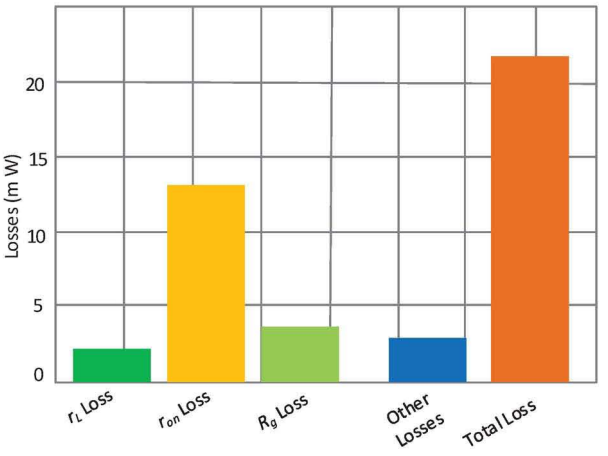

Fig. 3. Calculated losses at V_I = 4 V and 20 MHz switching frequency.

In the gate resistance R_g of the power MOSEFT at switching frequency f_s, the power dissipated is

$$P_{Rg} = I_{G(rms)}^2 R_g = \frac{V_I^2(1-D)^2}{f_s^2 L^2}\left(\frac{1-D}{12}\right). \tag{18}$$

The conduction power loss in the inductor L is dissipated in the internal resistance r_L of the device. Since air-core inductor is used, the inductor core power losses are negligible. To compute the rms of the inductor current i_L, we can assume that the transition of current i_L in complete switching period T is approximately a triangular with peak-to-peak Δi_L [14]. The rms inductor current $I_{L(rms)}$ is

$$I_{L(rms)} = \sqrt{I_{Srms}^2 + I_{Grms}^2} = \frac{V_I}{f_s L}\sqrt{\frac{D^3 + (1-D)^3}{12}}. \tag{19}$$

The inductor conduction loss is

$$P_{r_L} = I_{L(rms)}^2 r_L = \frac{V_I^2}{f_s^2 L^2}\left[\frac{D^3 + (1-D)^3}{12}\right] r_L. \tag{20}$$

From the above equations of loss analysis, we determine the total dissipative power loss P_{diss} in the gate driver as follow:

$$P_{diss} = P_{rL} + P_{Rg} + P_{r_{on}}. \tag{21}$$

III. DESIGN, SIMULATION, AND EXPERIMENTAL RESULTS

A. Gate-Driver Design

The gate driver is designed for the switching frequency $f_s = 20$ MHz. The driving and driven transistors were VRF148A, whose data are listed in Table I. The resonance frequency was $f_o = f_s/a = 20 \times 10^6/0.7742 = 25.833$ MHz. The total capacitance $C = C_{ds(MD)} + C_{iss(M)} = C_{oss} - C_{rss} + C_{iss} = 40 - 2.6 + 160 = 197.4$ pF. Hence, $L = 1/(C\omega_o^2) = 192.48$ nH, $Z_o = \sqrt{L/C} = 31.22$ Ω, and $Q = \omega_o L/(R_g + r_L) = 31.22/(0.3 + 0.1) = 78.05$. The supply voltage V_I was selected to be 4 V and load resistance R_L was 25 Ω. According to (21), the input current I_I is calculated and its value was 4.8 mA. The peak value of gate-source square voltage waveform v_{GS} of the driving transistor M was 4 V for $D = 0.5$, safely

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within the manufacturers rating of 40 V (4/40 = 0.1). The maximum value of gate-source voltage $V_{GSmax} = 3.2629 \times 4 = 13.05$ V. According to above loss analysis, the power losses are shown in Fig. 3 at 20 MHz switching frequency. The total loss of the proposed gate driver was 19.12 mW. The conduction loss P_{rL} in resonant inductor resistance r_L was 2.25 mW and the gate-resistance loss $P_{Rg} = 3.37$ mW. It can be noticed that the loss in on-resistor $P_{ron} = 13.5$ mW was dominant due to high on-resistance of the power switch M.

B. Simulation

Based on the circuit operation and design approach presented in Sections II, the gate driver was designed, and tested with a fixed resistive load of the driven MOSFET M_D. The Si power MOSFETs were utilized in the proposed gate driver and as a driven switch. The SaberRD software was used to observe the waveforms of the gate driver at constant switching frequency 20 MHz. The input voltage V_I was 4 V. To get ZVS, the components were adjusted so that $C = 280$ pF and $L = 135$ nH. The magnitude of the gate-source voltage depends on the duty cycle D. The maximum value of gate-source voltage V_{GSmax} was 13.72 V at $D = 0.5$ and $V_{GS(max)} = 22$ V at $D = 0.8$. Fig. 4 shows the inductor current, gate current, and gate-source voltage waveforms for the entire cycle. It can be noticed that the power transistor input capacitance C_{iss} is charged/discharged when the switch M is OFF. The gate-source and drain-source voltages of the driven power transistor M_D were captured during the turn-on transition as shown in Fig. 5. A quick turn-on transition time with large slew rate is observed (rising time 3 ns and falling time 4 ns), indicating that high-speed switching is achieved. The performance of the new gate driver proves many features that the topology has over conventional designs. Particularly, it proves high-speed transient response, small storage components, and low-design complexity for high-frequency operation.

C. Experimental Results

An VRF148A MOSFET (170 V, 6 A) from Microsemi Technologies was used as the switching device in the circuit. It

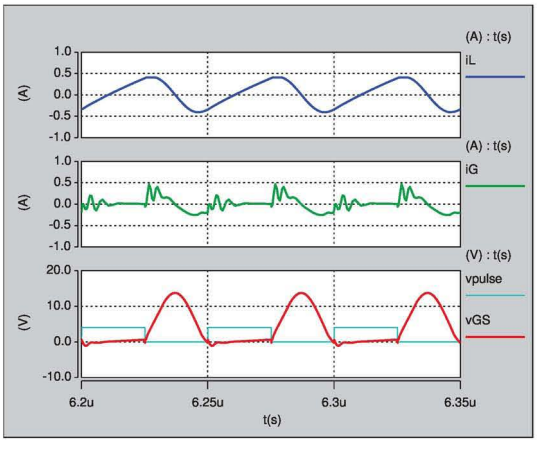

Fig. 4. Waveforms of inductor current, gate current, and gate-source voltage.

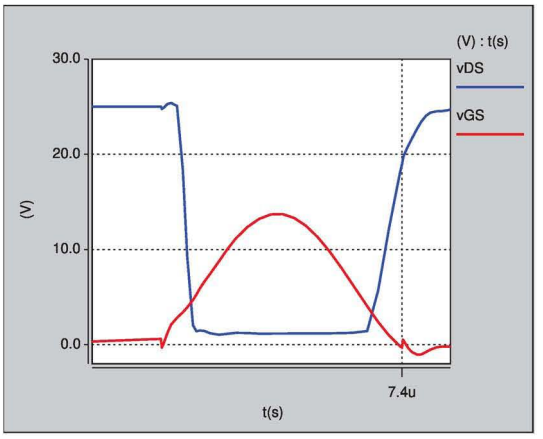

Fig. 5. Gate-source and drain-source voltages of driven power MOSFET.

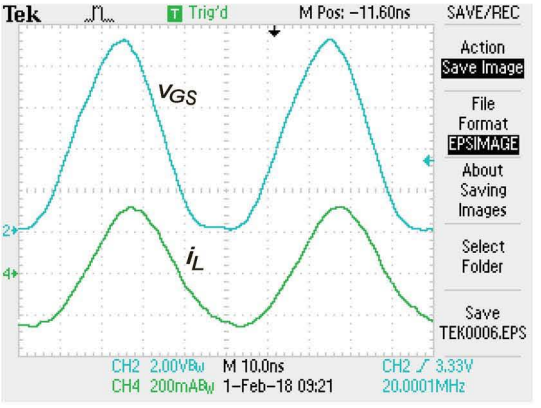

Fig. 6. The v_{GS} and i_L waveforms of proposed gate driver.

is driven by the proposed gate driver, enabling the duty cycle to be adjusted with fixed frequency. In addition, same power MOSFET is used as switch M in the gate-driver circuit. The dc supply was applied through the inductor L. All components of the gate driver were measured, using an HP4194A Impedance Analyzer. Fig. 6 shows the experimentally obtained waveforms of the gate-source voltage and the inductor current. They were measured at supply voltage $V_I = 4$ V, supply current $I_I = 0.02$ A, and the input power $P_I = 80$ mW. The duty cycle is variable between $D = 0.2$ to 0.8, and the operating frequency $f_s = 20$ MHz. The maximum value of gate-source voltage V_{GSmax} was 10 V at $D = 0.5$

IV. Conclusion

A new sinusoidal gate driver has been introduced. It has a low component count. It is useful as a low-side gate-drive circuit at high operating frequencies due to small energy storage passive components and low complexity. The transient response was fast as compared to conventional gate drivers. The circuit was designed, built, and tested. A good agreement between theoretically produced and the measurements was observed. This technique is suitable for telecom and RF applications that operate in the switching-mode from a few MHz to tens of MHz.

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