DIGITAL COMMUNICATION RECEIVER WITH INTEGRATED MAP SYNCHRONISATION AND ML DEMODULATION

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A new digital implementation of a receiver for digital communications is proposed. The key feature of the receiver structure is the close integration of the MAP carrier and clock synchronisation with the ML demodulation. It is shown that the same hardware is able to perform both operations, thus substantially reducing the receiver implementation complexity.

Introduction: This letter presents the use of digital signal processing for the implementation of a coherent demodulator which integrates the carrier and clock recovery, suitable for digital communications, as, for example, in regenerative satellites. A maximum *a posteriori* probability (MAP) method is employed to jointly estimate the carrier and clock phase of the received signal. The coherent demodulation is carried out by using the maximum likelihood (ML) estimation method, which usually requires a typical correlator circuit and a trellis decoder.[1] Our approach will show that, by a suitable choice of the architecture of the digital coherent receiver, the ML demodulator can be integrated in the joint carrier and clock recovery circuit with no increase in the overall system complexity. This scheme can be adapted to different digital modulation techniques suitable for digital communications, such as QPSK, O-QPSK and MSK. We focus here, as an example, only on the application for MSK signals, considering the interest of this modulation scheme in satellite communications.

Integrated MAP synchronisation and ML demodulation: The transmitted signal of the MSK type can be written as[2]

$$s(t) = \sum_n d_{I,n}(t)\sqrt{\left(\frac{2E}{T}\right)}\cos\frac{\pi t}{2T}\cos 2\pi f_c t + \sum_n d_{Q,n}(t)\sqrt{\left(\frac{2E}{T}\right)}\sin\frac{\pi t}{2T}\sin 2\pi f_c t \qquad (1)$$

where $d_{I,n}(t)$ and $d_{Q,n}(t)$ are the data sequences for the in-phase and quadrature channels, respectively. They are related to the input bit data sequence and are equal to ± 1 with the same probability. The terms $\cos \pi t/2T$ and $\sin \pi t/2T$ represent sinusoidal weighting factors, $1/T = R$ being the signal bit rate, f_c the carrier frequency and E the energy per bit. Now let us assume that the received signal $r(t)$ consists of $s(t)$ plus band-limited white Gaussian noise $n(t)$. The noise spectrum is considered to be flat and equal to $N_0/2$ W/Hz in the signal bandwidth $f_c - B$ to $f_c + B$, where we assume $B < f_c$.

The signal $r(t)$, supplied at the input of the digital receiver, is sampled according to the Shannon sampling theorem at the rate $1/t_s = f_s$. The system, which jointly estimates the carrier phase θ and clock phase ψ, processes a block of samples $\bar{r}$ of prefixed length. A MAP method[1] is employed to simultaneously estimate θ and ψ. It is well known that the MAP estimate of θ and ψ consists of choosing $\hat{\theta}$ and $\hat{\psi}$ such that the *a posteriori* probability density function of θ and ψ, i.e. $f(\theta, \psi/\bar{r})$, given the vector $\bar{r}$, is maximised. If the joint probability density function (PDF) $f(\theta, \psi)$ is uniform and the received signal PDF $f(\bar{r})$ is independent of θ and ψ, from the Bayes theorem, the MAP estimation procedure becomes: choose $\hat{\theta}$ and $\hat{\psi}$ such that $f(\bar{r}/\hat{\theta}, \hat{\psi})$ is maximum.

A necessary but not sufficient condition that must be satisfied by $\hat{\theta}$ and $\hat{\psi}$ in order to be MAP estimates of θ and ψ is given in Reference 3 with reference to an analogue implementation. The corresponding digital version of the MAP carrier and clock estimator is

$$\left.\frac{\partial \ln f(\bar{r}/\theta, \psi)}{\partial \psi}\right|_{\theta=\hat{\theta},\, \psi=\hat{\psi}} = -\sum_{i=1}^{L+1} \tanh\left\{\frac{2t_s}{N_0}\sqrt{\left(\frac{2E}{T}\right)}\sum_{l=1}^{2N} r(t) \times \cos(\pi t/2T + \hat{\psi})\cos(2\pi f_c t + \hat{\theta})\Big|_{t=(2i-1)T+lt_s-2\hat{\psi}T/\pi} \right.$$
$$\times \sum_{l=1}^{2N} r(t)\cos(\pi t/2T + \hat{\psi}) \times \sin(2\pi f_c + \hat{\theta})t_s\Big|_{t=(2i-1)T+lt_s-2\hat{\psi}T/\pi}$$
$$\left. + \sum_{i=0}^{L+1} \tanh\left\{\frac{2t_s}{N_0}\sqrt{\left(\frac{2E}{T}\right)}\sum_{l=1}^{2N} r(t)\sin(\pi t/T + \hat{\psi}) \times \cos(2\pi f_c t + \hat{\theta})\Big|_{t=2iT+lt_s-2\hat{\psi}T/\pi}\right\} \right.$$
$$\times \sum_{l=1}^{2N} r(t)\sin(\pi t/2T + \hat{\psi}) \times \cos(2\pi f_c t + \hat{\theta})t_s\Big|_{t=2iT+lt_s-2\hat{\psi}T/\pi} = 0 \qquad (2a)$$

$$\left.\frac{\partial \ln f(\bar{r}/\theta, \psi)}{\partial \theta}\right|_{\theta=\hat{\theta},\, \psi=\hat{\psi}} = -\sum_{i=1}^{L+1} \tanh\left\{\frac{2t_s}{N_0}\sqrt{\left(\frac{2E}{T}\right)}\sum_{l=1}^{2N} r(t) \times \cos(\pi t/2T + \hat{\psi})\cos(2\pi f_c t + \hat{\theta})\Big|_{t=(2i-1)T+lt_s-2\hat{\psi}T/\pi}\right\}$$
$$\times \sum_{l=1}^{2N} r(t)\sin(\pi t/2T + \hat{\psi}) \times \cos(2\pi f_c t + \hat{\theta})t_s\Big|_{t=(2i-1)T+lt_s-2\hat{\psi}T/\pi}$$
$$+ \sum_{i=0}^{L+1} \tanh\left\{\frac{2t_s}{N_0}\sqrt{\left(\frac{2E}{T}\right)}\sum_{l=1}^{2N} r(t)\sin(\pi t/2T + \hat{\psi}) \times \sin(2\pi f_c t + \hat{\theta})\Big|_{t=2iT+lt_s-2\hat{\psi}T/\pi}\right\}$$
$$\times \sum_{l=1}^{2N} r(t)\cos(\pi t/2T) + \hat{\psi}) \times \sin(2\pi f_c t + \hat{\theta})t_s\Big|_{t=2iT+lt_s-2\hat{\psi}T/\pi} = 0 \qquad (2b)$$

where $2(L+2)$ is the number of intervals (each T long) required to estimate θ and ψ, and N is the number of samples per bit. These equations suggest a digital closed-loop structure for the joint estimate of θ and ψ. By considering eqns. 2*a* and *b* as error signals, the MAP estimate of θ at the instant $(k+1)T$, i.e. $\hat{\theta}_{k+1}$, and the MAP estimate of ψ at the instant $(k+1)T$, i.e. $\hat{\psi}_{k+1}$, can be evaluated according to

$$\hat{\theta}_{k+1} = \hat{\theta}_k + K_\theta \left.\frac{\partial f(\bar{r}/\theta, \psi)}{\partial \theta}\right|_{\theta=\hat{\theta}_k,\, \psi=\hat{\psi}_k}$$
$$\hat{\psi}_{k+1} = \hat{\psi}_k + K_\psi \left.\frac{\partial f(\bar{r}/\theta, \psi)}{\partial \psi}\right|_{\theta=\hat{\theta}_k,\, \psi=\hat{\psi}_k} \qquad (3)$$

where K_θ is the carrier phase loop gain and K_ψ is the clock phase loop gain. These parameters must be determined in order to guarantee both system stability and good tracking performance. The configuration of the digital system which jointly estimates θ and ψ is indicated in Fig. 1.

The carrier and clock recovery circuit previously described can be affected by a 180° ambiguity for $\hat{\theta}$; to avoid an unacceptable bit error rate, a suitable differential encoding should be introduced in the modulation scheme. Indeed, the differential encoding is inherent in the MSK signal. Moreover, a better performance is achieved by employing an ML detection method with respect to classical quadrature demodulation followed by differential decoding.[2] In an ML demodulator the correlations between the received waveform and each of the possible signals represent the metrics to be evaluated. Over an

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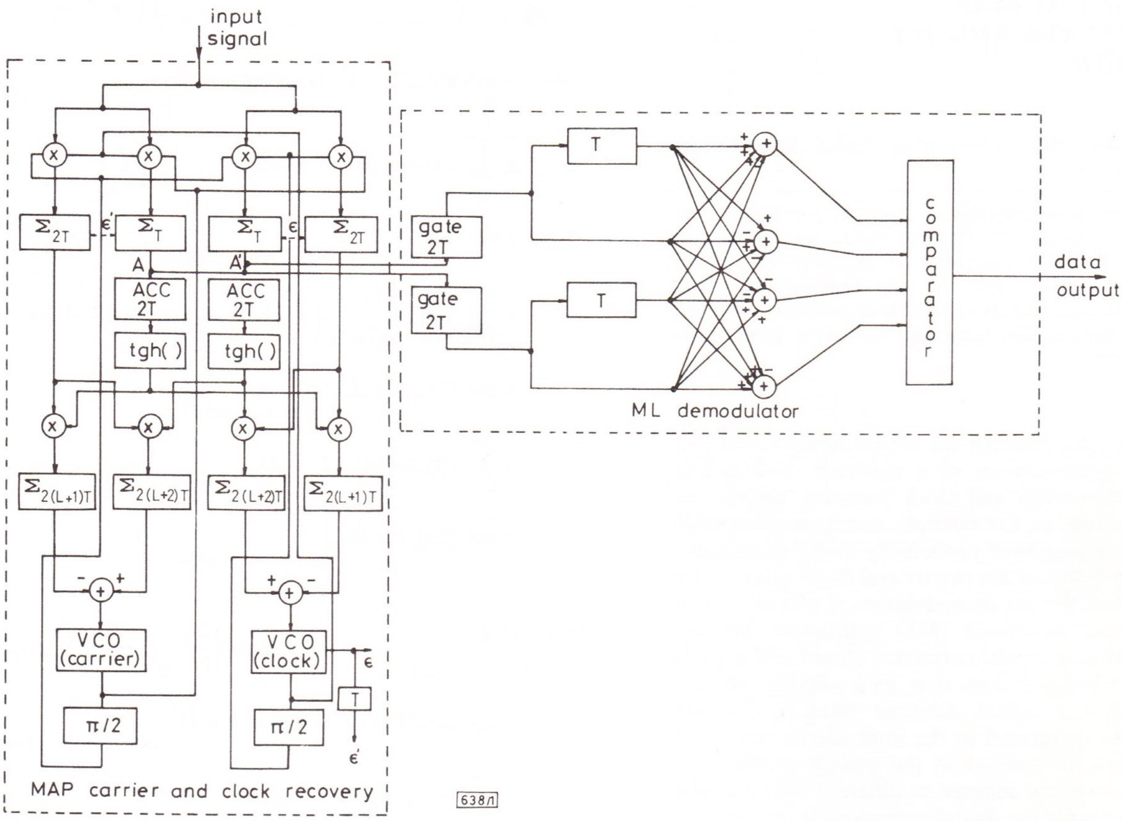

Fig. 1 *Block diagram of a digital communication receiver with integrated MAP synchronisation and ML demodulation*

appropriate number of bit intervals these metrics are accumulated, and used to detect the first transmitted bit, i.e. the first bit of the sequence corresponding to the largest metric. In the case of MSK signals, the optimum observation interval is equal to 2 bits.[2] In the digital receiver implementation, the ML detection circuit can be easily integrated with the joint MAP carrier and clock recovery circuit as shown in Fig. 1. The product of $r(t)$ by the two possible signals $\cos 2\pi(f_c \pm (\pi/2T))$ is obtained at the points A and A′ of Fig. 1, exploiting well known trigonometric identities.

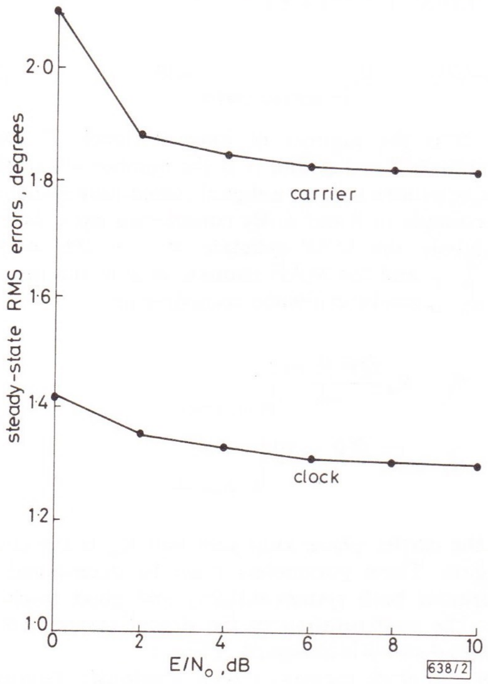

Fig. 2 *Steady-state RMS errors of carrier and clock estimated phases against E/N_0*

The overall number of multiplications and additions for the coherent demodulation of MSK signals is given by

$$M = 2(4N + 1)(2L + 3) + 4N \quad \text{multiplies/bit}$$
$$S = 2(2N + 1)(2L + 3) + 2(N + 1) \quad \text{adds/bit} \qquad (4)$$

In Fig. 2 the steady-state RMS errors of the carrier and clock estimated phases are shown against the parameter E/N_0. The results show that the MAP carrier and clock recovery circuit achieves a very good synchronisation performance that guarantees negligible (less than 0·1 dB) degradation on the obtainable bit error rate.

Finally, it can be stressed that the structure of the integrated MAP synchronising circuit and ML demodulator is highly suitable for a custom or semicustom LSI implementation.

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