UNIVERSITÀ
DEGLI STUDI
FIRENZE

UNIVERSITÀ DEGLI STUDI DI FIRENZE
DIPARTIMENTO DI INGEGNERIA DELL'INFORMAZIONE

CORSO DI DOTTORATO IN INGEGNERIA DELL'INFORMAZIONE
CURRICULUM: ELETTRONICA ED ELETTROMAGNETISMO
SSD ING-INF/01

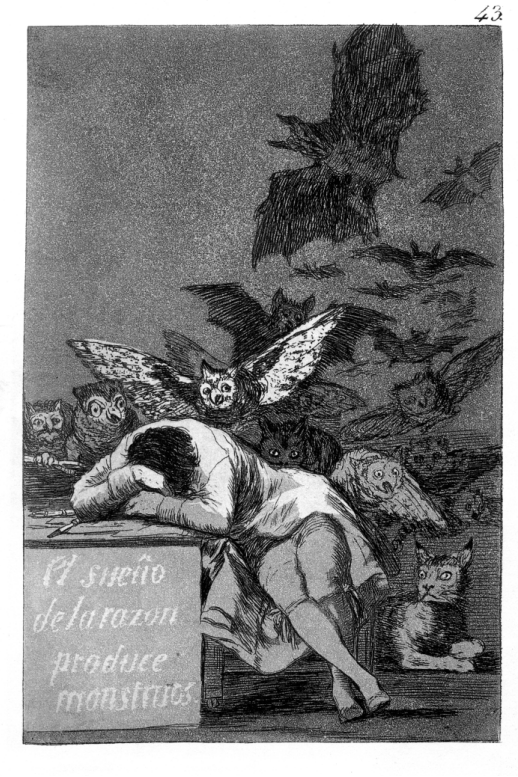
A TESTBENCH SYSTEM FOR STRUCTURAL HEALTH MONITORING WITH GUIDED-WAVE ULTRASOUND

Candidato
Pietro Giannelli

Tutori
Prof. Lorenzo Capineri
Ing. Giacomo Calabrese

Coordinatore
Prof. Luigi Chisci

CICLO XXX, 2014–2017



Francisco de Goya (1746-1828)
Capricho N°43: El sueño de la razón produce monstruos
(ca. 1796-1798)

Pietro Giannelli: *A Testbench System for Structural Health Monitoring with Guided-Wave Ultrasound,* © October 2017.

Thesis submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Information Engineering.

to those who care

PREFACE

It was fall 2013 when I joined the Ultrasound and Non-Destructive Testing Laboratory at the University of Florence—or perhaps I should say returned. At that time, a joint project with Thales Alenia Space Italia was about to enter its final stage.

The aim of that project was to develop a system for monitoring the structural health of aerospace-grade composite pressure vessels.

Starting from 2010 onwards, the research team in Florence had shaped a set of tools (devices and techniques) to fulfill the two major requirements: detection and localization of impacts between foreign objects and the vessel surface, and damage assessment of the composite material through guided-wave ultrasound inspection.

The electronics, however, were still lacking a definitive structure—an architecture.

During the following months, it became clear that the architectural challenge posed by a multi-channel ultrasound system that had to interact with several sensors attached to a voluminous object was a mere afterthought of the project: all the prototype electronics were ultimately shoved into a box, and cables were run between that box and the pressure vessel.

The shortcomings of a monolithic instrument became evident during the experimental phase: a bulky box with stiff cables was a heavy price to pay for monitoring less than a tenth of a square meter of carbon-fiber composite.

A question came naturally: would it be possible to perform structural health monitoring without all that bulky hardware? The answer was sensor networks.

The idea seemed extremely complex to realize right from the start, as the electronics developed for the prototype system highlighted the diversity of components needed for each sensor, and the amount of integration envisaged for the electronics was staggering. Indeed, in

order to be truly applicable to different structures, each sensor node needed to be nothing less than a mixed-signal system-on-chip.

Despite those bleak predictions, the possibility of performing structural health monitoring without needing bulky instrumentation and complex harnessing was simply too intriguing to be discarded.

And thus was born project Pandora, which would constitute the core of my Ph.D. activity for the following years. Texas Instruments seemed interested in the idea and decided to fund and back the research effort.

I am really grateful for the support and encouragement received during the course of my work, from the people in Florence, Milan, and Freising. Although I will not be making a list of names, I am sure they know who they are.

I also feel like I need to make an apology to my parents and relatives, that despite my poor disposition were always there when I needed them the most.

My biggest, lingering regret is not having been able to do more. With hindsight, the project was simply too vast for a single person to swiftly push forward, and many times it felt like I was cutting corners to move ahead.

I dearly hope that the work I have done has been sufficient to lay down sturdy foundations for the future of project Pandora.

Pietro Giannelli
January 18, 2018

INTRODUCTION

Structural health monitoring, a discipline subset of non-destructive testing and evaluation, deals with the assessment of the integrity of objects and components throughout their operative life, with the intent of increasing their safety and reliability, at the same time cutting maintenance costs.

The overarching aim behind the work presented in this dissertation is the development of wired sensor networks that can be deployed on structures to perform health monitoring with minimum encumbrance. This vision recognizes that the time is ripe to start working on bringing structural health monitoring to the mass market with stand-alone products: devices to keep under control the structural integrity of critical components in many different application fields.

This dissertation presents the design of a modular electronic instrument with the specific goal of creating a *testbench system*. Such device will ease the investigation of structural health monitoring techniques, at the same time allowing the improvement of the hardware and software needed to implement them, a task made possible by its modularity. This testbench system represents a first step towards the development of the envisaged sensor network architecture.

The foundations of the work hereby presented lie in a long string of research activities carried out in the past years at the Ultrasound and Non-Destructive Testing (USCND) laboratory of the University of Florence (Firenze, Italy), leading up to the design of a prototype health monitoring apparatus for space-grade composite pressure vessels commissioned by Thales Alenia Space Italia (Torino, Italy).

The experience maturated from said project suggested that a new, more versatile and scalable hardware was needed to ease future research efforts, including the possibility of fulfilling the vision of sensor networks for structural health monitoring.

A new project was thus started with the name *Pandora*, funded primarily by Texas Instruments inc. (Dallas, TX, United States), under which the current structural health monitoring research of the laboratory converged.

STRUCTURE OF THE DISSERTATION

This dissertation is divided in three parts. Given the heterogeneity of the arguments covered in the various chapters, appropriate context and bibliographical references on specific topics will be given in the relevant sections.

The first part introduces the topic of structural health monitoring, and frames the inspection techniques, target structures, and transducers that defined the context around which all the work revolved.

The second and third parts are specific to the testbench system electronics. Chapter 3 briefly describes the prototype SHM system previously developed for Thales Alenia Space Italia. The remaining chapters center on the architectural and hardware development done under project Pandora.

Since the work presented in this dissertation does not cover the entire design of the Pandora testbench system, which has not been finished yet, the components that have reached a sufficient state of completion are treated in Part II, while Part III describes those that were planned.

ORIGINAL CONTRIBUTIONS

Within the context of designing the new testbench system, an effort was done to improve several key aspects of structural health monitoring with guided-wave ultrasound, and thus provide the Pandora architecture with *state-of-the-art* tools to accomplish its purpose.

The work especially focused on the following arguments:

- *Ultrasonic guided-wave transducers*
  In Section 2.4, a multi-functional transducer for guided-wave ultrasound is presented. The new design expands the functio-

nality of previous interdigital transducers by adding a circular sensing element, and a resistive temperature device.

- *Ultrasonic transducer driver*
  A multichannel, multilevel class-D arbitrary waveform generator for the 100 kHz–1 MHz bandwidth was designed and built (Section 4.3.1), along with the relative pulse-width modulation scheme (Section 4.3.2), and the FPGA core required to operate the hardware (Section 4.3.3).

- *Receiver front-end electronics*
  Section 4.4 covers the development of an analog front-end with swappable voltage-mode and charge-mode amplifiers. An improved, fully-differential charge amplifier topology is presented in Section 4.4.4.

While some of these achievements represent ameliorations of existing technologies—like the work done on multi-functional transducers and the analog front-end—the ultrasound signal generation technique based on a multilevel class-D architecture was devised from the ground up, exploring an approach different from what is generally done in the literature with multilevel pulsers.

PUBLICATIONS

Some topics, figures, and results presented in this thesis have previously appeared in the following publications:

P. Giannelli, A. Bulletti, and L. Capineri, "Multifunctional piezopolymer film transducer for structural health monitoring applications," *IEEE Sensors Journal*, vol. 17, no. 14, pp. 4583–4586, 2017, ISSN: 1530-437X. DOI: 10.1109/JSEN.2017.2710425.

P. Giannelli, A. Bulletti, and L. Capineri, "Charge-mode interfacing of piezoelectric interdigital lamb wave transducers," *Electronics Letters*, vol. 52, no. 11, pp. 894–896, 2016. DOI: 10.1049/el.2016.0804.

A. Bulletti, P. Giannelli, M. Calzolai, and L. Capineri, "An integrated acousto/ultrasonic structural health monitoring system for composite pressure vessels," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 63, no. 6, pp. 864–873, 2016, ISSN: 0885-3010. DOI: 10.1109/TUFFC.2016.2545716.

L. Capineri, A. Bulletti, M. Calzolai, P. Giannelli, and D. Francesconi, "Arrays of conformable ultrasonic lamb wave transducers for structural health monitoring with real-time electronics," *Procedia Engineering*, vol. 87, pp. 1266–1269, 2014. DOI: 10.1016/j.proeng.2014.11.416.

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ACRONYMS

AAF Anti-Aliasing Filter

AC Alternating Current

ADC Analog-to-Digital Converter

AE Acoustic Emission

AFE Analog Front-End

ANSI American National Standards Institute

ASIC Application-Specific Integrated Circuit

AWG Arbitrary Waveform Generation

BJT Bipolar Junction Transistor

CFRP Carbon Fiber Reinforced Polymer

CMOS Complementary Metal-Oxide-Semiconductor

CMRR Common-Mode Rejection Ratio

CMUT Capacitive Micromachined Ultrasonic Transducers

COPV Composite-Overwrapped Pressure Vessel

CPV Composite Pressure Vessel

CW Continuous-Wave

DAC Digital-to-Analog Converter

DAQ Data Acquisition

DC Direct Current

DVGA Digital VGA

EIM Electrical Impedance Matching

EMAT Electromagnetic Acoustic Transducer

EMI Electromagnetic Interference

ENOB Effective Number of Bits

ESD Electrostatic Discharge

FDA Fully-Differential Amplifier

FET Field-Effect Transistor

FFT Fast Fourier Transform

FMC FPGA Mezzanine Card

FPGA Field-Programmable Gate Array

GF Gage Factor

GPIO General-Purpose Input-Output

HI-Z High-Impedance

HPS Hard Processor System

HV High-Voltage

I²C Inter-Integrated Circuit

IDT Interdigital Transducer

IEEE Institute of Electrical and Electronics Engineers

L-C Inductor-Capacitor

LDR Linear Dynamic Range

LNA Low-Noise Amplifier

LSB Least Significant Bit

LVCMOS-** Low-Voltage CMOS (voltage level standard)

LVDS Low-Voltage Differential Signaling

LWIR Long-Wavelength Infrared

MFC Macro-Fiber Composite

MM Memory-Mapped

MODEM Modulator-Demodulator

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor

NASA National Aeronautics and Space Administration

NDT, NDE Non-Destructive Testing / Evaluation

NMOS N-Channel MOSFET

NSD Noise Spectral Density

PCB Printed Circuit Board

PLL Phase-Locked Loop

PMOS P-Channel MOSFET

POL Point-of-Load

PSU Power Supply Unit

PV Pressure Vessel

PVDF Polyvinylidene fluoride

P(VDF-TRFE) P(VDF-tetrafluoroethylene)

PWAS Piezoelectric Wafer Active Sensor

PWE Pulse-Width Encoding

PWM Pulse-Width Modulation

PZT Lead zirconate titanate

Q Quality Factor

RCL Resistance Capacitance Inductance

RMS Root Mean Square

RTD Resistive Temperature Device

RTOS Real-Time Operating System

SHM Structural Health Monitoring

SINAD Signal-to-Noise and Distortion Ratio

SNR Signal-to-Noise Ratio

SOC System-on-Chip

SPI Serial Peripheral Interface

STEPS2 Sistemi e Tecnologie per l'Esplorazione Spaziale

TC Curie Temperature

THD+C Total Harmonic Distortion Plus Carrier

T/R Transmit/Receive

UART Universal Asynchronous Receiver-Transmitter

USB Universal Serial Bus

USCND Ultrasound and Non-Destructive Testing Laboratory

VGA Variable-Gain Amplifier

VITA VMEbus International Trade Association

Part I

STRUCTURAL HEALTH MONITORING WITH GUIDED-WAVE ULTRASOUND

1 MONITORING STRUCTURES

Structural health monitoring (SHM) is an umbrella term that groups together the methods adopted to evaluate the health (as in structural integrity and degradation) of some object in a continual fashion, without having to dismantle it (*in-situ*) [1]. These kinds of techniques are generally advantageous to plan the maintenance of systems that are difficult (or even impossible) to access, or generally expensive to take off-line for inspection.

Structural health monitoring is a field of study that intersects many areas of science and engineering, both from the application and implementation points of view. As a natural offspring of non-destructive testing and evaluation (NDT & E), SHM has made its way into many diverse applications, from civil infrastructure to rotating machinery, from nuclear reactors to spacecrafts, with a vast range of techniques, from fiber optics to ultrasound, from thermal imaging to impedance metering.

The multidisciplinarity of SHM is so vast that people coming from the most disparate backgrounds can give, and have given important contributions to the advancement of the subject. While people with a background in physics and mechanical engineering may be more inclined to study the core topics of structural failures, and how to detect them, there still remains a large amount of work related to the instrumentation and systems that make SHM possible, which falls into the domain of electronics and computer science.

1.1 STRUCTURAL HEALTH MONITORING TASKS

The main objectives that should be fulfilled by structural health monitoring can be summarized in a short list of macro-tasks:

1. Detection.

2. Localization.
3. Identification (diagnosis).
4. Prediction (prognosis).

The ordering of the above list is important, as each one of those tasks builds on top of the information provided by the previous, resulting in a rapid grow of complexity as additional functionality is built into a SHM system. A brief description of the tasks is provided in the following paragraphs.

DETECTION The first and foremost objective of SHM is to detect whether the integrity of the target structure is being compromised in any way, which can be done following two complementary approaches:

- *Passive-mode* is the detection of structural responses to various kinds of uncontrolled stimuli, performed through continuous *listening* for certain signals coming from the structure. For instance, the detection of impacts between the target structure and external objects is a form of passive-mode SHM.
- *Active-mode*, on the other hand, requires the direct stimulation of the target structure with the intent of identifying structural changes, which may be indicators of health degradation. In guided-wave SHM, active-mode is generally performed with a pitch-catch setup: an ultrasound signal is transmitted through the structure, received, and subsequently analyzed.

LOCALIZATION Precisely identifying the position where the structure has been compromised logically follows from the previous task. Localization can indeed be performed on both passive and active-mode data, obtaining two very different pieces of information: in passive-mode, the position of a detected *event* is determined, while in active-mode the position of a detected *structural change* is returned.

IDENTIFICATION AND PREDICTION The information provided by the detection and localization tasks can be merged and further processed to reach certain conclusions on the nature of the structural change that has occurred.

After the damage experienced by the structure has been precisely identified (if it was a damage at all), the expected lifetime and reliability of the structure can be evaluated with this new data, obtaining prognostic information.

Ideally, a *complete* SHM system should strive to cover all the points listed above.

The early design stages of a SHM system for research purposes are, however, much limited in scope, as the designer cannot really predict what the final requirements for identification and prediction will amount to. A testbench system should thus provide the enabling tools to perform an unhindered research activity, even by resorting to an over-designed hardware.

1.2 ULTRASONIC GUIDED-WAVE INSPECTION

One of the techniques with which SHM can be performed is the so-called *ultrasonic guided-wave inspection*, that involves the adoption of mechanical waves propagating along a structure, guided by its boundaries. Various types of guided waves exist, arising from the variegated composition of bulk waves traveling within structures of appropriate geometry, along with many different methods to artificially generate, and sense them.

In general, the advantage of using guided-waves arises from their ability to travel along objects, even for long distances, following their geometry without the need of a scanning action, and reaching places that may be otherwise unaccessible [2].

Guided-wave SHM has received considerable interest from the scientific community, such that the production in the field has reached an impressive volume, prompting the publication of several review papers over the years [3–5].

The contents of this dissertation are centered on a very specific branch of guided-wave SHM that uses Lamb waves to inspect plate-like structures.

Lamb waves get their name from Horace Lamb, an English applied mathematician who formulated and published their description a hundred years ago [6]. The propagation of these particular flavor of guided-waves is supported by plates of elastic material, that is, within homogeneous, thin solid objects having two well-defined parallel planar boundaries. During the years, the original theory has been generalized to encompass various kinds of plate-like structures, including curved shells, thin-wall pipes, multi-layered laminate structures, and so on.

The two characteristic equations of Lamb waves are reported in Equation 1.1 (symmetric modes), and Equation 1.2 (antisymmetric modes).

$$\frac{\tan(ph)}{\tan(qh)} = -\frac{4\kappa^2 pq}{(q^2-\kappa^2)^2} \tag{1.1}$$

$$\frac{\tan(ph)}{\tan(qh)} = -\frac{(q^2-\kappa^2)^2}{4\kappa^2 pq} \tag{1.2}$$

Where the waveguide boundary is defined by its thickness t ($h = t/2$), $\kappa = \omega/c_p$ is the wavenumber, ω is the angular frequency, c_p is the phase velocity of the Lamb wave mode, $p^2 = \omega^2/c_l^2 - \kappa^2$ and $q^2 = \omega^2/c_t^2 - \kappa^2$. c_l and c_t represent the longitudinal and transverse (shear) wave velocity in the guiding medium.

The characteristic equations 1.1 and 1.2 describe two sets of guided modes that are intrinsically dispersive, and can be numerically solved for c_p to obtain a dispersion curve plot.

As an example, the Lamb wave dispersion curves of an uniform aluminum plate were calculated using the LAMB toolbox[1] [7]. The real solutions, plotted in the wavenumber domain in Figure 1.1, show the existence of several symmetric and antisymmetric modes. It can

1 The LAMB toolbox is available at https://www.mathworks.com/matlabcentral/fileexchange/28367-the-lamb-toolbox.

be observed that a cutoff wavenumber exists below which only the zeroth order modes propagate, with diverging phase velocities.

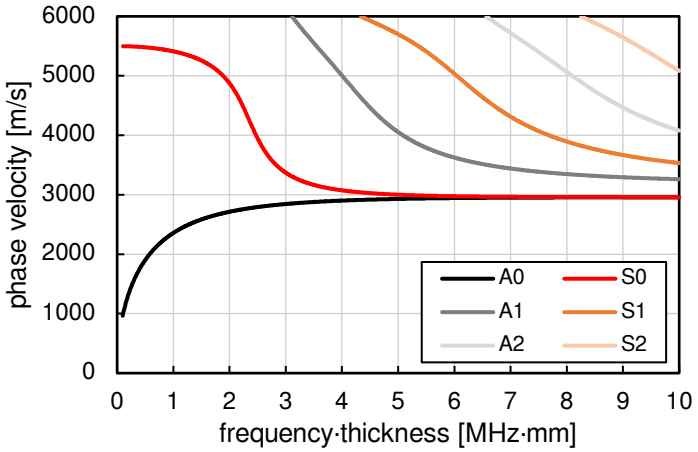


Figure 1.1: Lamb wave dispersion curves calculated for an homogeneous aluminum plate.

The S_0 and A_0 can be graphically represented with their longitudinal (along the wavevector) and normal (along the waveguide thickness) displacements as in Figure 1.2.

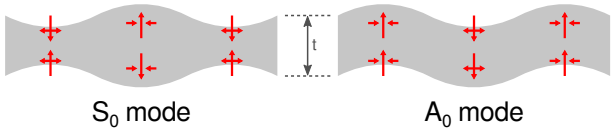


Figure 1.2: Displacement of the zeroth order Lamb wave modes.

1.3 CURRENT TRENDS IN GUIDED-WAVE SHM

Guided waves, and especially Lamb waves, represent an interesting way to perform structural health monitoring because their propagation is affected in a measurable fashion by the most common superficial and bulk defects encountered in plate-like structures [8–10].

The interaction of guided waves with material defects in composite laminates, such as delaminations [11–15] and debondings [16], has been studied extensively by the scientific community, with some works focusing specifically on damage resulting from impacts with foreign bodies [17, 18].

Guided waves can be used to perform both passive and active-mode monitoring, as long as the transducers and electronics allow duplexed operation. Monitoring is enacted by rigging the target structure with a certain amount of guided-wave transducers, either attached to the surface, or embedded, thus creating what is generally called a *smart structure*: a multi-channel electronic system is then needed to interface and operate all the transducers. Numerous SHM designs of this sort have been published [19–23].

On the algorithmic side, an interesting trend in guided-wave SHM is represented by the adoption of wavelet-based techniques, which allow the simultaneous analysis of non-stationary ultrasonic signals in both the time and frequency domains [24–26].

So far, several works exploiting wavelet analysis have been published on topics like active-mode damage detection [27–29], Lamb wave mode identification [30], impact localization [31], and pipe inspection [32].

1.4 TARGET STRUCTURES AND ENVIRONMENTS

Today, with the increasing adoption of composites as structural materials in many fields of engineering, the task of assessing the health of such components has become crucial to ensure the continued safety and reliability of the most advanced designs.

Pressure vessels (PVs) are one of the engineering structures that benefit most from the adoption of composites. Historically, pressure vessels have been entirely made of metal until the seventies, when NASA introduced the first composite pressure vessels (CPVs) for civilian use (as part of the firefighters breathing system program). CPVs were originally developed by NASA during the Apollo program [33].

Type I	All-metal vessel
Type II	Metal vessel with added fiber hoop wrapping
Type III	Metal liner with full composite overwrapping (liner is non-structural)
Type IV	High-density polymer liner with full composite overwrapping (liner is non-structural)
Type V	Liner-less, full composite construction

Table 1.1: Classification of pressure vessels.

The single most important advantage of using CPVs over regular, metal vessels is the considerable reduction of weight for the same operating pressure rating [34]. Weight reduction is essential to increase fuel efficiency (and reduce inertia) in automotive, transportation, and aerospace applications. Several CPV designs are possible, with increasing composite content: Table 1.1 lists the current classification of pressure vessel technologies.

Unfortunately, CPVs also present several drawbacks related to their complexity: designing them is difficult, construction is expensive, and failure modes are very different from metal vessels. Moreover, as CPVs made their way into the market as reusable components, concerns about their testing procedures and expected lifetime had to be addresses [35, 36].

Providing an adequate and cost-effective health monitoring technology for composite pressure vessels could potentially extend their useful life, cut maintenance costs, and greatly increase their safety. However, the problems associated with the development of such a technology are not only related to our current knowledge of composite materials, but also to the difficulties of performing monitoring tasks in potentially adverse environments.

Special qualification requirements already exist to ensure a safe and reliable operation of electronic systems and devices in the automotive and aerospace sectors. Complying with these regulations

is fundamental for the SHM system itself, but unfortunately insufficient to guarantee that it provides correct information at all times, as monitoring algorithms also need to be made resilient to changing environmental conditions [37–40].

1.5 PAST PROJECTS

The research work done at the Ultrasound and Non-Destructive Testing Laboratory in the field of structural health monitoring has been mostly oriented towards the identification of damage in carbon fiber reinforced polymers (CFRP) [41–43].

The activities led to the design of a proof-of-concept SHM system for spaceborne composite pressure vessels that performed impact detection and localization (passive-mode) and damage assessment (active-mode) with Lamb waves [44–47]. The system is described in Chapter 3.

2

LAMB WAVE TRANSDUCERS

There are a plethora of different ways to excite and receive Lamb waves on a plate-like waveguide [48, ch. 3]. One of the most common (even from a historical perspective) is the adoption of ultrasonic transducers with adjustable-angle wedge coupling [12, 49, 50], which can also be liquid [51]. Similarly bulky devices used in the field are Hertzian contact transducers [52].

Non-contact methods have also been extensively studied, including air coupling [7, 53–55], electromagnetic acoustic transducers (EMATs) [56–58], and laser-based techniques [55, 59, 60].

Capacitive micro-machined ultrasonic transducers (CMUTs) have also been recently applied to the generation and reception of Lamb waves [61], although their usage is currently restricted to the propagation in silicon substrates.

In the context of this work, the most interesting transducer technologies are represented by low-profile devices, such as interdigital transducers (IDTs), which will be treated in Section 2.3, piezoelectric wafer transducers [62, 63], and Lamb wave transducers made with macro-fiber composite materials (MFC) [64, 65].

Lamb wave transducers intended for permanent installation on composite pressure vessels need to abide some demanding operative conditions both related to the structure itself, and to the external environment. They also need to be unobtrusive, as space is generally a premium in the applications where CPVs are adopted (transportation, automotive, and aerospace), and possibly inexpensive.

From a SHM standpoint, one of the main problems associated with pressure vessels is their inflation / deflation cycles, which result in varying degrees of mechanical deformation of the structure to which the ultrasonic transducers are coupled. The ability to withstand such fatigue is indeed one of the requirements when choosing the transducer technology for this specific application.

Piezoelectric ceramics are widely adopted to make ultrasonic transducers but unfortunately they fall short in resisting to continuous stress and strain due to their brittleness. The intrinsic elasticity of polymer-based materials, on the other hand, is the main reason that led to the adoption of piezoelectric polymers in this work.

2.1 PVDF AND ITS COPOLYMERS

Polyvinylidene fluoride (PVDF) is an electroactive polymer that has been in use as piezoelectric material in the field of ultrasonics since the early 70's, after the initial discovery of its piezoelectric properties in 1969 [66]. PVDF and its copolymers have been the subject of extensive research through the years, summarized in a few review papers [67–70].

Bulk PVDF does not present piezoelectric properties, as it naturally exhibits a predominance of α-phase structure with randomly oriented dipole moments. A two-fold process involving mechanical stretching, to transition the crystalline structure to β-phase, and the application of a strong electric field, to align the dipole moments, is needed to obtain a strong piezoelectric behavior [71, 72].

It is useful to contextualize some of the properties of PVDF with reference to lead zirconate titanate (PZT), a widely adopted ferroelectric ceramic material. Such comparison can be found multiple times in the numerous papers cited throughout this section, but it can be boiled down to the parameters reported in Table 2.1.

Besides the lower dielectric constant, and the consequential higher impedance with respect to piezo-ceramics, one of the main drawbacks of poled PVDF is its very poor resistance to high temperatures.

Piezoelectric materials have a characteristic temperature at which all polarization is irreversibly lost: the Curie temperature (TC, a term borrowed from magnetism). In practice, however, the degradation in piezoelectric performance starts well before reaching TC, for material depolarization is a process accelerated by heat.

Pure PVDF has a TC of around 200°C (this is an extrapolated value, as it is above the melting point), but its piezoelectric constants start

		BI-AXIAL PVDF	PZT5A3
Dielectric constant	κ_{33}	13–22	1936
	κ_{31}	13–22	1616
Coupling coefficient	k_t	0.1–0.15	0.48
	k_p		0.62
Piezoelectric coefficient [pC/N]	d_{33}	13–22	485
	d_{32}	6–10	
	d_{31}	6–10	123
Maximum use temperature [°C]	T_{max}	90	175

Table 2.1: Comparison of the properties of a commercial poled PVDF film [73] against a commercial PZT ceramic [74].

to noticeably degrade at much lower temperature [75]. In fact, manufacturers suggest to never subject poled PVDF to temperatures above 75–90°C.

PVDF copolymers have been developed that present increased temperature stability. In particular, PVDF with added trifluoroethylene, or P(VDF-TrFE), can be used at temperatures up to 100°C, albeit its piezoelectric coefficients are not necessarily better that PVDF (performance is strongly dependent on the molar ratio and manufacturing process) [69, 76–78].

The development of P(VDF-TrFE) also addressed the problem of crystalline structure, as certain molar compositions present a significant prevalence of β-phase, and therefore do not require mechanical stretching during the manufacturing process [79–81].

In recent years, significant research effort has been directed toward the improvement of the piezoelectric performance of PVDF copolymers by merging them with other components. Works have been published about P(VDF-TrFE) composites made with graphene oxide [82], zinc oxide [83], lead zirconate titanate [84], and barium titanate [85] to name a few.

The applicability of piezoelectric polymers to SHM systems operating in challenging environments has been studied in a few publications [86, 87].

2.2 UNWANTED EXCITATION SOURCES

While PVDF films are used in structural health monitoring applications for their piezoelectric response, the material itself generates electrical signals also when exposed to other kinds of stimuli unrelated to ultrasonic guided waves. These unwanted signals can, in certain scenarios, degrade the signal-to-noise ratio of the system.

The main sources of noise captured by piezoelectric sensors originate from environmental vibrations conducted by the structure to which the sensor is coupled, its electrical cabling, or even the fluid in which the structure is immersed (e. g. air-coupled sound waves). The disruptive influence of vibrations on a guided-wave SHM system is strictly dependent on the application: civil, industrial, and vehicular structures are all prone to experience vibrations of different amplitude and spectral content.

A distinction, however, needs to be made between active and passive SHM (introduced in Section 1.1). In active mode, damage detection is performed with a defined inspection signal and timing, such that the system can be tailored to avoid the interference of known vibration sources. In passive mode, on the other hand, signals pertaining to the actual monitoring task may end up buried in irrelevant vibrations, making the detection process much more difficult, especially if the system is operating broadband.

Other potentially unwanted signal sources in PVDF sensors are of thermal origin, for the material also presents a strong pyroelectric response [71]. Due to this property, and its capability to absorb long-wavelength infrared radiation (LWIR) [88], PVDF has been extensively used in motion detectors, imaging [89, sec. 4.4], and laser beam characterization [90].

Fortunately, the pyroelectric response of a PVDF film is slow and relevant only at frequencies well below those of interest for guided-

wave ultrasound (see for instance the results published in [91–93], all obtained with PVDF films thinner than those adopted in this work). Moreover, sensor encapsulation and coupling add thermal mass to PVDF film transducers used in SHM, further increasing their thermal time constant.

2.3 INTERDIGITAL TRANSDUCERS

Interdigital transducers for guided Lamb wave applications are constituted by a sheet (or thin plate) of piezoelectric material equipped with electrodes on the surface: at least one side must host two sets of interleaved comb electrodes with separate connections, while the other may present either a ground plane, another pattern of electrodes, or nothing at all (although it is good practice to provide a reference plane).

The exploded view of a generic IDT is shown in Figure 2.1, where the geometrical parameters are also defined. The transducer has one side coupled to the guiding medium (a plate-like structure) or, in certain cases, can be embedded [42]. The adoption of a backing layer on top of the transducer is also an option.

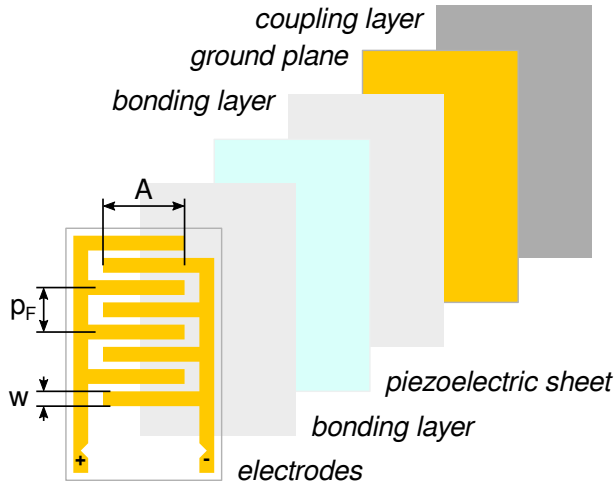


Figure 2.1: Exploded view of an interdigital transducer.

The two sets of comb electrodes are generally assumed to operate with 180°-out-of-phase signals (both in transmission and reception), such that the transducer provides a geometrical wavelength selectivity connected to the finger pitch.

Initial theoretical and practical developments of IDT transducers for Lamb waves were published in [94–97], where the basics of their operation are explained. In brief, IDTs are geometrically designed in the wavenumber domain to obtain a certain mode selectivity specific to the dispersion curves of the guiding medium to which they are going to be coupled. The finger pitch p_F determines the peak response at the wavelength $\lambda_{GW} = 1/p_F$, that in turn corresponds to a specific set of Lamb mode frequencies supported by the target structure.

The length A of the electrodes defines the in-plane collimation of the two Lamb wave beams emitted along the longitudinal axis of the IDT pattern. If the beam divergence angle γ is defined as the position of the first local minima of the main lobe, it was shown in [98] that Equation 2.1 well fits the divergence angle generated by a single finger of width A. In the same work, it was also shown that the number of finger does not influence the divergence angle, but only the amplitude of the lobes.

$$\gamma = \sin^{-1}\left(\frac{\lambda_{GW}}{A}\right) \tag{2.1}$$

The effect of finger width W can be studied by performing the spatial Fourier transform of the electrode pattern [96, 99]. In general, enlarging W boosts the response to the fundamental wavelength (i. e., at λ_{GW}), but its effects at shorter wavelengths need to be carefully analyzed if higher-order harmonics are of interest. Aside from the acoustical effects, finger width and length also determine the electrical capacitance of the transducer.

Piezopolymer film IDTs conjugate the broadband response of the piezoelectric material with the geometrical wavelength selectivity of the electrodes, meaning that the excitation signal can be adjusted to follow the optimal wavelength without having to worry about mechanical resonances of the piezoelectric material itself [100].

When the transducers are operated at a frequency·thickness lower than the cutoff of 1+ order Lamb modes, only two modes can propagate: the zeroth order antisymmetric (A_0) and symmetric (S_0). In this condition, it is generally easier to discriminate the wave packets belonging to the two modes, as their phase velocities can be largely different, and one of the two will be attenuated by the IDT geometry.

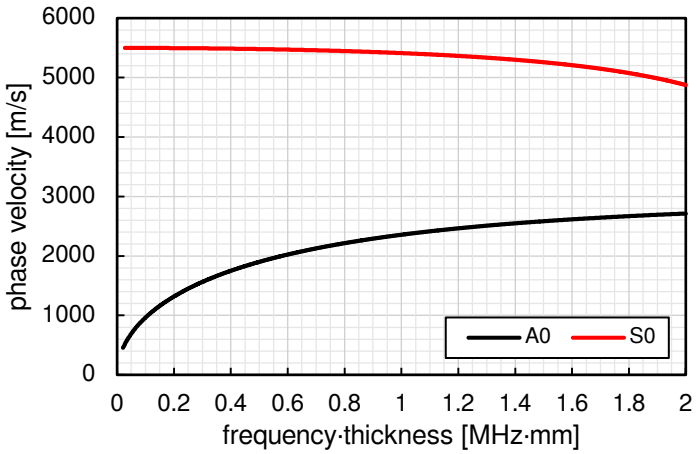


Figure 2.2: Low frequency dispersion curves calculated for an aluminum plate.

If the target waveguide is known beforehand, its Lamb wave dispersion curves can be computed and used to determine the finger pitch p_F required to boost the sensitivity to a specific mode at a certain frequency. This can be done graphically by taking the dispersion plot in the range of interest (e. g., the plot for aluminum plates shown in Figure 2.2), and drawing a line connecting the origin with the target frequency point on the mode dispersion curve: the slope of this line determines the optimal finger pitch.

Several aspects of IDTs have been studied and published that specifically apply to the field of guided-wave SHM. Analytical modeling of Lamb wave generation using (piezoceramic-based) IDTs was originally published in [101]. A theory of mode excitation with IDTs specific to composite laminate plates was developed in [102, 103], while

a numerical analysis approach was presented in [104]. Lamb wave generation with graded IDTs was studied in [105].

Though this dissertation focuses on IDTs made with piezopolymer films, transducers based on macro-fiber composite (MFC) materials have also been proposed [64, 106, 107], representing one of the most recent developments in the field.

IDTs developed at USCND present a significant difference from those published by other research teams, in that they are manufactured via laser etching, starting from metal-coated—usually with Pt-Au, or Cr-Au alloys—poled PVDF sheets [42, 99]. Since PVDF is mostly transparent to the laser beam, it does not heat up considerably during the etching process, and the laser passes through the polymer etching the back side metalization as well. Therefore, the process results in having an identical electrode pattern on both sides of the PVDF.

The piezoelectric polymer films used throughout the previous and current research activities were purchased form Piézotech S.A.S.[1] and Precision Acoustics Ltd.[2].

The improved IDT described in the following sections represents a direct continuation of a previous design [41, 43, 44], which was also successfully adopted in the SHM system described in Chapter 3 [47]. When used in active mode, those transducers were operated with burst signals within the 100 kHz–1 MHz range that, after being fine-tuned to the waveguide material, was found to provide a reasonable trade-off between Lamb wave resolution and attenuation. The 100 kHz–1 MHz bandwidth was carried over to the testbench system described later in this dissertation.

Since the thickness of the piezopolymer film is $t = 110\mu m$, and the longitudinal wave velocity in PVDF is $c_l \approx 2200 m/s$ the fundamental thickness-mode resonance frequency f_{tr} can be calculated as in [108]:

$$f_{tr} = \frac{c_l}{2t} \approx 10MHz \tag{2.2}$$

1 Piézotech S.A.S., F-68220 Hesingue, France; website: http://www.piezotech.eu.

2 Precision Acoustics Ltd., Dorset DT2 8QH, United Kingdom; website: https://www.acoustics.co.uk/.

Which is well above the specified operating frequency range.

2.4 A MULTIFUNCTIONAL DEVICE

The possibility to etch an arbitrary pattern on the metal coating of the piezopolymer film constituted an enabling technology for including different sensing elements on the same film.

Two additional sensory patterns have been etched alongside the IDT electrodes on the same PVDF film device: a 1/4″ circular element (another piezoelectric sensor), and a resistive temperature device (RTD). The picture of one transducer including all the three patterns is shown in Figure 2.3 alongside a dimensional drawing.

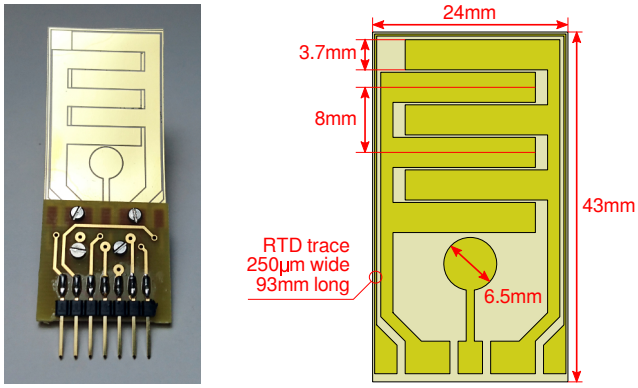


Figure 2.3: Multifunctional IDT: (a) picture; (b) dimensional drawing.

2.4.1 *The Interdigital Pattern*

The interdigital pattern etched on this transducer retained the previously used finger pitch p_F=8 mm and aperture, but the width was expanded to cover all the available inter-finger spacing to maximize both the transducer response to the fundamental wavelength, and its capacitance.

IDT CAPACITANCE The interdigital capacitance was measured on a free-hanging transducer (uncoupled to other structures) using a Keysight 4284A RCL meter, and the results are plotted in Figure 2.4. This measurement includes the contribution of all the fingers connected in parallel, as well as the stray capacitance belonging to the electrode access traces that connect the fingers together.

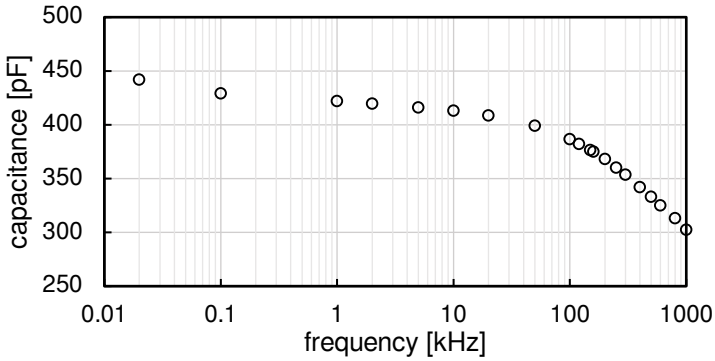


Figure 2.4: Measured capacitance of the interdigital pattern.

2.4.2 *The Circular Piezoelectric Element*

IDTs present some advantages for guided-wave inspection, like directionality and wavelength selectivity, that may be become deficiencies in certain scenarios.

When performing impact detection and localization, for instance, using non-selective sensors with axisymmetric geometry distributed over the structure allows collecting acoustic emission (AE) signals without affecting their information content [21, 109]. The assumption of sensor omni-directionality is generally taken for granted in acoustic source localization problems on plate-like structures, whether the source is an impact event, or the energy released during material alteration [110].

Some companies have specialized in providing patch piezoelectric sensors that can be used to perform acoustic source localization, like

Acellent and Physik Instrumente. Specifically, the diameter of Acellent's SML-SP-1/4-* PZT sensor (1/4", or 6.35 mm) was used as reference to draw the circular element of the design hereby presented.

The first experimental application of the circular element part of this multifunctional piezopolymer transducer was to perform impact localization on a carbon-fiber laminate sheet [111].

SENSOR CAPACITANCE The circular element capacitance was measured on a free-hanging transducer using a Keysight 4284A RCL meter, the results are plotted in Figure 2.5. Similarly to the IDT capacitance measured above, this result also includes the stray capacitance of the electrode access traces.

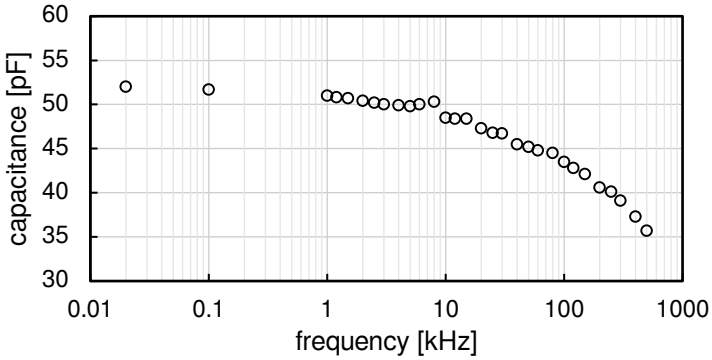


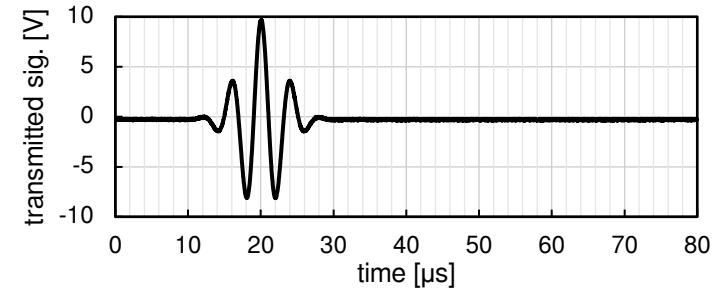
Figure 2.5: Measured capacitance of the circular piezoelectric element.

SENSITIVITY COMPARISON The performance of the circular piezoelectric element as a Lamb wave receiver were evaluated by comparing it to a PZT device of similar active area, the Physik Instrumente P-876.SP1.

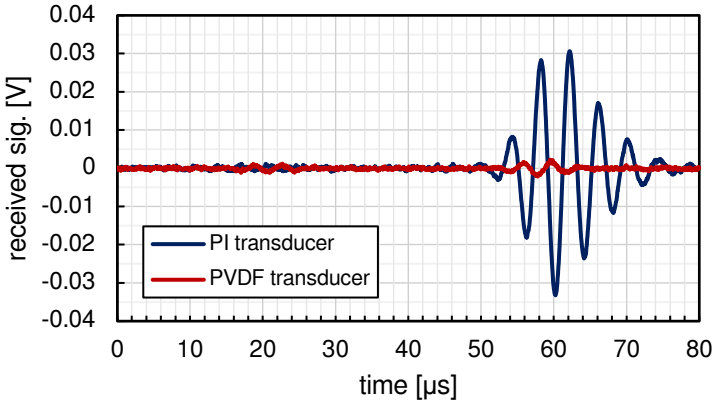
The two sensors were taped side-by-side to an aluminum plate 1.2 mm thick, with a third transducer used as transmitter and placed at a distance of 200 mm from both. A Morlet wavelet centered at 250 kHz was transmitted, and the response signal was received from both sensors using the same pre-amplifier (an instrumentation amplifier

with a gain of 78 dB @ 250 kHz). The acquired traces are plotted in Figure 2.6.

The plot shows that, as expected from the piezoelectric properties of the materials, the circular element sensitivity is much lower than that of the PZT device. Such a wide difference, however, may not be a problem in impact detection applications, where signals tend to be rather large.



(a)



(b)

Figure 2.6: Experimental sensitivity comparison of the circular element with a commercial PZT sensor of similar size: (a) transmitted Morlet (central frequency 250 kHz); (b) signals received from the two sensors.

2.4.3 *The Resistive Temperature Device*

The resistive temperature device (RTD) was included with the aim of providing local temperature sensing of the structure under test, which is a particularly important information when performing SHM with guided-waves [38–40, 112, 113].

A 250 µm-wide trace was etched on the Cr-Au coating, running along the perimeter of the piezoelectric film: with a length of 93 mm, the end-to-end resistance of the trace amounted to ~350 Ω at room temperature.

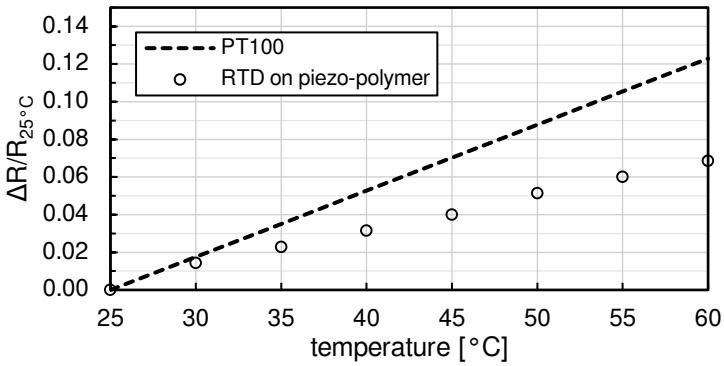


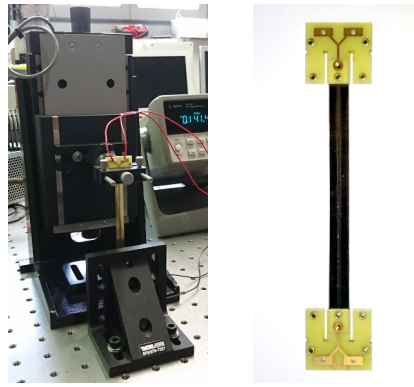
Figure 2.7: Relative resistance change over temperature of the RTD embedded into the multifunctional IDT.

Preliminary measurements in an industrial oven resulted in the temperature characteristic of Figure 2.7, shown together with the linearized curve of a PT100. These measurements were performed with the device left free-hanging, and did not account for thermal dilation of the PVDF substrate, which has a linear thermal expansion coefficient of about 130×10^{-6} K^{-1}.

Transducer straining is indeed a common expected occurrence in real-world applications, especially when they are installed on pressure vessels subjected to frequent inflation and deflation cycles.

Another experiment was then set up to evaluate the gage factor $GF = (\Delta R/R) / (\Delta L/L)$ of the metal coating when the PVDF was subjected to a controlled elongation at constant temperature.

Three strips of piezopolymer material with different geometry were cut and strained using the micro-positioner fixture shown in Figure 2.8: it was expected that they would all yield a similar GF.



(a) (b)

Figure 2.8: Gage factor measurement: (a) micro-positioner test fixture; (b) one of the PVDF sample strips.

The results of Figure 2.9, unfortunately, paint an unsatisfactory picture. With such a huge difference in gage factor between the three samples, the proposed RTD sensor is not a really promising solution. The poor strain performance are however understandable, as the deposition of uniform metal-coatings on piezoelectric PVDF films, having repeatable characteristics, is not really a primary concern of the manufacturers at this time (several metal coatings techniques have been analyzed in [114]).

As a side result of the GF measurements, it was observed that one of the PVDF samples became plastic at a relative strain smaller that the other two (the red trace of Figure 2.9, which stops at a relative strain lower that the others).

That sample was also the only one of the three that had been subjected to laser etching. So far there has been no further investigation on the matter, however this behavior indicates that laser etching affects the piezopolymer material, after all.

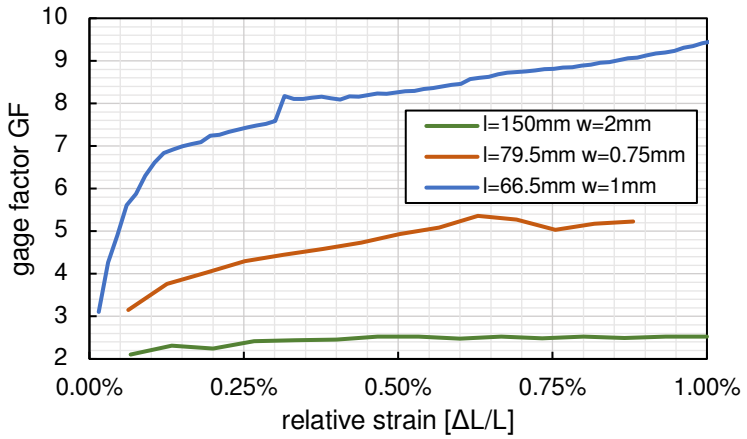


Figure 2.9: Measured gage factor of the metal coating on three PVDF sample strips. Dimensions of the samples are indicated in the legend.

2.5 MULTI-ELEMENT IDT

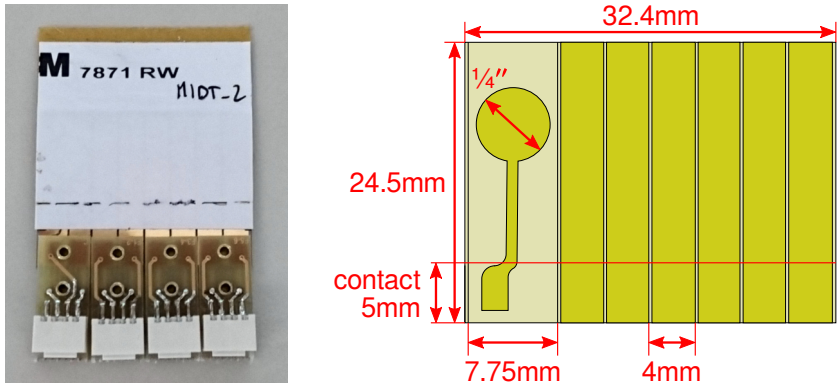
One of the limitations of interdigital transducers is that, once the geometry of the electrodes has been set during the manufacturing phase, their selectivity becomes tied to a specific wavelength. The corresponding peak frequency response is thus defined by the interception of the guiding medium dispersion curves with the IDT's own finger pitch.

While adapting the drive frequency of the transducer to match the wavelength is generally not a problem (as long as the transmission system supports broadband operation), this takes away a great deal of versatility from IDTs.

The problem of adjusting the wavelength selectivity of IDTs after manufacturing has been addressed before in the literature. In [106, 107], the authors proposed a fine-pitched IDT with independent fingers that could be reconfigured by changing the interconnection of the electrodes. A similar, fine-pitched geometry was also proposed in [115, 116], but in that case every finger was individually driven with a time-delayed replica of the same signal, and incoming signals from each finger were received independently.

The latter approach seems more promising but requires a significant increase of complexity in the electronics and signal processing domains. Also, individually receiving the signals from each finger is bound to result in a significant SNR degradation.

Apart from the papers specific to IDTs cited above, the generation of Lamb waves using time-delay periodic arrays has been studied in [117], and a large number of relevant works have been published on transducer arrays for ultrasound guided-waves [118–122].



(a) (b)

Figure 2.10: Multi-element IDT: (a) picture; (b) dimensional drawing.

A prototypical variation of the multifunctional IDT presented in Section 2.4 was designed and manufactured with independent electrode connections, but retaining the original patterning (6 finger pairs plus one circular element). This multi-element IDT is shown in Figure 2.10, note that the RTD has been scrapped from this design due to the poor performance highlighted in Section 2.4.3.

The new geometry required moving the connectors to the long side of the piezopolymer film for easier access to the electrodes, which in turn required the segmentation of the PCB clamps, as the active film would have been difficult to attach to curved surfaces otherwise.

Prototypes of the multi-element IDT are still in an early testing stage and thus no results can be presented here.

2.6 COUPLING THE TRANSDUCERS

A firm coupling of the transducers to the target structure surface is paramount to obtain maximum energy transfer in transmission and reception. However, the ability to attach and detach the transducers at will is arguably more important during laboratory experimental phases.

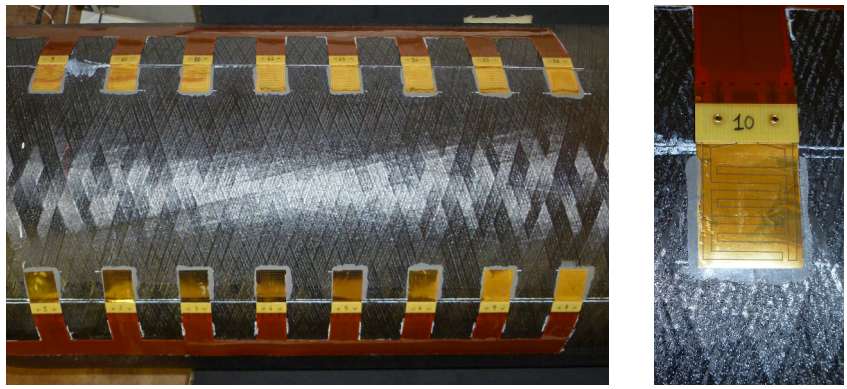
In the latter case, using double-sided tape as coupling medium has proven to be an acceptable solution, as long as the target surface is sufficiently slick and clean (polished aluminum is a good example). Unfortunately, as the surface grows in roughness, tapes with carriers become incapable of maintaining a good adhesion (especially for prolonged periods): in those circumstances, an alternative but still temporary solution might be represented by transfer tapes (i. e.,carrier-less adhesive).

The best mechanical coupling was achieved with permanent bonding through epoxy paste adhesive. Figure 2.11 shows the pictures of two linear IDT arrays bonded to the surface of a filament-wound composite pressure vessel using the Henkel Hysol EA 9394. This epoxy can be cured at room temperature, and is therefore compatible with transducers.

The setup of Figure 2.11 was part of the SHM system presented in Chapter 3.

2.7 PVDF-IN-FLEX AND OTHER SOLUTIONS

The current transducer design and fabrication, with the electrodes etched directly on the metal coating of the PVDF film, adopts mechanical clamping to provide the electrical interconnections between external cables and the electrodes. Two circuit boards with proper copper pad layout are riveted around one end of the piezopolymer film, creating pressure connections with the pads etched on the metal coating of the film. Connectors and wires are then soldered to the PCBs.



(a) (b)

Figure 2.11: Picture of two IDT arrays bonded with epoxy paste adhesive on a COPV: (a) entire picture; (b) detail.

Although direct soldering of the lead wires on PVDF is clearly not possible, as it would melt the film, other solutions have been successfully used to create good electrical contacts (or the electrodes themselves, if using non-coated PVDF), like conductive glues and inks [114, 123].

A different approach to building PVDF sensors that was briefly investigated during the course of this work was completely encasing the piezopolymer film within a flexible circuit made with standard polyimide film.

The idea was to insert an uncoated PVDF film between two flex PCB layers having the electrodes etched on copper (like standard circuit traces), using a couple of adhesive sheets to bond together the three layers. This stack-up is illustrated in Figure 2.12.

An important goal of this stack-up was retaining sensor flexibility, which automatically ruled out the adoption of rigid epoxy paste adhesives such as those used in Section 2.6, even though they had proved to be a good bonding agent for the permanent installation of PVDF transducers.

Since the adhesive layer is interposed between the copper electrodes and the PVDF, it will obviously reduce the electric field applied

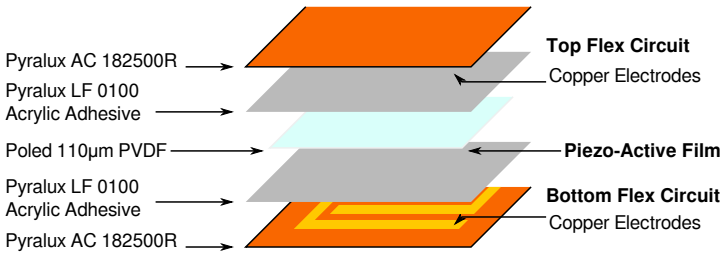


Figure 2.12: Stack-up of a piezoelectric PVDF transducer embedded in a flex circuit.

to the piezoelectric material. Therefore, the adhesive thickness and its dielectric properties need to be carefully controlled. Even so, this drawback may represent an acceptable trade-off when compared to the possibility of designing an arbitrary electrode pattern directly on copper.

Standard flex circuit assembly technologies are incompatible with PVDF, as they involve high-temperature lamination (usually above 180°C). Low-temperature bonding between PVDF and a circuit board, however, was achieved successfully using an acrylic adhesive in [124].

Preliminary bonding tests were performed with an acrylic-based adhesive used for flex circuit assembly (DuPont Pyralux LF sheet adhesive[3], code LF0100), which had two important advantages: its thickness was known (25 µm), as well as its dielectric constant (3.6–4).

A non-pretreated [125], bare, 110 µm thick PVDF film clipping was clamped in a vise together with sheet adhesive and a copper-clad polyimide sheet (DuPont Pyralux AC 182500R[4]), and placed for 24 hours in an oven at 60°C.

Unfortunately the adhesive did not activate at this low temperature. Further tests were repeated for longer times without significantly different outcomes.

3 http://www.dupont.com/products-and-services/electronic-electrical-materials/flexible-rigidflex-circuit-materials/brands/pyralux-flexible-circuit/products/pyralux-lf.html

4 http://www.dupont.com/products-and-services/electronic-electrical-materials/flexible-rigidflex-circuit-materials/brands/pyralux-flexible-circuit/products/pyralux-ac.html

Even if a bonding solution has yet to be found, a transducer made with the proposed stack-up could lift some of the limitations of the current manufacturing process that prevent the patterning of complex electrodes at one's discretion.

Indeed, realizing multiple electrodes with independent connection is fairly difficult with laser etching, as the process forces an identical pattern on both sides of the PVDF film. This, combined with the necessity of keeping wide access traces to the electrodes (the metal coating is extremely thin, around 500 Å, and therefore more resistive than a PCB trace), results in significant stray capacitive loading of the electrodes (which also happen to be piezo-active), with a non-negligible waste of PVDF surface.

With the problem of access traces solved, small transducer arrays could be easily fabricated on a PVDF film, obtaining a transducer already enclosed in a flex circuit, and thus easy to merge with the electronics.

Part II

A SHM HARDWARE TEST BENCH ARCHITECTURE

3

A PROTOTYPE SHM SYSTEM

A first prototype SHM system, integrating all the hardware needed to perform structural health monitoring for a specific application, was developed during a joint project between the Ultrasound and Non-Destructive Testing Laboratory and Thales Alenia Space Italia, funded under Piedmont Region's STEPS2[1] program [45–47].

The purpose of the project was to monitor the status of a space-grade, type III composite-overwrapped pressure vessel (COPV) propellant tank using arrays of IDTs bonded to its exterior surface. The operations performed by the SHM system included impact detection and localization (passive-mode), and structural damage assessment (active-mode).

Normally, the system would stay in passive-mode, continuously listening for an impulsive signal indicating the occurrence of an impact event. After detecting an impact, a software processed the signals recorded by all the transducers to triangulate the strike point coordinates. Although impact detection was performed in-hardware, signal processing and triangulation were done by an external computer.

Active mode could be enabled to perform damage inspection on the COPV by using the arrays in a pitch-catch fashion: each IDT in turn transmitted a pre-defined square wave burst, with the other transducers recording the received Lamb wave packets. The data thus collected were processed and compared to a previously acquired baseline, creating a coarse tomographic image showing the progression of structural damage suffered by the COPV (this task was done by an external computer, as well).

1 Sistemi e Tecnologie per l'Esplorazione Spaziale

3.1 OVERVIEW OF THE HARDWARE

The hardware platform was a combination of custom electronics and evaluation boards stuffed inside a 4U 19″ subrack enclosure (shown in Figure 3.1).

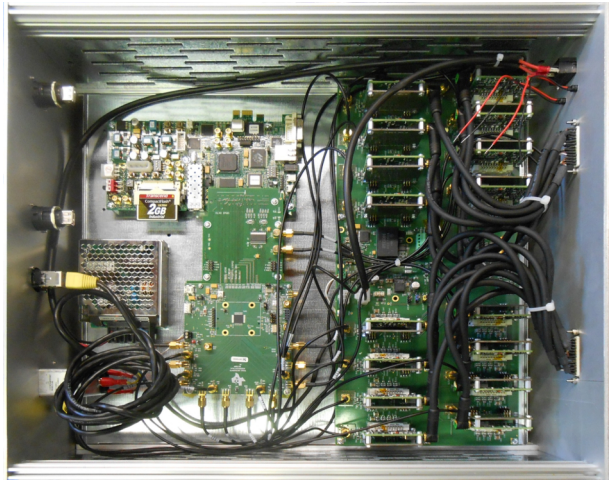


Figure 3.1: Picture of the interior of the prototype SHM system hardware subrack enclosure.

A simplified block scheme of the hardware is shown in Figure 3.2. Except for the analog front-end cards (described below), most of the additional custom electronics—the backplane board, hosting the front-ends, and an FMC adapter, routing the output lanes of the ADC to the FPGA—was designed to interface and power the core system components: the FPGA card (Xilinx Spartan-6 FPGA SP605[2]), and the ADC board (Texas Instruments AFE5851EVM[3]). The complete schematics of the backplane are available in Appendix A.

2 https://www.xilinx.com/products/boards-and-kits/ek-s6-sp605-g.html
3 http://www.ti.com/tool/afe5851evm

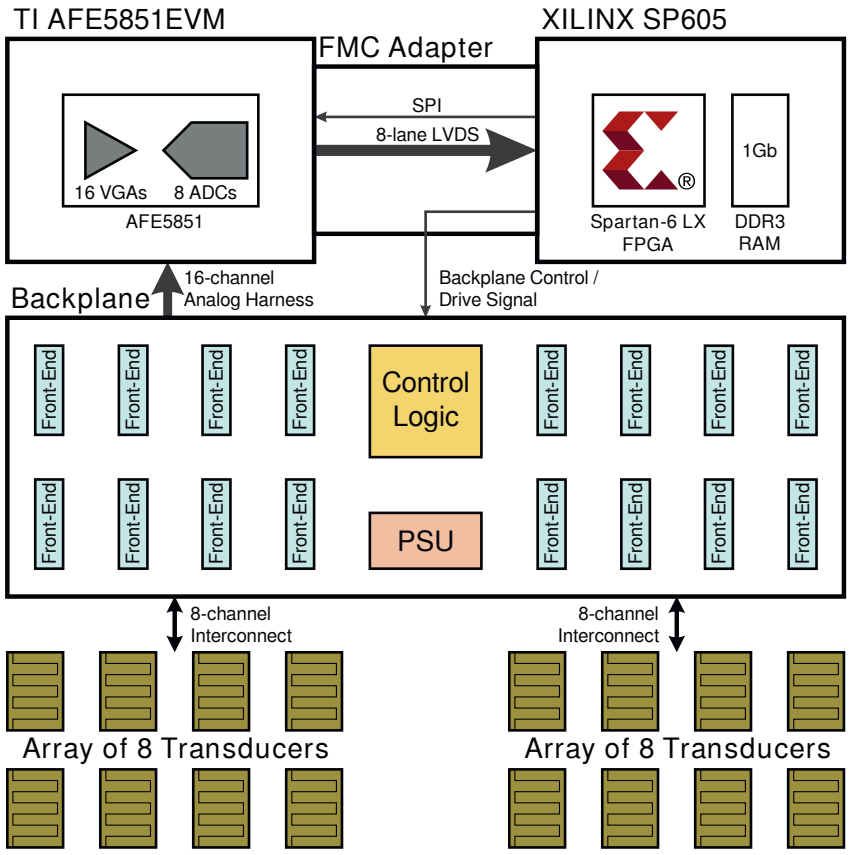


Figure 3.2: Block scheme of the prototype SHM system hardware.

3.2 THE ANALOG FRONT-END

Each one of the 16 transducers supported by the platform was connected to its own analog front-end, a small daughter card that included the transmission power stage and part of the signal conditioning circuitry used for reception. Those cards completely depended on external hardware to perform their functions: drive and control signals had to be issued from the external logic, as no controller was included on the cards, and all of the four supply rails required to power

the circuits had to be provided externally. The front and rear pictures of the analog front-end (latest revision) are shown in Figure 3.3, card size is 53×40 mm excluding the connectors.

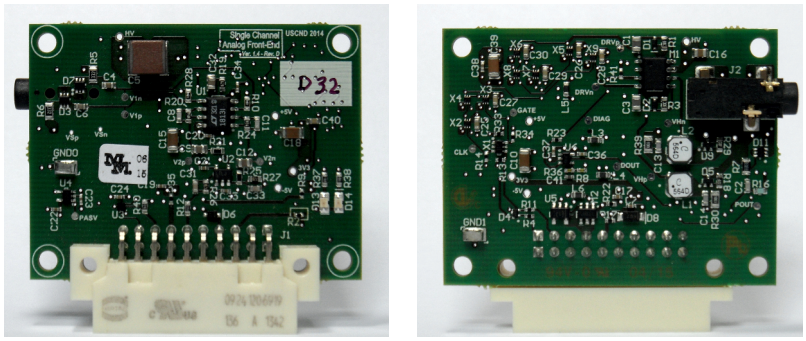


Figure 3.3: Pictures (front and rear) of the analog front-end card developed for the prototype SHM system. Board size is 53×40 mm.

The electronics of this front-end were designed to satisfy very specific requirements, in particular for what concerns the transducer driver (described in Section 3.2.2), and therefore lacked the versatility needed to approach structural health monitoring tasks with *state-of-the-art* techniques.

The complete signal conditioning chain was not confined to the analog front-end daughter cards, but split between different physical boards. Therefore, it is better understood by examining Figure 3.4, where the block scheme of the front-end daughter card is shown together with the complementary circuitry that was present on the backplane and inside the AFE5851 data converter chip.

The transducer diagnostic functions built-in the analog front-end are not treated in this dissertation, and were thus not included in Figure 3.4. The analog multiplexer present on the daughter card—the same component used on the backplane: a Maxim MAX14589E—had the purpose of switching one of the analog outputs between passive mode and diagnostics.

The following sections briefly describe the main functional blocks present on each analog front-end card. The complete daughter card schematics are reproduced in Appendix A.

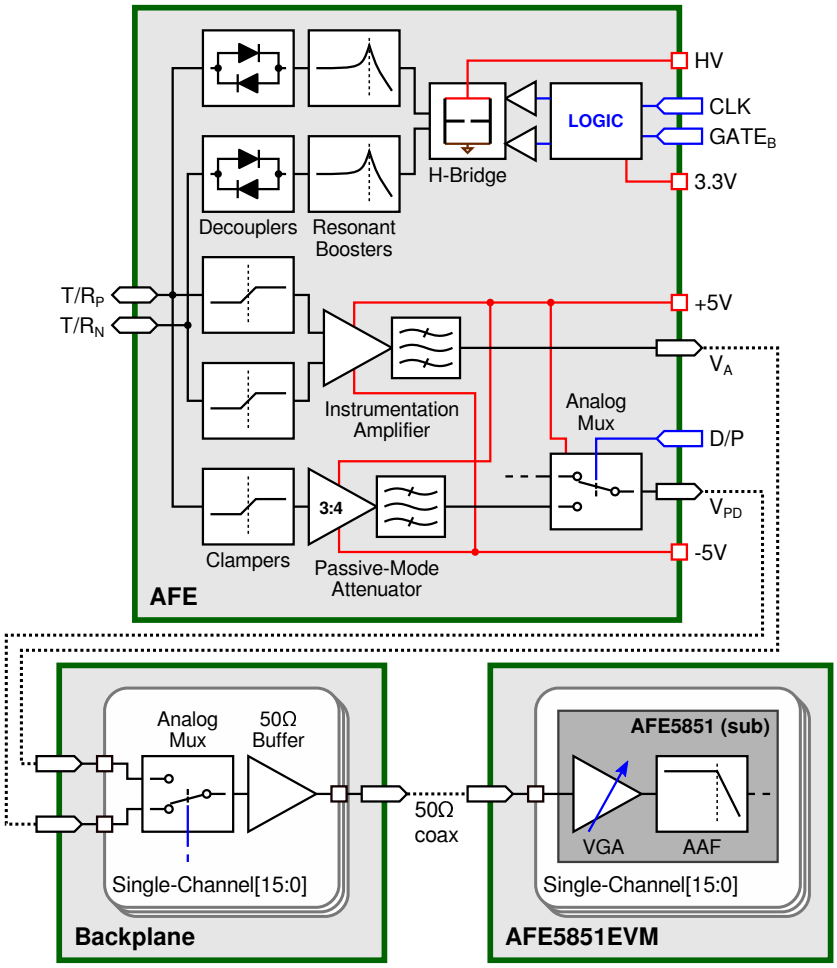


Figure 3.4: Block scheme of a single-channel analog front-end daughter card, completed by the signal conditioning blocks provided by other parts of the SHM system. The scheme is missing the transducer diagnostic section, which is not covered in this dissertation.

3.2.1 *Active-Mode Receiver*

The active-mode receiver consisted of a custom instrumentation amplifier having ~ 60 dB of gain within the 100 kHz–1 MHz bandwidth. The characteristics of this amplifier are shown in Figure 3.5 (transfer function), and Figure 3.6 (common-mode rejection ratio).

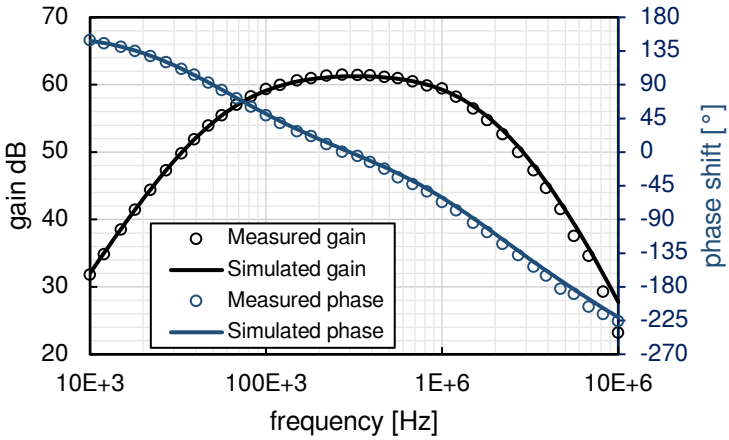


Figure 3.5: Simulated and measured frequency response of the instrumentation amplifier.

3.2.2 *Resonant Transducer Driver*

The transducers were driven with a H-bridge square-wave pulser, supporting up to 90 V of supply voltage, followed by two L-C resonators. A simplified schematic is shown in Figure 3.7. A combinatorial circuit made with discrete CMOS inverters was used to feed the two halves of the H-bridge with complementary signals, starting from two LVCMOS-33 logic inputs (clock and gate signals). The high-side PMOS of the bridge were driven with a bootstrap circuit connected directly to the NMOS gates, so that there was no dead-time control between the switches.

The clock signal could, in principle, be a pulse train of frequency up to 5 MHz and arbitrary duty ratio. However, the presence of voltage-

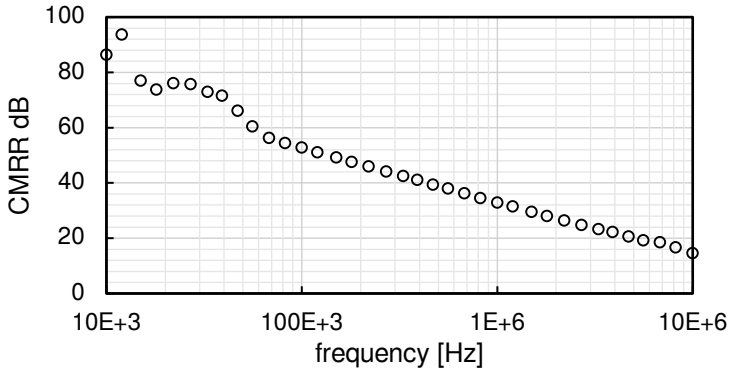


Figure 3.6: Measured common-mode rejection ratio of the instrumentation amplifier.

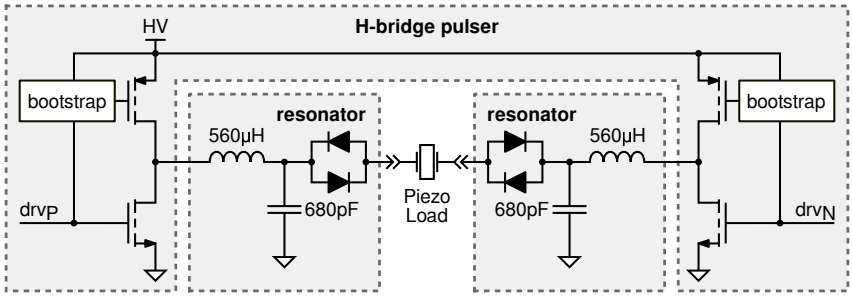


Figure 3.7: Simplified schematic of the H-bridge transducer driver with L-C resonant voltage boosters.

boosting L-C networks that, together with the transducer impedance, fixed a resonance frequency (~ 250 kHz), discouraged the adoption of drive signals with a frequency not close to said resonance. Moreover, the large current sunk by the H-bridge during switching limited the feasible length of the pulse train, as the MOSFETs could heat up and the supply rail dwindle under the load.

Several strategies exist to design electrical impedance matching (EIM) networks for piezoelectric transducers, both narrow-band [126], and broadband [127, 128]. The L-C network included in this driver was designed as a resonant booster to maximize the transmission signal around a certain frequency that was predicted to include the

matching point between the A_0 mode wavelength of the structure, and the IDT finger pitch.

3.2.3 *Duplexer Stage*

Transmit / receive duplexing was implemented with a simple diode clamp protecting the inputs of the signal conditioning electronics. This solution required the introduction of limiting resistors (3.3 kΩ) in series with the transducer connections (as the drive signal could reach several hundred volts), thus creating a voltage divider directly at the preamplifier inputs.

3.2.4 *Passive-Mode Receiver*

Given the amplitude of impact response signals, several orders of magnitude higher than those usually received in active-mode, the passive-mode receiver was actually a $\sim 3:4$ resistive divider followed by an op-amp buffer (Texas Instruments OPA172). This receiver was connected to only one of the two electrodes of the transducer, to further cut in half the inbound signal amplitude.

3.3 DATA ACQUISITION AND HANDLING

Since the ADC (a Texas Instruments AFE5851) had 16 total input channels, the two analog signals coming from the daughter cards (active and passive-mode receivers) had to be multiplexed together before being routed to the data acquisition card. Therefore, only one of the analog signals conditioned by the front-end cards could be acquired at any given time. The analog multiplexers were toggled by the system controller when switching between passive-mode and active-mode.

The ADC had a total of 8, 12-bit sampling cores multiplexed to 16 single-ended inputs. Each input channel also integrated two programmable analog signal conditioning blocks (hence the denomination AFE5851): A variable gain amplifier (−5 dB–31 dB, also suppor-

ting time gain compensation) and a programmable anti-aliasing filter. The ADC sampled at a fixed rate of 20 MSps per channel in both active and passive mode—even though the stream was later down-sampled by 2 when operating in passive mode—and transmitted the data to the FPGA over 8 LVDS (low-voltage differential signaling) lanes.

The FPGA collected and stored the 16 time traces in a 10k (samples per channel) circular buffer inside the system memory. In passive mode, data acquisition was performed continuously, overwriting the oldest samples over time, and the FPGA took care of interrupting the recording process as soon as an impact event was detected. In active mode, on the other hand, data acquisition was single-sequence and synchronized with the emission of the transducer drive signal.

Interleaved sampling was used to accommodate the 16 input signals to the 8 ADC cores, which operated at the actual rate of 40 MSps. The damage detection algorithm used in active mode did not have particularly strict inter-channel timing requirements, as each trace acquired from the transducer array was processed independently of the others, and only needed a repeatable timing between subsequent pitch-catch acquisitions.

Passive mode, on the other hand, assumed the time alignment of all the 16 traces acquired during an impact event to extrapolate a differential time-of-arrival between the transducers, which was then used to triangulate the point of impact on the COPV surface. In this context, neglecting the fixed delay affecting half the traces, arising from the ADC performing interleaved sampling did result in an error, which was however completely negligible in light of the overall localization accuracy achieved by the system.

All the signal processing tasks (damage detection and impact triangulation) were performed off-line on the host computer. The memory contents stored while in passive mode (after an impact event), and the active mode traces were collected by the host computer through an USB-to-UART bridge. This interface was also used to configure and control the instrument.

3.4 LIMITATIONS OF THE PROTOTYPE SHM SYSTEM

While the system presented in this chapter performed fairly good in its intended application [47], it was affected by a number of shortcomings that prompted the profound revision that is the subject of this dissertation.

In light of the shift towards a sensor network paradigm envisaged for the future research efforts, the first and foremost problem of this system was its monolithic architecture. While having all the electronics encased into a single unit, working in unison, proved to be a viable simplification in this specific application and at this stage of the project, having a hardware that could potentially mimic a distributed SHM system will lead to exposing and tackling the issues hiding behind distributed SHM electronics, and the scalability of such systems.

Beside the architecture, several other design choices limited to varying degrees the usefulness of the prototype SHM system:

- The front-end cards provided a single transmission / reception channel per transducer, limiting their usability with the next generation of multi-functional and multi-element devices described in Section 2.4 and Section 2.5.
- The original active mode inspection procedure relied on the transmission of only one signal at a time, and thus the electronics did not allow the simultaneous operation of multiple transducer drivers. Moreover, the drivers included hard-wired L-C resonant voltage boosters that fixed their frequency response.
- Only one analog signal could be acquired at any given time from each front-end card, and no feedback channel existed to capture the transducer driver outputs.
- Signal conditioning, and especially the duplexer stage, was elementary and could be improved.
- The electronics in general were too bulky for the functionalities they provided, making their upscaling unfeasible.

4

DEVELOPMENT OF A MODULAR SHM SYSTEM

4.1 THE PANDORA ARCHITECTURE

Project Pandora started with the overarching aim of developing wired sensor networks to be deployed on composite pressure vessels (or other, plate-like composite structures). The road to get there, however, is long and steep.

The envisaged sensor node will require the integration of many diverse functional blocks, some of them even needing different semiconductor technologies:

- High-voltage ultrasound transducer driver.
- Low-noise analog front-end.
- Analog-to-digital converter.
- Signal processing and communications.
- Power converters.

The design requirements of these components are also strongly connected to the health monitoring techniques that will be implemented, and thus a sound sensor node design can only be achieved after a thorough experimental phase has been completed, evaluating which techniques provide the best results and should be supported by the final sensor network.

An intermediate development step was therefore needed before being able to move into sensor integration: the creation and adoption of a testbench system to define the paradigm and requirements of a SHM sensor network architecture.

Such system was devised at the architectural level in a top-down fashion, but its actual design and testing was approached from the

bottom up, as the system was planned to be modular from the very beginning.

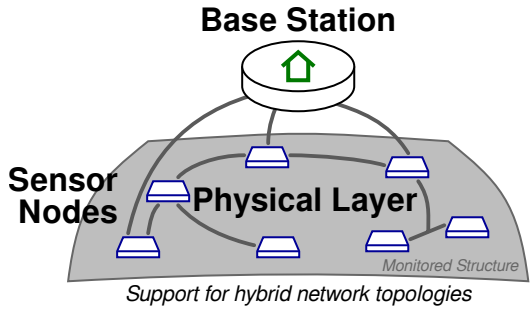


Figure 4.1: Simplified representation of a Pandora wired sensor network.

The proposed architecture mimicked the natural hierarchy of a wired sensor network, with a number of nodes, a few physical channels, and a base station (shown in Figure 4.1).

The sensor nodes consisted of self-contained electronics and transducers, and were therefore represented by separate daughter cards in the testbench system. The communication channel and the base station, on the other hand, were to be both included in a backplane card that could host a number of identical daughter cards, providing the means to locally emulate a physical channel between them. A schematic illustration of the testbench architecture is shown in Figure 4.2.

The daughter cards were the first part on which the development process was started. The various functions required by a sensor node were split in different physical modules according to the architecture shown in Figure 4.3.

Design and testing of the daughter card components started from the transmission (Section 4.3) and reception (Section 4.4) modules, as they were the only parts strictly requiring custom electronics.

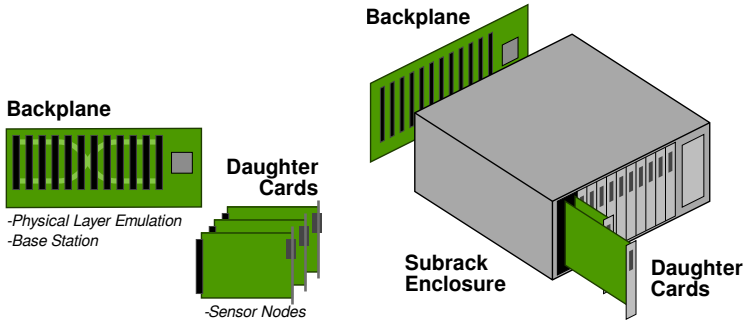


Figure 4.2: Illustration of the Pandora testbench instrument: (a) main components and their function; (b) assembled instrument.

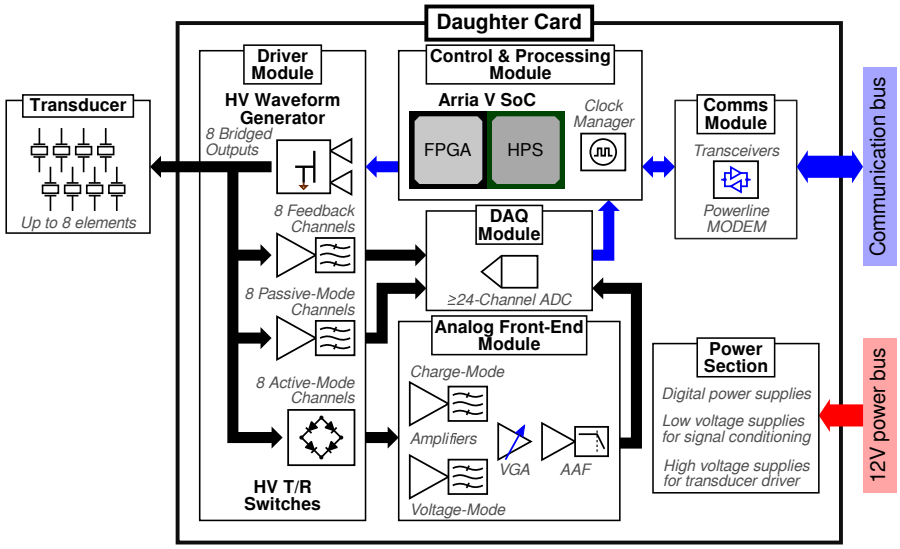


Figure 4.3: Target architecture of a daughter card.

The other components were temporarily covered for by development kits and evaluation modules: an Intel FPGA Arria V SoC development kit[1] was used in place of the processing core, while the whole data acquisition part was replaced by the combination of a Texas Instruments ADS52J90 evaluation module[2] and its companion TSW14J56 data capture evaluation module[3].

The design plans of the Pandora architecture are further expanded in Chapter 5, where the parts of the testbench system still under development are fleshed out, highlighting the future work required to complete the platform and make it capable of stand-alone operation.

The subsequent Chapter 6 hints at the eventual development of wired sensor networks for SHM, and the main challenges that will be encountered during the final stage of project Pandora.

4.2 TARGET FEATURES OF THE TESTBENCH SYSTEM

Since project Pandora started soon after commissioning the system described in Chapter 3, with the intent of following in its tracks, the initial target requirements of the testbench system were mostly inherited from the characteristics of the prototype SHM system.

The fundamental idea was that the new design had to improve upon, or at least replicate the features and performance that were instrumental to the previous system functioning. In particular, the essential features that needed to be included were:

- Support for active-mode with multiple transducers, each one capable of operating half-duplex.
- Support for passive-mode with the same transducers.

Several hardware and software requirements sprung directly from the points listed above as results of the activities performed using the prototype SHM system, while others arose from the research

1 https://www.altera.com/products/boards_and_kits/dev-kits/altera/kit-arria-v-soc.html
2 http://www.ti.com/tool/ads52j90evm
3 http://www.ti.com/tool/tsw14j56evm

that was undertaken in the period immediately following the end of the STEPS2 project. For instance, the adoption of multi-functional / multi-element transducers described in Chapter 2 was never contemplated before the beginning of project Pandora.

An important planning feature of the testbench system architecture had to do with the envisioned role of the daughter cards. The previous section has introduced them as node electronics that will handle a single transducer, interacting with other identical daughter cards to form a distributed health monitoring system. While this represented the core idea that will be pursued, the long expected development time also required a compromise solution that could allow some research on SHM applications to be performed before completing the whole testbench system. To address this need, the daughter cards were also structured to be able to interface with multiple, independent transducers and operate stand-alone during the initial phase of the project.

A short list of the main requirements of the testbench system, covering the active-mode part that is the focus of this dissertation, is presented below:

- Transmission and reception bandwidth: 100 kHz–1 MHz.
- Support for high-impedance capacitive transducers (< 1 nF).
- Pre-amplifier voltage gain at center band: 60 dB.
- Burst-mode transmission with at least 50 V amplitude.
- 8 independent half-duplex transmission / reception channels.
- Synchronous transmission and data acquisition.
- ADC with 12 bits at 20 MSps per channel or better.

It is expected that the testbench system will see many of its current requirements amended in the future, following an iterative design process that will proceed side-by-side with the research activity exploring its applications. This is the main reason behind keeping the system as modular as possible.

4.3 TRANSMITTING SIGNALS

Ultrasonic transducer drivers capable of arbitrary waveform generation (AWG) come in many forms, but are generally subdivided in two categories: linear and switch-mode.

Many commercial power amplifiers are available to drive ultrasonic transducers and generate arbitrary waveforms. Although an exposition of this subject is beside the scope of this dissertation, it should be mentioned that fully-integrated, high-voltage linear amplifiers for ultrasound are an emerging research topic [129, 130].

On the switch-mode side there is a well developed market of integrated multichannel pulsers manufactured by numerous companies. Those pulsers include a set of MOSFET switches connected to fixed, usually high-voltage (hundreds of volts) supply rails that are driven with pulse-width modulated (PWM) logic signals to re-create approximate waveforms at their output. Over the years, several techniques have been proposed to perform PWM with ever increasing quality of the output waveforms [131–136].

Modulating the pulse widths is not the sole option to shape arbitrary signals with a pulser. In recent times, ultrasound pulsers having multiple switches connected to different voltage *levels* have started to proliferate, allowing the development and adoption of specific multilevel pulse width modulation schemes [137–139], a technique that was originally developed for power inverters [140].

The pulse-width modulation schemes cited above, including the multilevel ones, are slightly different from the approach used in the current work, and described in the sections that follow. The intended application played an important role in distancing the proposed ultrasound driver from other solutions, as the target bandwidth was in the range $\leqslant 1$ MHz, whereas many of the works cited were oriented towards high-frequency imaging. This difference opened to the possibility of introducing a significant separation between the PWM carrier and the baseband signal, and operate in pure class-D with output reconstruction filters.

4.3.1 *A Class-D Ultrasound Transducer Driver*

A 8-channel transducer driver module was designed and manufactured following an architecture similar to common class-D amplifiers for audio applications, only operating at ultrasound frequencies and using a bridged, multilevel power stage.

The board itself was designed following the ANSI/VITA 57.1 standard as much as possible [141]: although the digital part was compliant with the standard, the analog section presented high-voltage signals that required a secondary board-to-board connector (a Samtec QMS-PC[4]). The final module dimensions were 120×69 mm, longer than a standard mezzanine card.

The complete module schematics can be found in Appendix B.

4.3.1.1 *Multilevel Power Stage*

The building blocks of the transducer driver were two commercial, multichannel ultrasound pulser chips (Hitachi HDL6V5583), and a bank of L-C reconstruction filters. Overall, the pulser ICs provided 16 half-bridge power stages with split supplies, plus an active clamp and damper tied to ground (i. e., a three-level power stage). The driver module used two such channels, followed by two reconstruction filters, in a bridged configuration to obtain 8 copies of the five-level power stage shown in Figure 4.4. All the pulser channels operated with externally provided supplies of $|\mathrm{HV}| = 48$ V.

Every HDL6V5583 channel was controlled by two dedicated input logic signals, which were fed to an internal circuitry tasked with level shifting and MOSFET gate driving. It was assumed that the internal logic would also take care of imposing switching dead-time, although no mention of such function was explicitly made in the available documentation.

The truth table showing the various voltage levels that could be generated by each bridged pulser channel ($V_{DO,P}$-$V_{DO,N}$ in Figure 4.4) is shown in Table 4.1. A pulser channel receiving the H H logic input automatically enabled the active clamp and damper: simultaneous

4 https://www.samtec.com/products/qms-pc

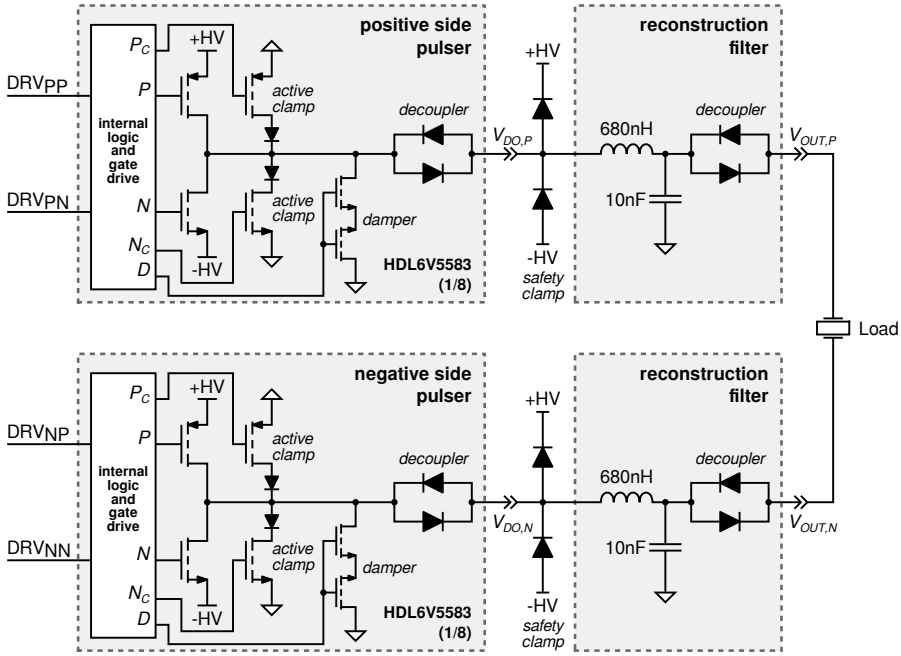


Figure 4.4: Schematic of the differential power stage that drives each transducer channel.

turn-on of the positive and negative switches was not allowed by the internal logic of the pulser chips, as it would short the high voltage supplies.

Auxiliary output safety clamping diodes were added to protect the chip from high-voltage overshoots caused by the load, as recommended by the manufacturer's datasheet.

PULSER CHIP CHARACTERISTICS AND LIMITATIONS As shown in Figure 4.4, each channel of the HDL6V5583 included two complementary drive MOSFETs, two complementary clamp MOSFETs with blocking diodes, and a back-to-back MOSFET damper. The electrical characteristics of the MOSFETs reported by the manufacturer on the datasheet are listed in Table 4.2.

The switch transition times and maximum drive frequency were also specified on the datasheet, albeit for specific operating conditions

DRV_{PP}	DRV_{PN}	DRV_{NP}	DRV_{NN}	OUTPUT
H	L	L	H	$+2 \cdot HV$
H	L	H	H	$+HV$
H	H	L	H	
H	L	H	L	0
H	H	H	H	
L	H	L	H	
L	H	H	H	$-HV$
H	H	H	L	
L	H	H	L	$-2 \cdot HV$

Table 4.1: Output levels ($V_{DO,P}$-$V_{DO,N}$) of the ultrasound pulser and their corresponding logic inputs. Hi-Z states are not shown.

	R_{ON}	C_{OSS}	$I_{D,SAT}$
High-side drive PMOS	7 Ω	27 pF	−1.8 A
Low-side drive NMOS	7 Ω	11 pF	1.8 A
PMOS active clamp	13 Ω	15 pF	−1 A
NMOS active clamp	13 Ω	6 pF	1 A
Back-to-Back damper	500 Ω typ.	—	—

Table 4.2: Summary of the characteristics of the HDL6V5583 MOSFETs declared in the component datasheet.

that did not correspond to our application. In the absence of conclusive information, it was assumed that the pulser chip could operate up to a maximum of 25 MHz (at 0.5 duty ratio) with ±48 V supply rails (which roughly correspond to half the rated supplies of the chip, ±100 V), meaning that a minimum pulse width of $t_{PW,min} = 20$ ns had to be respected whenever a switch was toggled. This assumption was carried through the design of the pulse-width modulation strategy that was eventually used to generate the output signals.

RECONSTRUCTION FILTERS The discrete reconstruction filters of Figure 4.4 were designed to ensure a certain amount of carrier rejection regardless of the electrical characteristics of the transducer load. 10 nF capacitors were chosen to dominate over the expected capacitance range of the transducers described in Section 2.4, because a strong high-frequency residual of the carrier (in the tens of megahertz) could shock the mechanical thickness-mode resonance of the PVDF film. The inductor value of 680 nH directly followed from the chosen capacitor value to obtain a filter roll-off above ~2 MHz.

L-C reconstruction filters for class-D audio amplifiers are designed by considering the damping introduced by the load itself, which usually presents a low impedance [142]. When driving ultrasonic transducers like those described in Section 2.4, however, the load provides no damping of its own, and the reconstruction filters would end up retaining a high Q factor, with a very sharp resonant peak.

In the proposed design, damping was introduced by the power stage itself as an average behavior resulting from the continuous toggling of the switches. For each pulser channel, the active clamp and damper to ground were always closed as soon as the high-voltage switches were opened, never leaving the output in a high-impedance state.

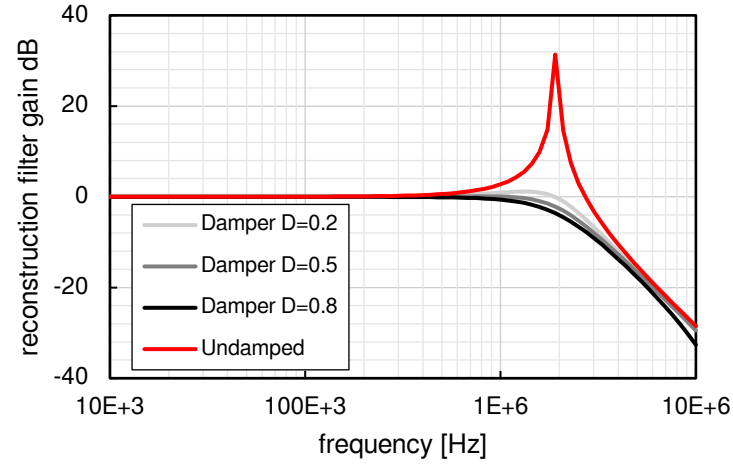
The actual damping effect of the switching power stage can be easily evaluated using a simulator that can perform periodic small-signal analysis of a switch-mode circuit, such as SIMPLIS[5].

5 SIMPLIS Technologies, Inc., Portland OR, 97240-0084, United States; website: https://www.simplistechnologies.com/.

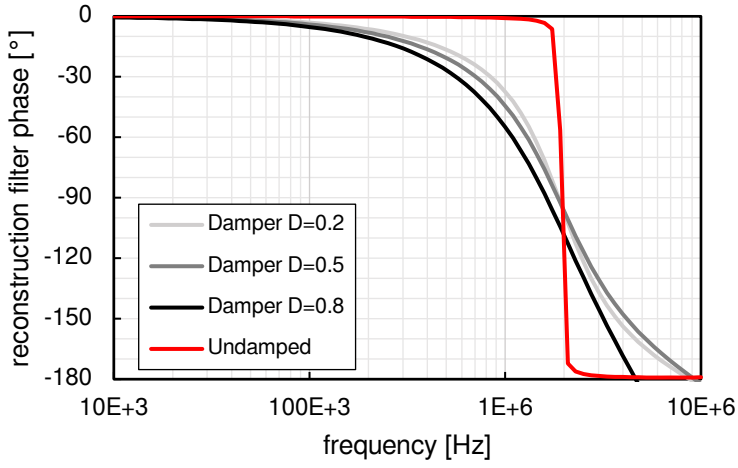
The plots of Figure 4.5 show a comparison between the undamped response of the L-C reconstruction filter (which includes the effects of component parasitics), and the same filter connected to the pulser power stage operating at steady state in a single-ended configuration, corresponding to half the drive circuitry shown in Figure 4.4. A capacitive load of 100 pF, modeling the transducer, was used in both cases.

Both the switching frequency and the duty ratios affect the reconstruction filter damping: Figure 4.5 was simulated with a carrier frequency of 5 MHz and various duty ratios of the positive and negative drive switches. The damper duty ratio indicated in the plot legend corresponds to the switching period interval where *both* drive switches remain open (i. e., the logical NOR of the two control signals), which thus becomes the duty ratio of the active clamp and damper.

As evidenced by the plots, the longer the active clamp remains closed (i. e., lower duty ratio of the energizing switches), the more the reconstruction filter is damped.



(a)



(b)

Figure 4.5: Simulated frequency response of the reconstruction filters with and without the average damping introduced by the pulser: (a) gain; (b) phase.

4.3.1.2 *Pulser Power Supplies*

The pulser was externally supplied with split ±48 V rails, though the module could handle up to ±100 V. The original design, which can still be seen in the schematics of Appendix B, also included some point-of-load (PoL) linear regulators with ±46 V outputs that were supposed to improve the transient response to the current spikes sunk by the pulser.

In principle, supplying a switching circuit that rapidly draws large currents within a short time frame could be done by a bank of capacitors. If the total stored energy is sufficiently large, the voltage rail will drop slowly while switching and then, as the circuit becomes idle, the power supply will slowly replenish the charge in the capacitors.

This approach works well and has been used extensively in ultrasound systems where the transmitter operates with low duty cycle: even though the power stage can sink significant amounts of current, it does so for a small time compared to the pulse repetition period, and thus the average current drawn from the power supply is reasonably small.

As the transmission system is operated for longer times (i. e., longer output waveforms), the capacitance required to maintain a steady power rail must inevitably grow, and with it the recovery time (unless the power supply is also scaled up). Since the capacitance density per unit volume decreases with increasing voltage rating of the capacitor, this whole power supply scaling strategy may become unfeasible in certain scenarios where space is not available.

The idea of adding post-regulators to the high-voltage supplies goes in the direction of splitting the performance requirements between the voltage boosting circuit (a somewhat slow switch-mode power supply that generates the ±48 V rails starting from the 12 V bus), and PoL linear regulators having very fast transient response.

This architecture was attempted in the first driver module prototype by including some integrated, high-voltage, linear PoL regulators. Unfortunately it did not provide satisfactory performance improvements, as the transient response of the regulators was slow and

fixed by design. Therefore, the pulsers were eventually attached directly to the external ±48 V power supplies.

Operating the driver in continuous wave (CW) was not possible at high supply voltage due to excessive switching losses. Indeed, the HDL6V5583 datasheet specifies CW operation with ±5 V supplies and reduced current drive. The driver module described here did not include adjustable regulators to step down the power rails, although the introduction of such capability has been planned (see Section 5.2).

4.3.1.3 *Ancillary Electronics*

Besides hosting the eight differential output channels, the driver module also provided a part of the signal conditioning circuitry required to use the attached transducers in reception, and thus make the design half-duplex. The rationale behind integrating a subset of the reception chain on this card was to keep the high-voltage signals as much as possible confined to a dedicated section of the system: the only high-voltage traces exiting from the driver module were those that link directly to the transducers, which are not planned to be tapped by any other daughter card circuit.

The reception components are described later in this section, and include: the output feedback sense (Section 4.3.5), the passive mode receivers (Section 4.3.6), and the transmit / receive switches (Section 4.3.7).

The 32 logic signals that controlled the pulser chips were sourced directly from off-board through the FMC connector, while the module configuration was handled by a local GPIO expander (Texas Instruments TCA6424) interfaced via an I²C bus.

The complete block scheme of the driver module is shown in Figure 4.6, and pictures of the manufactured prototype are shown in Figure 4.7.

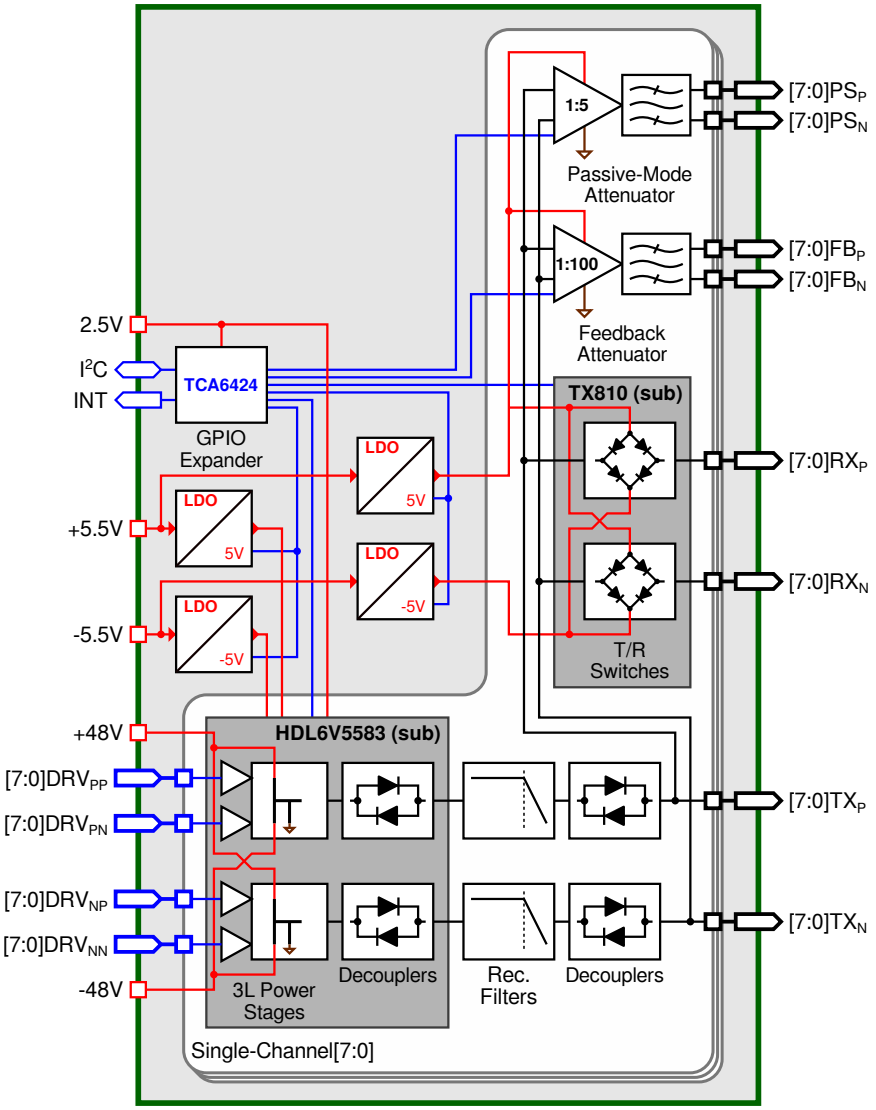
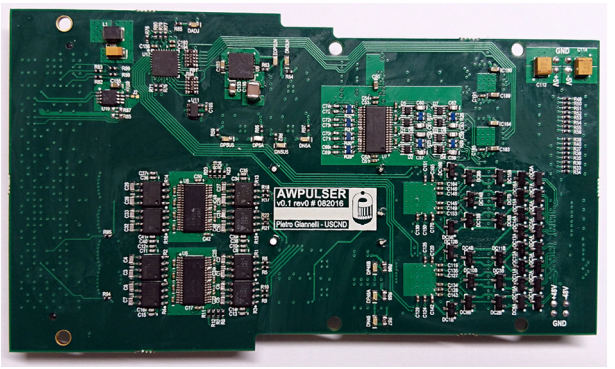
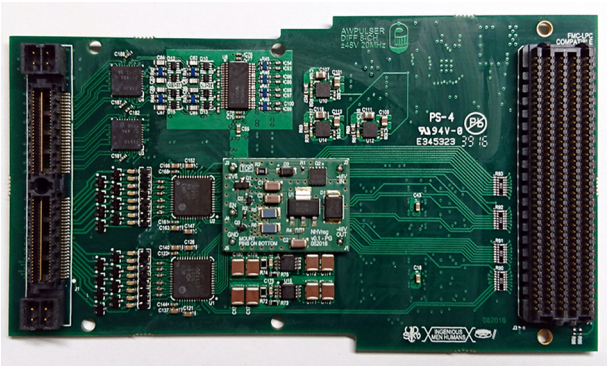


Figure 4.6: Block scheme of the eight-channel transducer driver module.



(a)



(b)

Figure 4.7: Pictures of the ultrasound driver module prototype: (a) Top side; (b) Bottom side showing the analog and digital connectors. Board size is 120×69 mm.

4.3.2 *Multilevel Pulse Width Encoding*

Generating arbitrary waveforms with a five-level class-D amplifier required the ideation of an appropriate modulation strategy.

In a generic class-D amplifier, the switch-mode power stage outputs pulses of varying duty ratio at a certain modulation frequency (the carrier), higher than the bandwidth of the baseband signal that need to be reproduced. The reconstruction filter present between the power stage output and the load is such that it rejects the carrier and delivers a *reconstructed* baseband signal to the load.

Ideally, the reconstructed output signal should be dictated by the per-period average of the pulse-width modulated (PWM) output, that is it should be a perfect interpolation of the integral over one modulation period of each pulse generated by the power stage. If the n-th pulse has length T_n, amplitude V_P (which represents the supply rail of the switching power stage), and the carrier has frequency f_{PWE}, the corresponding voltage $V_{out,n}$ reconstructed at the output after one period would be:

$$V_{out,n} = f_{PWE} \int_0^{T_n} V_P \, dt = V_P T_n f_{PWE} = V_P D_n \tag{4.1}$$

Where $D_n = T_n f_{PWE}$ is defined as the duty ratio of the n-th pulse. This per-period average results in a staircase signal similar to the output of a digital-to-analog converter (DAC), which then needs to be interpolated by the reconstruction filter, obtaining the intended output waveform. The process is illustrated in Figure 4.8.

The explanation above is of course an oversimplification used to introduce the basic idea behind class-D amplifiers: that the *sampled* amplitude of a baseband signal is converted into the varying duty ratio of a pulse train, and a filtering action can be used to recover such information.

In reality, the reconstruction filter of a class-D amplifier performs baseband signal recovery with limited efficacy, resulting in a significant residual carrier ripple and time delay. A general performance improvement is obtained by rising the carrier frequency to oversample the baseband signal, at the cost of increased power losses. The big

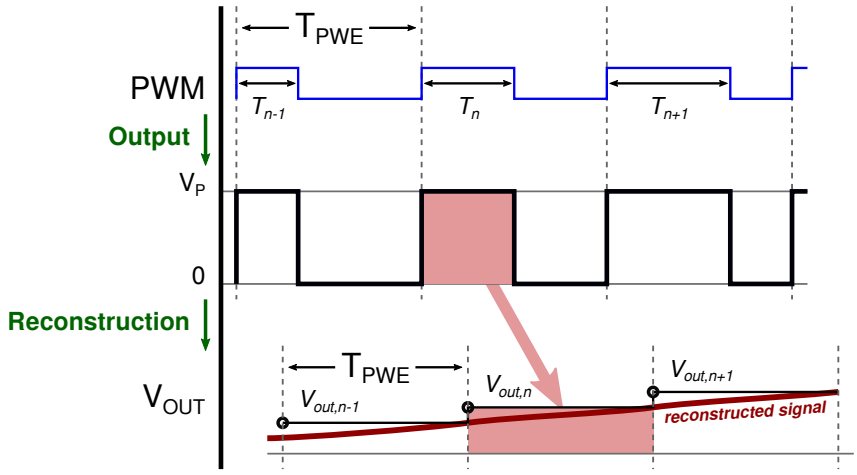


Figure 4.8: Basic depiction of class-D signal generation.

advantage lies, however, in the simplicity inherent to the hardware of a class-D, where a single voltage supply is needed to generate all the intermediate levels to ground by toggling a couple of switches at a sufficiently high frequency.

As long as the reconstruction filter is able to reject the carrier and pass the baseband signal, the output waveform amplitude is entirely defined by the sequence of pulse duty ratios generated by the switching power stage, and its voltage supply rail. In a multilevel PWM, the amplitude of the pulses V_P is not fixed but can assume a certain set of predefined levels which, together with the duty ratio, represent two degrees of freedom to generate the output signal.

As explained in Section 4.3.1, each channel of the transducer driver module allowed to generate a total of 5, equally-spaced levels through four logic drive signals. A pulse width encoding (PWE) algorithm was thus devised to transform arbitrary signals sampled at a fixed rate (equal to f_{PWE}) into four pulse-width modulated logic signals.

Note that the modulated logic signals will henceforth be referred to as DRV_{PP}, DRV_{PN}, DRV_{NP}, and DRV_{NN}, while the encoded duty ratios corresponding to the n-th sample of the original waveform will be indicated with $D_{n,PP}$, $D_{n,PN}$, $D_{n,NP}$, and $D_{n,NN}$.

Since the encoding process was completely digital, the duty ratios of the PWE signals had to be quantized according to a minimum duty step δD, corresponding to an integer divisor of the PWE period, div. This divisor was also chosen to be even.

$$\delta D = \frac{1}{div \cdot f_{PWE}} = \frac{T_{PWE}}{div} \tag{4.2}$$

As will be shown later in Section 4.3.3, the duty resolution and PWE period are linked together by the clock (f_{SYSCLK}) of the hardware used to generate the modulated output logic signals, and this imposes an absolute limitation on the minimum achievable pulse width resolution.

The proposed PWE is therefore an algorithm that takes an input sequence of samples S_n, and converts each one of them into four encoded words representing the duty ratios of the four logic signals required to drive the pulser chips (i. e., *not* a floating or fixed point value between 0 and 1), Figure 4.9 visually explains the process. The reconstructed output shown at the bottom includes a token one-period time delay, whose actual value depends on the reconstruction filter, and neglects all the residual carrier ripple. The various amplitude scales, intentionally omitted from Figure 4.9, are determined by the hardware.

The values that these four words can assume could be, in principle, any integer number between 0 and div (representing, respectively, 0 to 1 duty ratios). However, there are additional limitations arising from other system constrains that need to be taken into account.

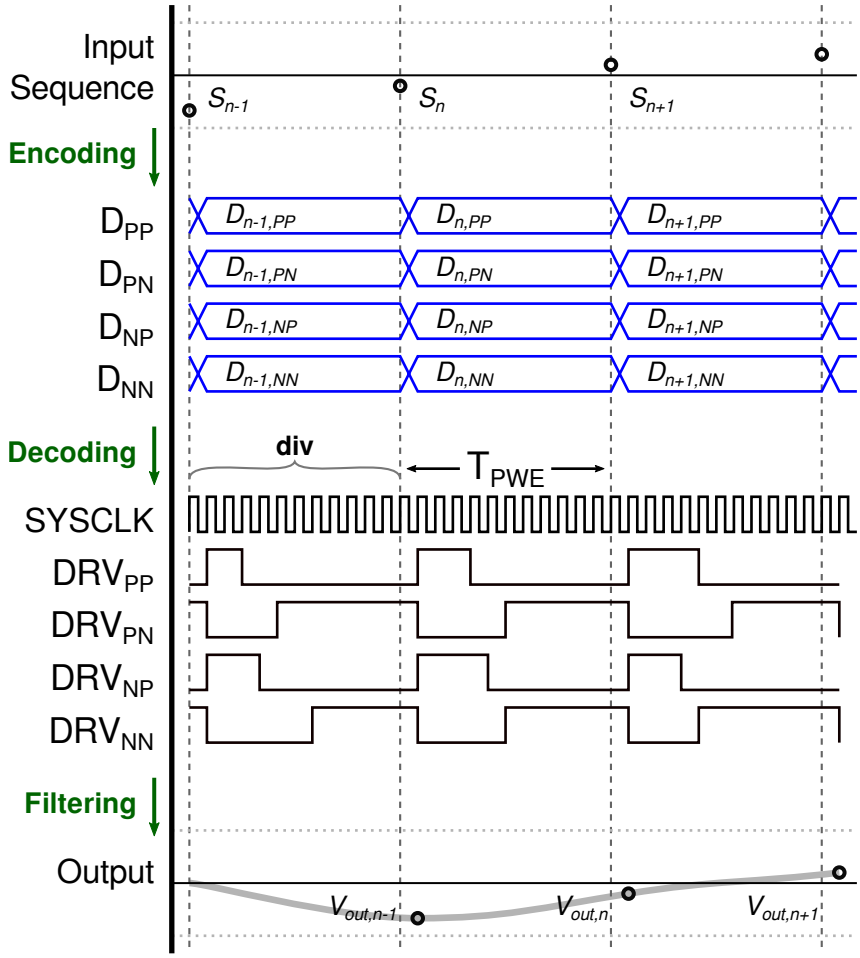


Figure 4.9: Simplified graphical representation of the five-level signal generation process.

4.3.2.1 *Limitations of the Duty Ratio Encoding*

Two factors limited the feasible duty ratios of the four logic signals: the minimum pulse width $t_{PW,min}$, and the impossibility of enabling together the two switches belonging to the same half-bridge (DRV_{PP} and DRV_{PN} cannot be on at the same time, the same holds true for DRV_{NP} and DRV_{NN}).

The minimum pulse width restricted the minimum (D_{min}) and maximum (D_{max}) duty ratios according to the following formula:

$$D_{min} = (1 - D_{max}) = t_{PW,min} \cdot f_{PWE} \tag{4.3}$$

The values resulting from the above formula are real, and need to be casted to the encoded duty domain as follows:

$$\begin{aligned} D_{n,min} &= \lceil div \cdot t_{PW,min} \cdot f_{PWE} \rceil \\ D_{n,max} &= \lfloor div(1 - t_{PW,min} \cdot f_{PWE}) \rfloor \end{aligned} \tag{4.4}$$

Using duty ratios of exactly 0 or 1 was still possible, as it did not violate the minimum pulse width requirement. The consequences of duty limitations were the existence of two *forbidden amplitude zones* which limited the possibility of directly encoding the input sample sequence when its amplitude was too high, or too low.

This is better explained graphically considering a simple, two-level PWE. The plot of Figure 4.10 shows the correspondence between input sample amplitude (x axis), and the encoded duty ratio (y axis). Due to the existence of two forbidden zones (marked in gray), input signals falling in those areas are either masked or saturated. The input range that can be encoded by direct duty quantization is denoted linear dynamic range (LDR).

For what concerns the mutual exclusion of switches belonging to the same half-bridge mentioned above, the constrain simply translated into Equation 4.5.

$$\begin{aligned} D_{n,PP} + D_{n,PN} &\leqslant div \\ D_{n,NP} + D_{n,NN} &\leqslant div \end{aligned} \tag{4.5}$$

Though it may seem that the adoption of two switches from the same half-bridge (and thus generating pulses of opposite polarity) within

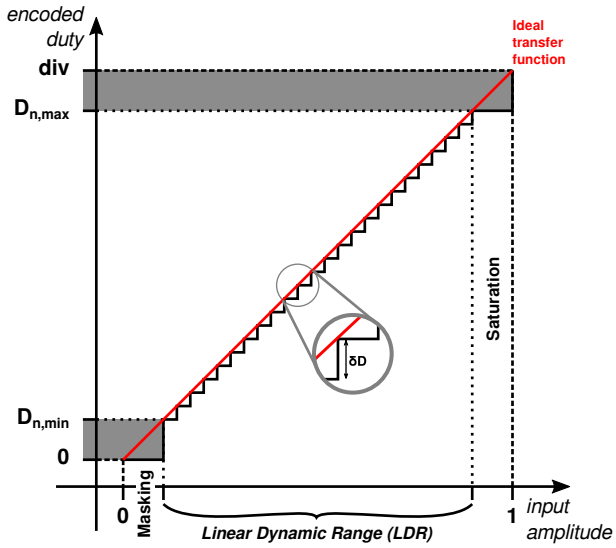


Figure 4.10: Plot showing the effect of pulse width limitations on the dynamic range of a two-level encoder.

the same PWE period should never happen in practice, it will be shown later that this was actually part of normal operation with the final encoding algorithm—and it further limited the overall LDR.

4.3.2.2 *Leading and Trailing Edge Decoding*

Switches belonging to the same half bridge could be used within the same PWE period by simply displacing their activation: as long as the condition of Equation 4.5 was respected, the on-time of one switch could be aligned to the leading edge of the PWE period, and the other aligned with the trailing edge.

This strategy was used in the final FPGA decoder design described in Section 4.3.3.

4.3.2.3 *Handling Multiple Levels*

Since the hardware provided 5 amplitude levels (Table 4.1), the easiest way to encode the input sequence was to split the input dynamic range into 4 amplitude bands and use specific switch combinations

depending on where each sample fell, as shown in Figure 4.11. The input signal needed to be pre-scaled and limited within the ± 2 amplitude range, which corresponded to the maximum, $\pm 2 \cdot \mathrm{HV}$ output voltage span (note that this range did not account for duty ratio limitations: those were enforced by the encoder on its own).

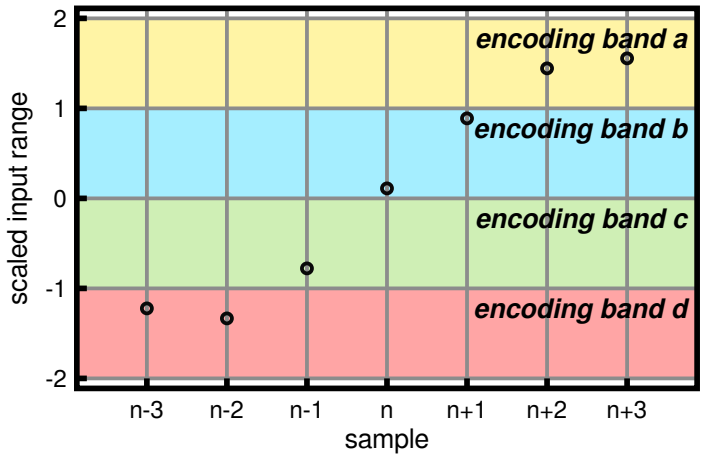


Figure 4.11: Amplitude band splitting of the input sequence used to perform five-level PWE.

4.3.2.4 *Switching Time Constants*

It has been already explained in Section 4.3.1 how the reconstruction filter damping originates from the average behavior of the power stage switches. This peculiarity results in an abrupt change of the circuit time constants whenever any one switch stops (or starts) toggling at f_{PWE}: such a change in the reconstruction filter damping will determine a noticeable transient of the output signal (in the form of a spike).

Whether these transients are acceptable or not strictly depends on the application. However, within the context of this work, it was decided to avoid their occurrence in order to keep the output signal as smooth as possible.

In practice, this meant that *all* the switches had to keep toggling continuously at f_{PWE}, even if that would not be strictly needed to reproduce a specific sample. The pulse width encoder was thus developed to force all of the four encoded duty ratios to remain between $D_{n,min}$ and $D_{n,max}$ at all times, regardless of the input sample sequence.

The consequence of this was an overall compression of the usable LDR, as the power stage switches ended up introducing a baseline of mutually-canceling average contributions to each sample being encoded.

The usable LDR resulting from the continuous toggling of all the switches can be quantified by assuming that two of them are operating at minimum duty ratio (e. g., PN and NP), while the other two operate at maximum duty ratio (e. g., PP and NN). The resulting, integrated output would be:

$$\begin{aligned} V_{n,max} &= HV\frac{D_{n,PP} - D_{n,PN} - D_{n,NP} + D_{n,NN}}{div} = \\ &= HV\frac{D_{n,max} - D_{n,min} - D_{n,min} + D_{n,max}}{div} \\ &= HV\left(2 - 4\frac{D_{n,min}}{div}\right) \end{aligned} \tag{4.6}$$

Since the minimum duty ratio is defined by an absolute time, and thus grows with the carrier frequency, Equation 4.6 shows that the LDR shrinks with increasing f_{PWE}.

4.3.2.5 *Crossing the Boundary Between Bands*

Though the upper saturation of the linear dynamic range was a hard limit that could not be infringed by the proposed encoding technique, the lower limit corresponding to the *masking* region of Figure 4.10 could be easily circumvented.

Intuitively, masking regions should appear across every boundary between the bands shown in Figure 4.11, their amplitude depending on the minimum achievable duty ratio, causing the encoded waveform to experience something similar to a *crossover distortion* when

the input sample sequence happens to transit from one band to the other.

The solution to avoid this potential distortion problem was actually already presented above, when the preservation of switching time constants was considered, and is based on operating switches of opposite polarity together (i. e., use counteracting pulses within one switching period), or alternatively distributing the duty ratio between switches of equal polarity.

The principle behind this encoding approach is better explained graphically, using a simplified example.

With reference to Figure 4.12a, assume that the n-th sample being encoded has a value slightly above 0, but smaller than what could be reproduced by a single pulse of minimum duty ratio. The set of pulse width signals shown on the left diagram represents the direct conversion of the sample in a single pulse, which however happens to fall within the restricted duty region and thus cannot be generated. On the right is shown the proposed alternative: both PP and NP switches are operated close to 0.5 duty ratio, and the reconstructed, output signal results from their difference, that at this point can be smaller than the minimum duty.

Figure 4.12b shows a similar concept applied to the crossover of 1. In this case the sample to be encoded has a value slightly larger than 1. Direct conversion would result, for instance, in one switch being operated at fully duty ratio (always on), and the other being operated with a duty smaller than $D_{n,min}$. The proposed alternative is, again, to operate the two switches with close to 0.5 duty ratio.

4.3.2.6 *Putting It All Together*

The final PWE algorithm needed to take into account all the points raised above: every switch was to be kept toggling at f_{PWE} to preserve the time constants, and some way to avoid crossover distortion had to be implemented.

Considering for now only the positive half of the input dynamic range, the encoder always enforced a duty ratio greater or equal than $D_{n,min}$ on all the four output words. Band splitting was adjusted to ac-

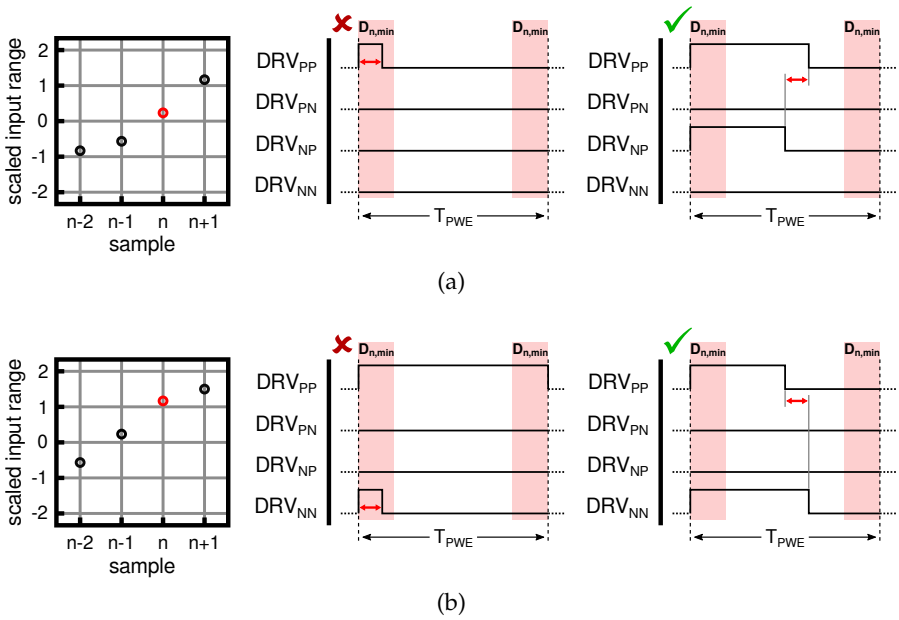


Figure 4.12: Example of how PWE avoids crossover distortion: (a) level 0 crossover; (b) level 1 crossover.

count for this baseline duty, and resulted in the two crossover points of 0 and $(1 - 2D_{n,min}/div)$.

Within each one of these amplitude bands, two different encoding criteria were used. If S_n is the amplitude of the input sample being processed, when $S_n \leqslant (1 - 2D_{n,min}/div)$ the encoder adopted the conversion shown in 4.7.

$$\begin{aligned} D_{n,PP} &= D_{n,min} \\ D_{n,PN} &= D_{n,min} \\ D_{n,NP} &= D_{n,min} \\ D_{n,NN} &= \text{round}(S_n \cdot div) + D_{n,min} \end{aligned} \tag{4.7}$$

When $(1 - 2D_{n,min}/div) < S_n \leqslant (2 - 4D_{n,min}/div)$, 4.8 was used instead.

$$\begin{aligned} D_{n,PP} &= \text{round}\left\{\left[S_n - \left(1 - 2\frac{D_{n,min}}{div}\right)\right] div\right\} + D_{n,min} \\ D_{n,PN} &= D_{n,min} \\ D_{n,NP} &= D_{n,min} \\ D_{n,NN} &= div - D_{n,min} \end{aligned} \tag{4.8}$$

Covering the negative half of the dynamic range, from 0 to -2, was done by exploiting the symmetry of the power stage. It was sufficient to swap the encoded words between $D_{n,PP} \rightleftharpoons D_{n,NP}$, and between $D_{n,PN} \rightleftharpoons D_{n,NN}$, to reverse the polarity of the reconstructed output.

Finally, it should be noted that a way to encode signals $> (2 - 4D_{n,min}/div)$ was also included in the source code, which worked by allowing some switches to be completely turned on or off, thus violating some of the constraints. This high-range encoding profile was never used during the preliminary tests reported at the end of Section 4.3.3, as it caused the appearance of transients in the reconstructed output waveform due to the abrupt change in time constants. It is however present in the encoder source.

The MATLAB script written to encode an arbitrary waveform in a five-level data stream is printed in Appendix C.

4.3.2.7 *Encoder Code Structure*

The pulse-width encoder script requires the following input data to execute:

- A text file containing the sequence of samples to encode.
- The sample rate of such data, corresponding to f_{PWE}.
- The system clock of the decoder, f_{SYSCLK}.
- The minimum pulse width of the pulser, $t_{PW,min}$.
- Pre-processing gain and offset, which are applied to every value read from the input file before encoding.

- The file name used to store the encoded output.

The sample rate must be an even integer divisor of f_{SYSCLK}. Moreover, the encoder code enforces an input dynamic range of $[+2; -2]$ to every sample, after the pre-processing gain and offset have been applied: values beyond those limits are automatically clamped. The script also calculates the duty ratio limitations of the hardware, which are later used to determine the encoder amplitude band-splitting thresholds.

The input sample sequence is processed iteratively following the flow chart reported in Figure 4.13. When the encoding is done, a graphical representation of the results is shown for the user's convenience. The data are then stored in the output file using a format compatible with the hardware decoder described in Section 4.3.3.

4.3.2.8 *A Waveform Encoding Example*

Figure 4.14 shows the actual results of encoding a single cycle of sine wave at 100 kHz. The input sample sequence is plotted in Figure 4.14a; zero-padding was added at the beginning and at the end to highlight how the encoder handles a 0 signal.

The parameters used to configure the encoder corresponded to realistic, hardware-compatible values: system clock $f_{SYSCLK} = 100$ MHz and carrier frequency $f_{PWE} = 5$ MHz, resulting in a PWE divisor $div = 20$. The minimum pulse width was set at $t_{PW,min} = 20$ ns, and thus the minimum encoded duty was $D_{n,min} = 2$.

The amplitude of the sine wave was chosen to cover the full LDR determined by the timing parameters, that is ± 1.6.

Figure 4.14b is a plot of the four streams encoded by the script. The vertical axis goes from 0 to the maximum div, which in this context corresponds to unity duty ratio. The information about waveform polarity is lost in the plot, as it is determined by how the decoded stream is fed to the pulser power stage.

The leading and trailing sections of the encoded outputs show that in the presence of a 0 input the duty ratio of all the switches collapses to $D_{n,min}$, rather than zero, so that the reconstructed output averages to 0 while maintaining the power stage in a switching state that preserves the time constants.

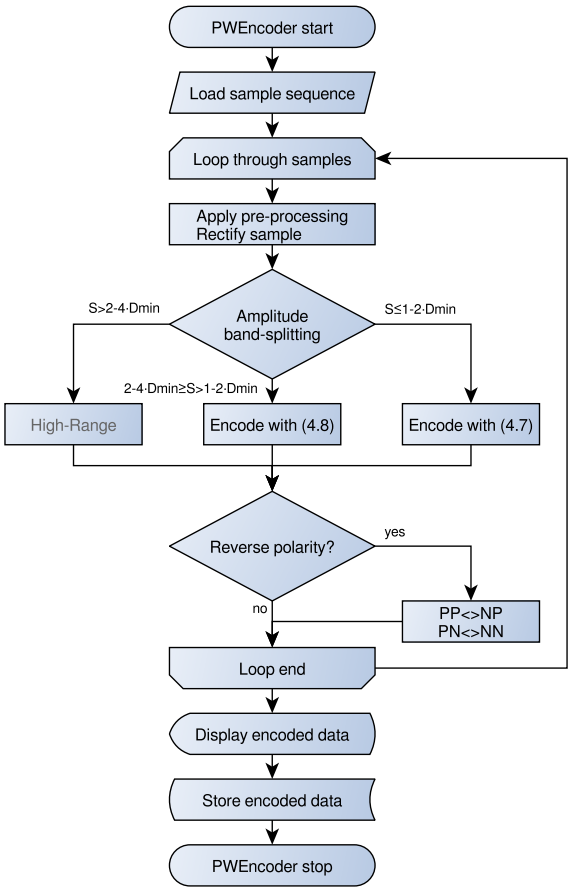
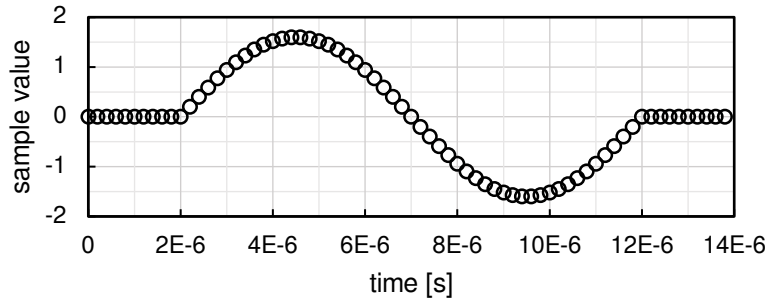
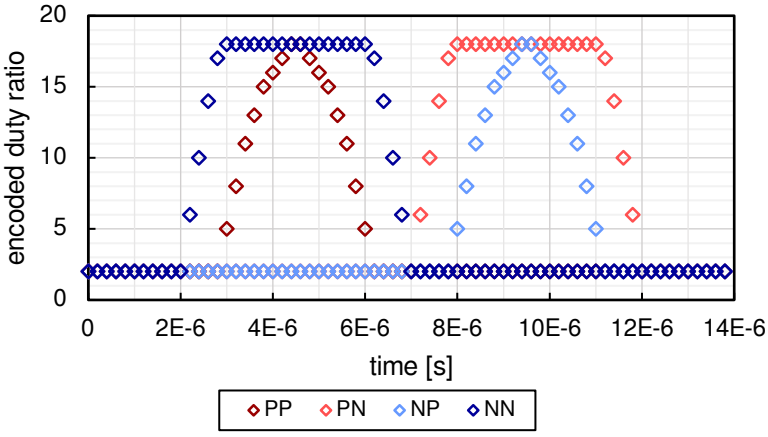


Figure 4.13: Flow chart of the pulse-width encoder code.



(a)



(b)

Figure 4.14: Example pulse-width encoding: (a) input sample sequence (one cycle of sine wave at 100 kHz); (b) the four encoded duty ratio streams.

4.3.3 *All-Digital Waveform Generation*

The transducer driver module connected directly to the FPGA, an Intel FPGA Arria V ST SoC 5ASTFD5K3F40I3N, through a parallel, 32-bit LVCMOS-25 bus. With $2 + 2$ bits per channel, the FPGA logic fully controlled each one of the possible states of the ultrasound pulser power stage (+HV, -HV, active clamp, and Hi-Z per side). Although the HDL6V5583 also provides registered digital inputs, the current design uses the device in *transparent latch mode*, with logic-level synchronization ensured at the source.

A proof-of-concept, FPGA core was developed to decode the PWE data generated with the method described in Section 4.3.2, and output the pulse-width modulated signals needed to operate all the 8 ultrasound driver channels, providing inter-channel synchronization and fixed-latency. The Verilog source code of this core, called `AWPulser8Decoder`, can be found in Appendix D.

The `AWPulser8Decoder` core allows the reproduction of eight pulse-width modulated signals with up to 512 samples per channel and 8-bit duty resolution (256 duty ratio steps per sample). The decoder supports both burst mode, repeating the stored waveform sequentially a fixed number of times (up to 255), and continuous wave (CW), continuously repeating the waveform until a stop command is received.

The decoder clock, which sets the absolute minimum pulse width step, is currently tied to the system clock ($f_{SYSCLK} = 100$ MHz), even though the Arria V SoC FPGA fabric can handle clock rates up to 650 MHz. Plans have been made to integrate a reconfigurable PLL in the design and provide run-time adjustment of the decoder clock.

High-resolution pulse width generation techniques going beyond the system clock rate by using an asynchronous, tapped-delay line approach have been proposed in the literature [143]. They were, however, not considered for this design.

The decoder core is interfaced to the FPGA embedded controller as an Avalon slave, through the system Avalon memory-mapped (MM)

interface, providing register-based control and configuration as reported at the beginning of Appendix D.

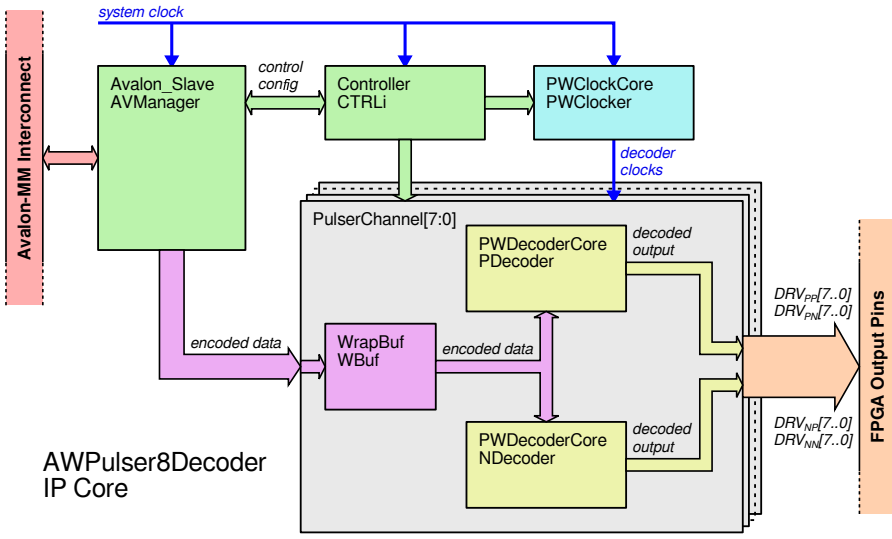


Figure 4.15: Hierarchical block scheme of the `AWPulser8Decoder` FPGA core.

The structure and operation of `AWPulser8Decoder` can be explained with reference to Figure 4.15. The encoded data for each channel is transferred via Avalon bus from the embedded controller into a set of local buffers (WrapBuf), having a 32-bit word size and thus packing together four encoded samples per word (each sample defines one logic output—PP, PN, NP, NN).

During decoding, the buffers are swept slowly, with an appropriately divided clock rate, to retrieve the samples to decode, while a counter operating at full clock rate is used to transform the encoded samples in pulse-width modulated logic signals. Start and stop commands are issued from the embedded controller using a bus triggering command through the Avalon-MM interface (no dedicated triggering signals are included in the design).

4.3.4 *Characterization of the Waveform Generator*

The ultrasound driver module was designed to be part of a larger system and therefore lacked the ability to operate standalone: connecting to the transducers, generating the required power rails, interfacing with a computer to emit signals, are all tasks that could not be performed without external electronics.

Testing the module performance thus required additional hardware. While the digital domain was handled by the Arria V SoC development board, the analog part required the design of a custom board that could provide the ±5 V and ±48 V power rails, and bring out the analog signals with easy-to-use connectors and accessible test-points. A picture of this test card is shown in Figure 4.16.

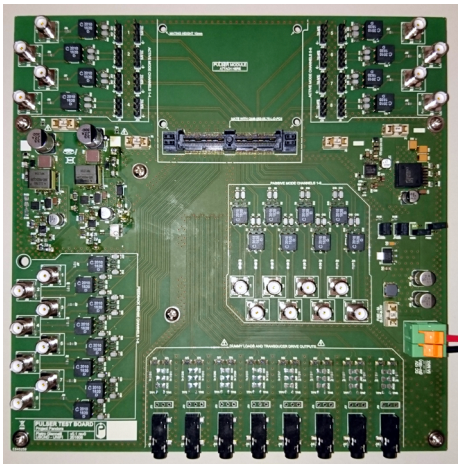


Figure 4.16: Picture of the ultrasound driver module analog test board. Board size is 180×180 mm.

The following sections report the results of several tests performed to assess the characteristics of the proposed ultrasound driver module used as an arbitrary waveform generator. The results represent the combined performance of both hardware and software, including the pulse-width encoding algorithm.

A number of operating parameters were selected, or fixed by the intrinsic limitations of the hardware, and apply to all the measure-

ments presented below (unless otherwise noted). These include: the system clock of the FPGA decoder ($f_{SYSCLK} = 100$ MHz), the minimum pulse width imposed by the HDL6V5583 ($t_{PW,min} = 20$ ns), the pulser high-voltage supply (± 48 V). The carrier frequency used during most of the tests was $f_{PWE} = 5$ MHz which, combined with the other parameters, set the duty ratio divisor $div = 20$ and determined an LDR of $\pm 1.6 \cdot HV$ (calculated according to Equation 4.6). The minimum quantized duty ratio was $D_{n,min} = 2$, or 10%.

Given the set of parameters above, one can calculate the overall amplitude quantization of the driver by noticing that, for each polarity, a total of $2div - 2D_{n,min} = 32$ steps are available. This means that a total of 64 quantization steps are used to cover the $\pm 1.6 \cdot HV$ full-scale output (i. e., 6 bits), resulting in a $LSB = 3.2 \cdot HV/2^6 = 50 \times 10^{-3} \cdot HV = 2.4$ V.

4.3.4.1 *Step Response*

The step response of the ultrasound driver module was tested with two signals chosen to cover the excursion over one or two amplitude bands of the encoding algorithm. As explained in Section 4.3.2.6, the encoder used two different methods to encode the input samples belonging to the $[0; (1 - 2D_{n,min}/div)]$ band (low-range), and $((1 - 2D_{n,min}/div); (2 - 4D_{n,min}/div)]$ band (mid-range), which also applied to the negative half of the dynamic range.

Considering the specified system parameters, the low-range and mid-range full-scale outputs corresponded to the input values of 0.8 and 1.6. The two step function were thus designed as abrupt transitions from 0 to 0.8, and from 0 to 1.6. Those signals corresponded to, respectively, a 0 V to 38.4 V step, and a 0 V to 76.8 V step at the load.

The encoded step signals were reproduced on a 100 pF load, and the differential outputs measured across the load are reported in Figure 4.17 and Figure 4.18. Neglecting the propagation delays between the logic inputs of the pulser to the module outputs, the plots show that the settling time in both cases corresponds to ~ 4 PWE periods even though, given the large residual carrier ripple, it is difficult to define a settling boundary.

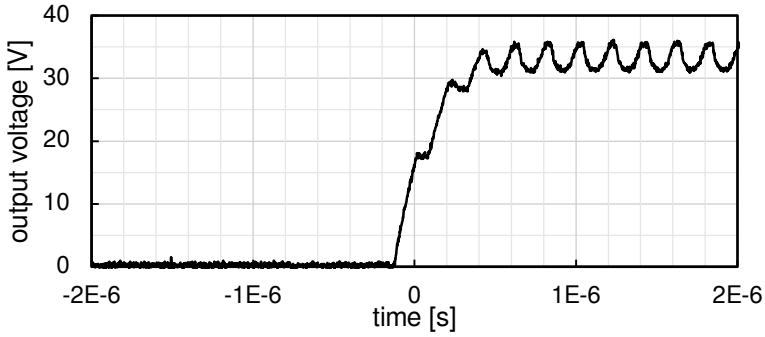


Figure 4.17: Low-range step response, 0 to $0.8 \cdot$ HV transition, 5 MHz carrier.

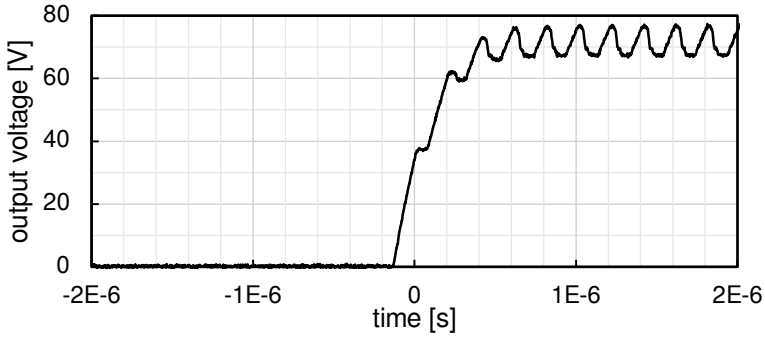


Figure 4.18: Mid-range step response, 0 to $1.6 \cdot$ HV transition, 5 MHz carrier.

It should be noted that the step response is primarily determined by the reconstruction filters, and thus by their damping. As explained in Section 4.3.1.1, the filter Q factor of the proposed ultrasound driver depended on the switch-mode operation of the power stage, and changed with the duty ratio. Specifically, the Q factor was lower for higher duty ratios of the active dampers, which ultimately meant that the reconstruction filters Q increased when generating increasingly large outputs. This peculiar behavior is evident in Figures 4.17 and 4.18: before the step, when the output voltage is 0, no significant carrier ripple can be appreciated, despite the fact that the pulsers are switching at constant f_{PWE}; afterwards, when the output voltage has reached its settling level, the ripple has a significant amplitude.

4.3.4.2 *Conversion Linearity*

The digital-to-analog transfer characteristic of the ultrasound driver was measured by generating a staircase signal with LSB vertical step size, sweeping all the available quantization steps. Each step was made 7 PWE periods long to allow the output to settle.

The resulting output, driving a 100 pF load, is plotted in Figure 4.19 together with the ideal staircase output.

Figure 4.19 highlights a few interesting properties of the transfer characteristic. First of all, despite the conversion being monotonic, the cross-over regions between low-range and mid-range encoding display an abrupt change of gain that lasts for a few codes, where the output almost flattens. Also, the gain of the remaining segments is visibly higher then what was expected, and there is a distinct offset. These phenomena could probably be corrected by adjusting the encoding algorithm.

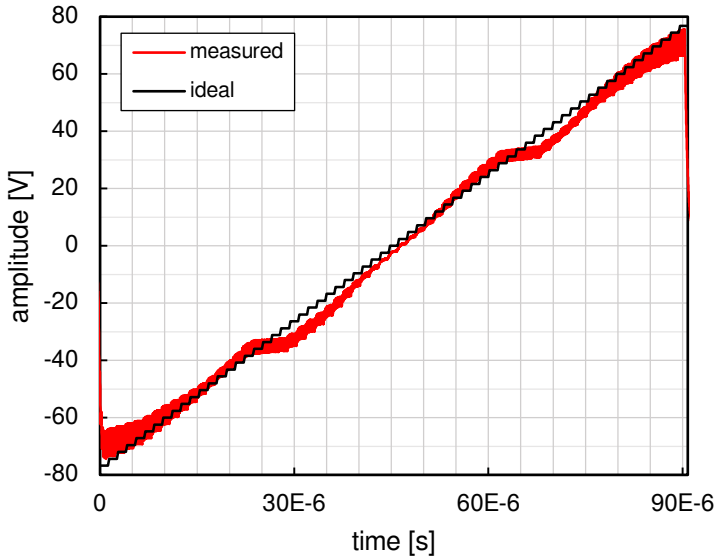


Figure 4.19: Full-scale staircase output ($\pm 1.6 \cdot HV$) with LSB step size overlapped to the ideal transfer characteristic, 5 MHz carrier.

4.3.4.3 *Distortion and Noise*

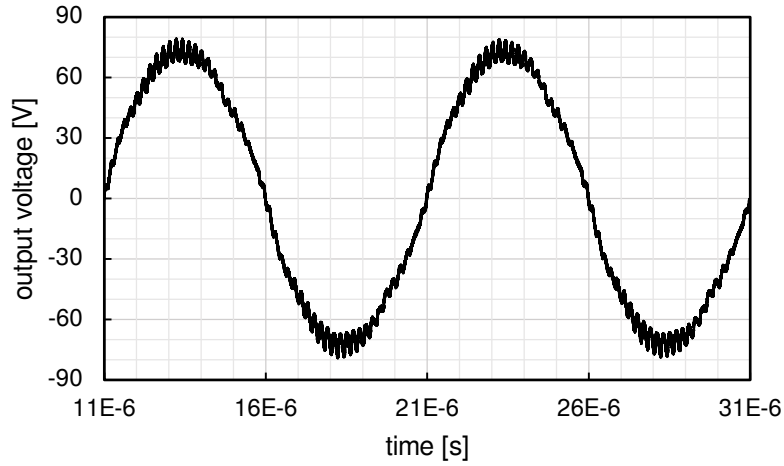
Even though the aim of the driver module is arbitrary waveform generation, initial testing was performed with sine wave signals at different frequencies. This choice allowed the evaluation of output spectral content and modulation effects with narrow-band signals.

Since the driver module cannot yet operate in continuous wave due to the limitations exposed in Section 4.3.1.2, a trick was adopted to emulate a sine wave from a tone burst transmission signal. The tone burst outputs were acquired with an oscilloscope and an integral number of periods was precisely trimmed at their nodes with a rectangular window. The trimmed waveforms were then Fourier transformed without adding further padding, and thus acted as if the signals were continuous in time. Using this approach, the resulting spectra clearly showed the baseband signal peaks and their harmonics, along with the carrier.

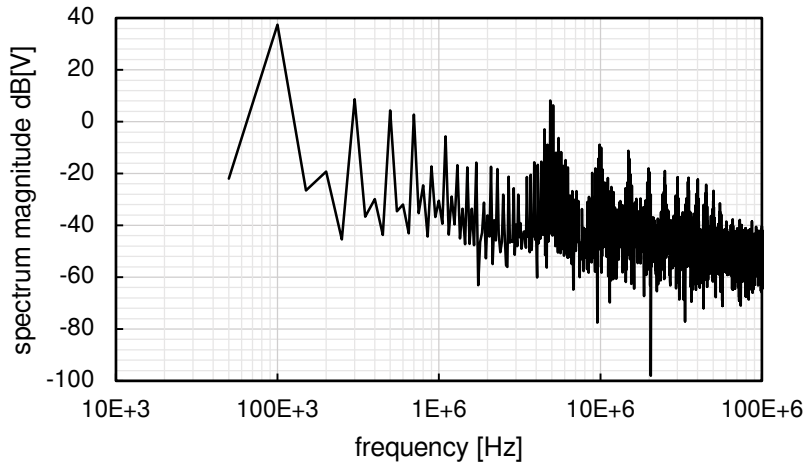
The testing frequencies f_0, chosen to cover the 100 kHz–1 MHz decade, were: 100 kHz, 150 kHz, 220 kHz, 330 kHz, 470 kHz, 680 kHz, and 1 MHz. The amplitude of the transmitted tone burst signals was scaled to the maximum LDR permitted by the system: $\pm 1.6 \cdot \mathrm{HV}$.

Windowing of the acquired traces was done by including an increasing number of sine wave periods as f_0 grew, to keep a reasonably sharp frequency resolution in the resulting FFT spectra. Two periods were windowed at $f_0 = 100$ kHz, up to 11 periods at 1 MHz.

The results are plotted in Figure 4.20 through Figure 4.26. The same operating conditions maintained throughout these tests: power stage supply rails of ± 48 V and 100 pF load.

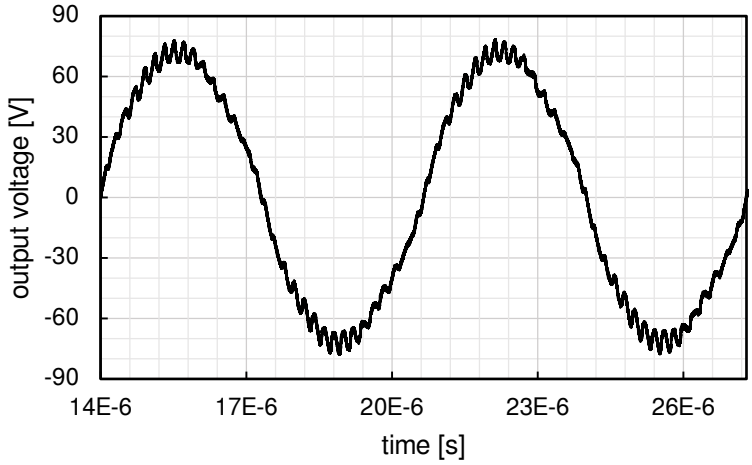


(a)

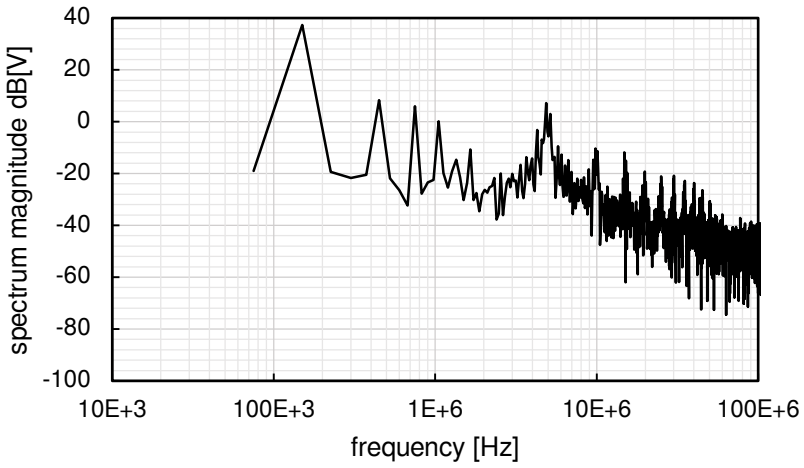


(b)

Figure 4.20: Tone burst driver test output at 100 kHz: (a) windowed waveform; (b) FFT spectrum.

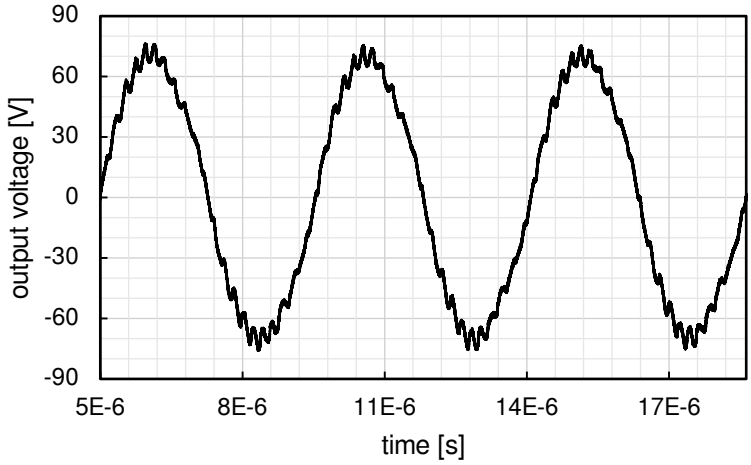


(a)

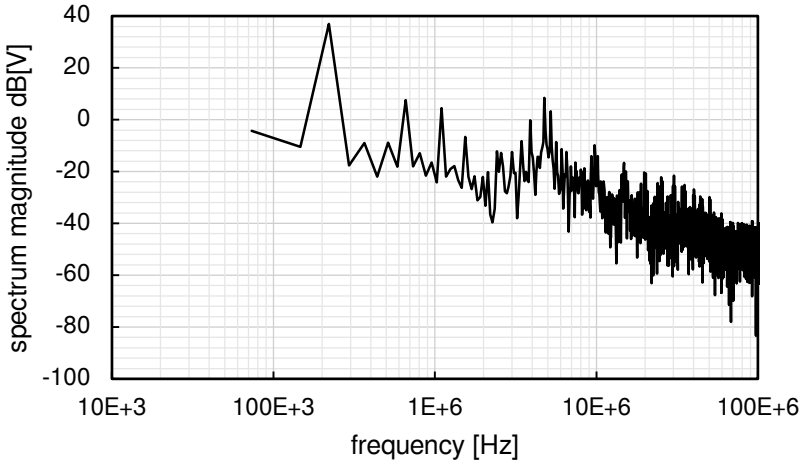


(b)

Figure 4.21: Tone burst driver test output at 150 kHz: (a) windowed waveform; (b) FFT spectrum.

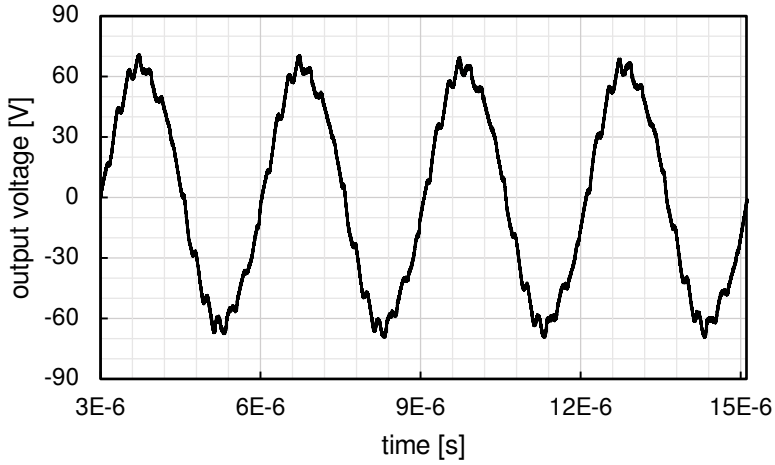


(a)

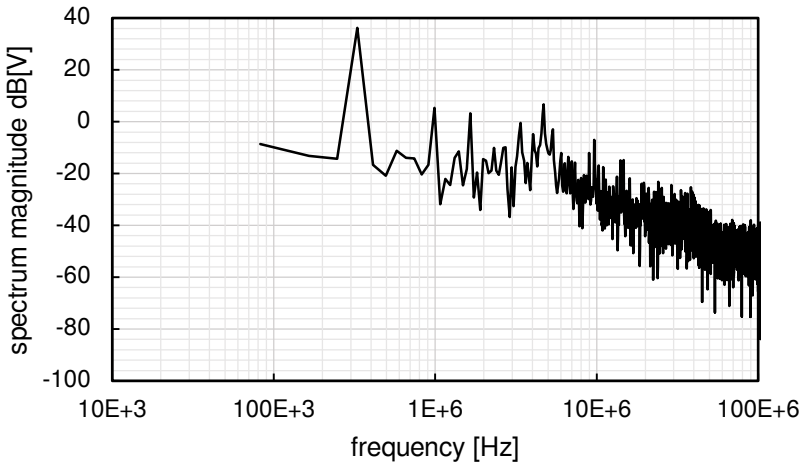


(b)

Figure 4.22: Tone burst driver test output at 220 kHz: (a) windowed waveform; (b) FFT spectrum.

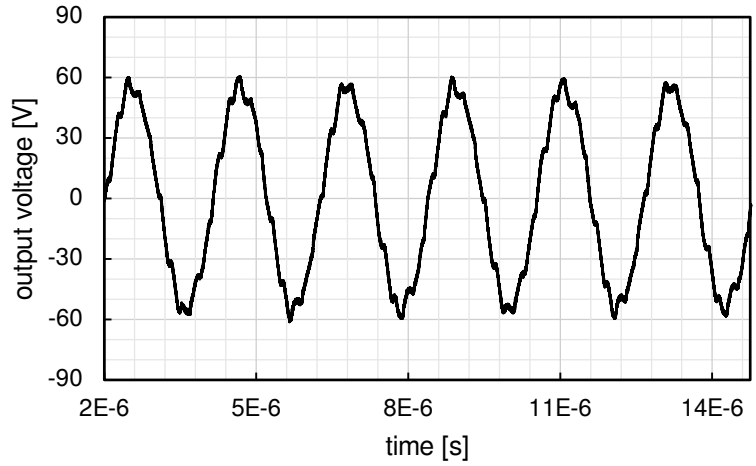


(a)

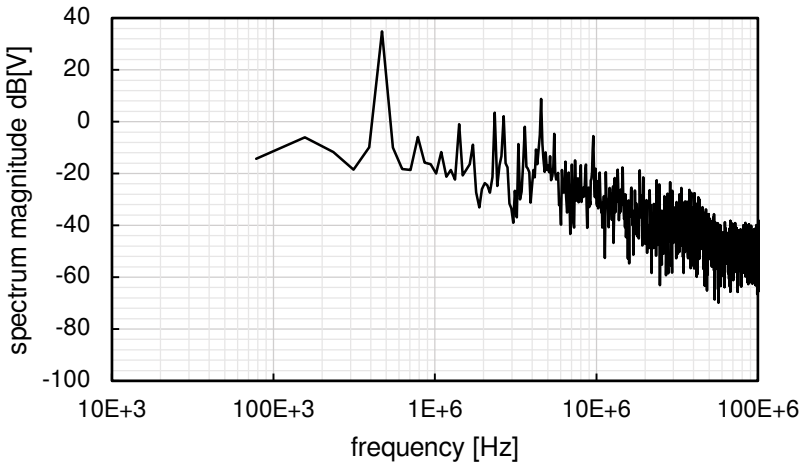


(b)

Figure 4.23: Tone burst driver test output at 330 kHz: (a) windowed waveform; (b) FFT spectrum.

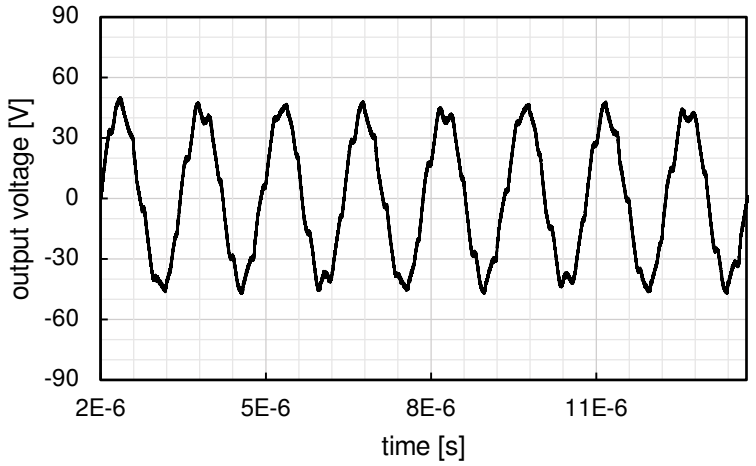


(a)

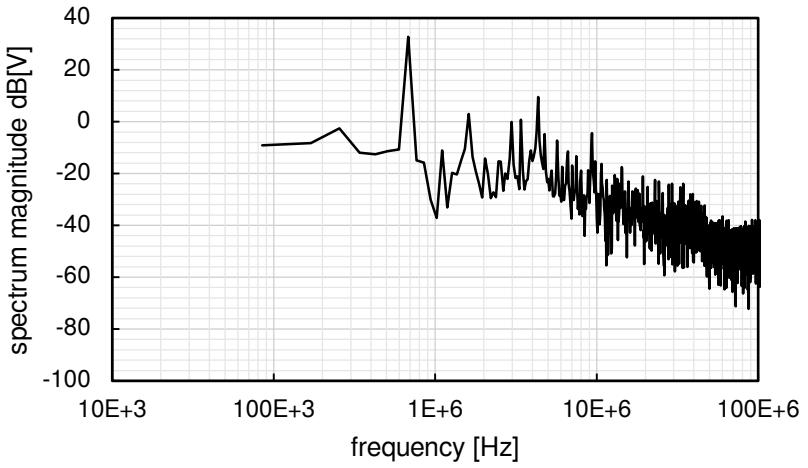


(b)

Figure 4.24: Tone burst driver test output at 470 kHz: (a) windowed waveform; (b) FFT spectrum.

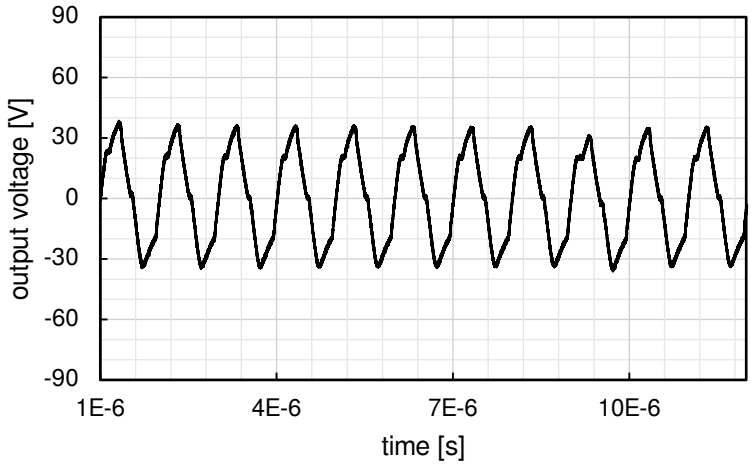


(a)

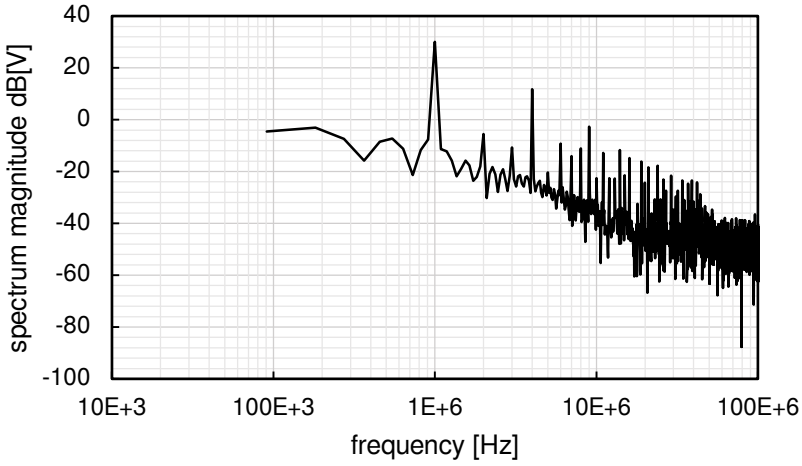


(b)

Figure 4.25: Tone burst driver test output at 680 kHz: (a) windowed waveform; (b) FFT spectrum.



(a)



(b)

Figure 4.26: Tone burst driver test output at 1 MHz: (a) windowed waveform; (b) FFT spectrum.

The waveform plots clearly show an amplitude reduction with increasing tone burst frequency f_0, even though all the signals were encoded with the same peak amplitude and carrier frequency. A plot highlighting this behavior is shown in Figure 4.27.

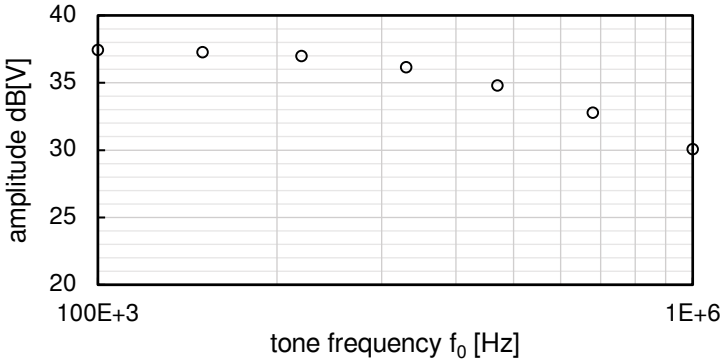


Figure 4.27: Amplitude of the fundamental output of tone burst tests in the 100 kHz–1 MHz range.

Quantifying the *quality* of the generated waveforms is not straightforward, as the spectra show many peaks: some related to the baseband tone, the residual carrier, and some carrier intermodulation sidelobes.

A criterion to evaluate the signals was chosen by combining the total harmonic distortion of the baseband signal, including contributions up to the 10^{th} harmonic whenever possible, with the amplitude of the carrier at f_{PWE}: this quantity was named THD+C and has the expression shown in Equation 4.9, where V_1 is the amplitude of the tone burst fundamental, V_n are the harmonics, and V_C the carrier.

$$\text{THD+C} = \frac{\sqrt{\sum_{n=2}^{k} V_{n,\text{RMS}}^2 + V_{C,\text{RMS}}^2}}{V_{1,\text{RMS}}^2} \tag{4.9}$$

The THD+C was calculated for all the tone bursts acquired, and the resulting values are plotted in Figure 4.28.

The SINAD (Signal-to-noise and distortion ratio) could also be evaluated from the data acquired above, applying the dispositions included in the IEEE 1658 standard [144].

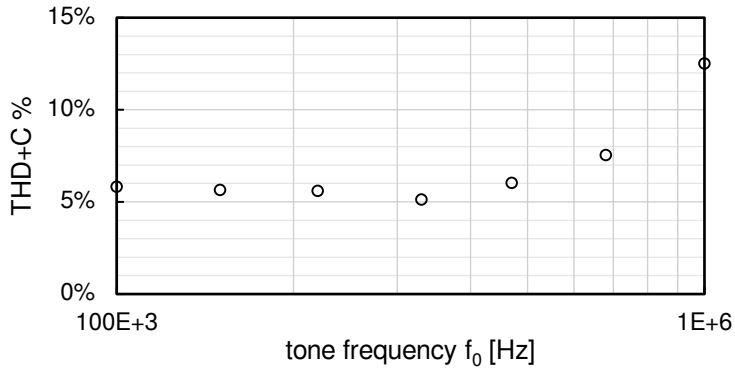


Figure 4.28: THD+C of the tone bursts generated with 5 MHz carrier.

The standard method for calculating the SINAD in the frequency domain involves processing the FFT spectra of integral-cycle tone waveforms generated by the device under test. This process is repeated for different tone frequencies output at full-scale amplitude.

Equation 4.10 is used to calculate the SINAD starting from the FFT of an acquired trace, where the $V_{0,RMS}$ term represents the RMS amplitude of the fundamental, while the NAD term at the denominator is expanded in Equation 4.11.

$$\text{SINAD} = \frac{V_{0,\text{RMS}}}{\text{NAD}} \tag{4.10}$$

The NAD is calculated by considering the remaining spectral components after removing the DC and the contributions at f_0, and thus represents the RMS of noise and unwanted signals (including the harmonics, the residual modulation carrier, and the intermodulation products). For all the measurements hereby presented, the energy contributions of the fundamental were always restricted to a single FFT bin, resulting in a total of 3 points being removed from the NAD calculation (i. e., the DC term, and both positive and negative components at f_0).

$$\text{NAD} = \frac{1}{\sqrt{N\,(N-3)}} \sqrt{\sum_{n \in B_{\text{NAD}}} S\,[n]^2} \tag{4.11}$$

In Equation 4.11, $S[n]$ is the FFT magnitude, which in the original SINAD definition is replaced by a spectral average but here represents the spectrum of a single waveform (the difference between the two is negligible), N is the number of points of the FFT, and B_{NAD} is the set of all integers between 1 and $N-1$, excluding the two indexes corresponding to the fundamental bins ($S[0]$ corresponds to the DC component, and thus also excluded).

The SINAD calculated from the tone burst tests executed in the 100 kHz–1 MHz range with $f_{PWE} = 5$ MHz is reported in Figure 4.29.

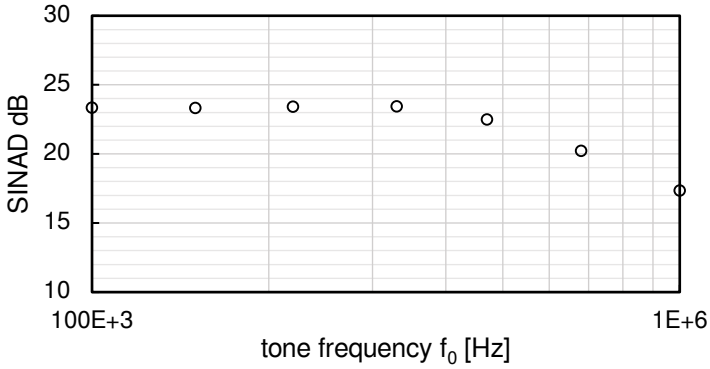


Figure 4.29: Signal-to-noise and distortion ratio of the ultrasound driver operating with a 5 MHz carrier.

The effective number of bits (ENOB) is directly related to the full-scale SINAD (expressed in dB) through Equation 4.12.

$$\mathrm{ENOB} = \frac{\mathrm{SINAD}_{\mathrm{dB}}}{20} \log_2 10 - \frac{\log_2 1.5}{2} \tag{4.12}$$

The ENOB of the ultrasound driver operating with $f_{PWE} = 5$ MHz is plotted in Figure 4.30.

A waveform generation test was also done with a tone burst at $f_0 = 470$ kHz, but doubled carrier frequency ($f_{PWE} = 10$ MHz). In this case the duty ratio stepping was reduced to $div = 10$, resulting in a smaller amplitude LDR of $\pm 1.2 \cdot HV$. The result is shown in Figure 4.31.

Trading duty ratio quantization for increased sample rate resulted in a smoother-looking sine wave, and also pushed the carrier at a fre-

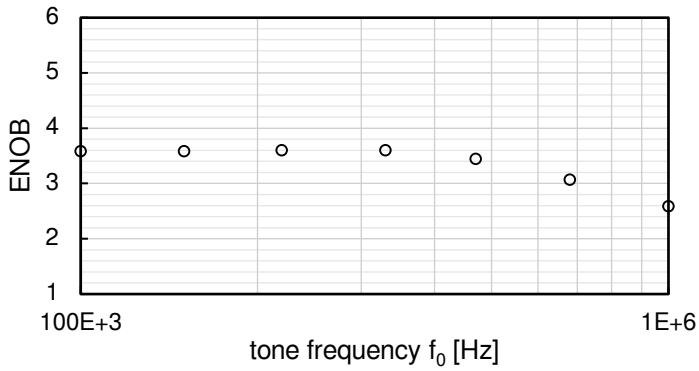


Figure 4.30: Effective number of bits of the ultrasound driver operating with a 5 MHz carrier.

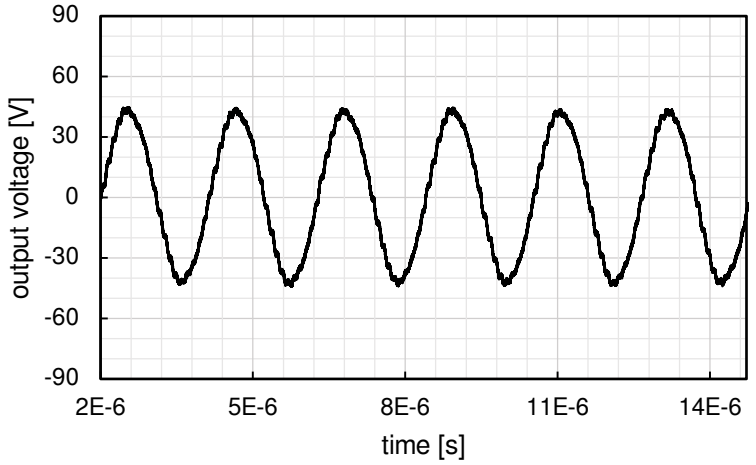
quency where the reconstruction filters provided better rejection. The increase in signal quality was confirmed by calculating the SINAD in these conditions, which resulted in a value of 26.8 dB, 4.4 dB higher than the corresponding SINAD obtained with $f_{PWE} = 5$ MHz.

However, the drawbacks of increasing f_{PWE} included a smaller LDR and increased power consumption (pulser switching losses are directly proportional to the carrier frequency).

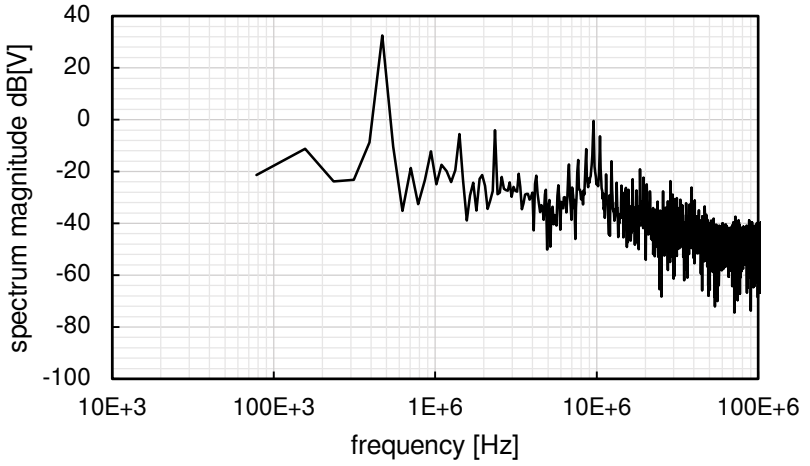
4.3.5 *Output Feedback*

The transducer-driving output lanes (after the reconstruction filters) were fitted with feedback amplifiers to collect scaled-down ($\sim 1:100$) replicas of their signals, and individually route them to dedicated input channels of the ADC. These feedback paths will eventually allow the system to sense the high-voltage signals as they are being applied to the transducers.

Though no functionality has yet been implemented, the envisaged purposes of the feedback path include output correction and providing a reference transmitted signal to be used further down the line, while processing the data collected by the reception chain.



(a)



(b)

Figure 4.31: Tone burst driver test output at 470 kHz: (a) windowed waveform; (b) FFT spectrum.

4.3.6 *Passive-Mode Receiver*

Previous experience with the system described in Chapter 3 suggested that specific, low-gain signal conditioning channels were required to perform passive-mode impact and vibration detection.

Those channels were designed similarly to the output feedback described above (using banks of Texas Instruments THS4524 fully differential amplifiers), but provided an attenuation of $\sim 1:5$.

4.3.7 *T/R Switching*

Transmit / receive switching is handled by two dedicated multichannel chips (Texas Instruments TX810) that contain a bank of diode bridges with programmable biasing. Together with the pulser chips, these are the only devices of the entire analog signal chain that require split ± 5 V supplies.

The specified bandwidth of the TX810 is much wider than what is required by the proposed design, even at the lowest bias setting (65 MHz).

4.4 RECEIVING SIGNALS

Guided-wave ultrasound propagated over complex media like CFRP plates and shells incur in significant attenuation [145] which, combined with the poor sensitivity of piezopolymer film transducers discussed in Chapter 2, makes the task of receiving these signals particularly arduous: very large gain is generally required from the preamplifiers, and low-noise.

Furthermore, practical considerations regarding the target operational environment of SHM systems (e. g., ground vehicles, aircrafts, rotating machinery) suggest the presence of significant EMI, pushing in the direction of adopting fully-differential signal conditioning circuitry.

Broadband piezoploymer transducers tend to present a large capacitive impedance within the bandwidth of interest for the proposed

system (100 kHz–1 MHz), in the kilohm range, that needs to be taken into account when designing the signal conditioning electronics.

As the active area of piezopolymer transducer shrinks (like those presented in Section 2.5 and Section 2.7), maintaining the same film thickness results in an inevitable increase of the source impedance, to the point where signal extraction strategies should be reconsidered.

The topic of transducer interfacing will be explored below with explicit reference to the IDTs presented earlier in the text, but the conclusions are generally applicable to every kind of piezoelectric sensor.

4.4.1 *Voltage-Mode and Charge-Mode Interfacing*

Considering a single piezoelectric sensor with two electrodes, there are two complementary ways of detecting the charge generated by direct piezoelectric effect, that essentially depend on the way the sensor is electrically loaded.

- When the sensor is left open-circuit, a voltage can be detected at its electrodes when excess charge is generated. In reality, any *voltage-mode* sense circuit will have a finite input impedance.
- If the sensor electrodes are deliberately shorted, on the other hand, the excess charge can be detected as a current flowing through the short. Of course, actual *charge-mode* circuits have a non-zero input impedance.

When dealing with IDTs, different sensing modes benefit from different connection of the electrodes. This is easily explained referring to Figure 4.32.

In Figure 4.32a, all the electrodes on the bottom side of the IDT are shorted together and used as a ground plane of sorts, resulting in half the fingers being in series with the other half and, since the signals are supposed to be equal in magnitude but opposite in phase, the resulting open-circuit voltage developed between the [+] and [-] terminals is two times that generated by a single finger. A voltage-

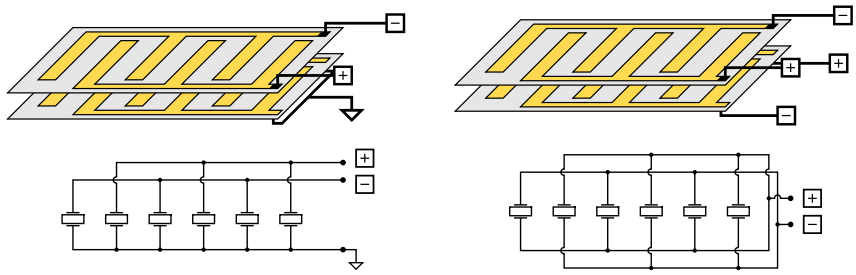


Figure 4.32: IDT preferred connection strategies for sensor interfacing: (a) voltage-mode; (b) charge-mode.

mode amplifier with sufficiently high input impedance works well with this configuration.

Consider instead the configuration of Figure 4.32b, where the fingers are connected in antiparallel. In this case all the charge separated at each electrode pair will build up on a single equivalent capacitance: as there is no stacking of fingers, the total open-circuit voltage at terminals [+] and [-] will be the same as that of a single finger. This configuration, however, allows the complete extraction of the charge generated by the IDT, and is thus best suited for interfacing with a charge-mode amplifier.

The advantage of using one solution over the other depends on the intended application and sensor characteristics. For instance, a sensor displaying a rather large stray (non piezo-active) capacitance might benefit from charge-mode interfacing. An interesting example reported in the literature regards the interfacing of PVDF-based PWAS, where the authors resorted to using a charge amplifier to boost the received signal [146].

The analog front-end developed as part of the Pandora testbench system (described in Section 4.4.6) integrated both sensing method, providing swappable voltage-mode (instrumentation amplifier) and charge-mode pre-amplifiers.

4.4.2 *The Fully-Differential Charge Amplifier*

The fully-differential charge amplifier was developed as a natural extension of the well-known differential-input charge amplifier shown in Figure 4.33. An inverting unity-gain buffer was added to close a secondary feedback loop, obtaining the differential-input, differential-output topology shown in Figure 4.34.

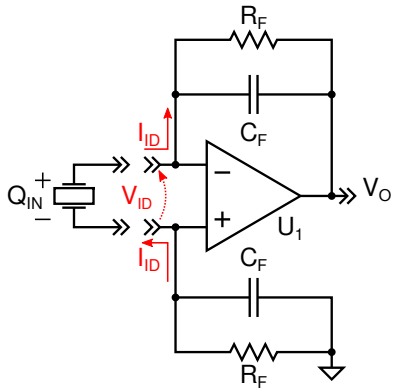


Figure 4.33: Differential-input charge amplifier schematic.

The mid-band charge conversion gain of the two amplifier topologies can be found through simple circuit analysis, and has in both cases the expression reported in Equation 4.13.

$$|A_{DM}| = \left|\frac{V_O}{V_{ID}}\right| = \left|\frac{V_{OD}}{V_{ID}}\right| = \frac{2}{C_F} \tag{4.13}$$

What changes significantly between the two topologies is the differential input impedance presented to the source, when the same feedback impedance is used ($Z_F = R_F \parallel C_F$).

The differential input impedance of the charge amplifier of Figure 4.33 can be calculated using Equation 4.14, where A_{OL} is the open-loop gain of the operational amplifier U_1.

$$Z_{IN} = \frac{V_{ID}}{I_{ID}} = \frac{2 \cdot Z_F}{1 + A_{OL}} \tag{4.14}$$

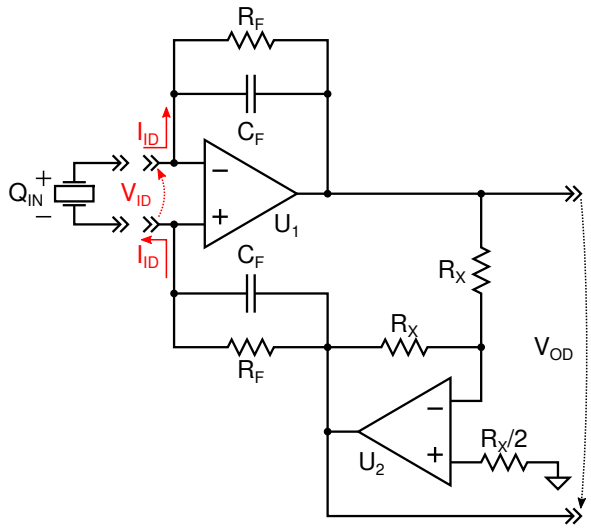


Figure 4.34: Fully-differential charge amplifier schematic.

The input impedance of the fully-differential variant of Figure 4.34, on the other hand, has the expression shown in Equation 4.15. Therefore, as long as the open-loop gain of the operational amplifier U_1 does not start to roll-off, the input impedance magnitude of the fully-differential charge-amplifier will be practically half that of its parent circuit.

$$Z_{IN} = \frac{V_{ID}}{I_{ID}} = \frac{2 \cdot Z_F}{1 + 2 \cdot A_{OL}} \tag{4.15}$$

This advantage is particularly important when interfacing piezoelectric sensors in the presence of parasitic loading (e. g., due to the cable's stray capacitance): a lower impedance path, the charge amplifier itself, will collect and amplify most of the charge generated.

4.4.2.1 *Equivalence Between Charge and Voltage Gain*

An equivalence can be established between the charge-to-voltage conversion gain, and the regular voltage gain of capacitive sources. Although based on idealized conditions, this equivalence can be useful to compare amplifiers of different nature.

Knowing the source capacitance C_{SRC} [F] and the conversion gain A_{DM} [V/C] of the charge amplifier, the voltage gain required by a voltage-mode amplifier with infinite input impedance to get the same output signal amplitude would be:

$$A_{V,eq} = A_{DM} \cdot C_{SRC} \tag{4.16}$$

Incidentally, the equation above also represents the gain experienced by the equivalent input voltage noise of the main op-amp in the charge amplifier topology (U_1 in Figure 4.34).

4.4.2.2 *Charge Amplifier Prototype*

A fully-differential charge amplifier prototype board was designed and manufactured to test the topology. The prototype included additional conditioning stages cascaded to the charge amplifier, providing gain and bandpass filtering: a simplified schematic of the complete signal chain is shown in Figure 4.35.

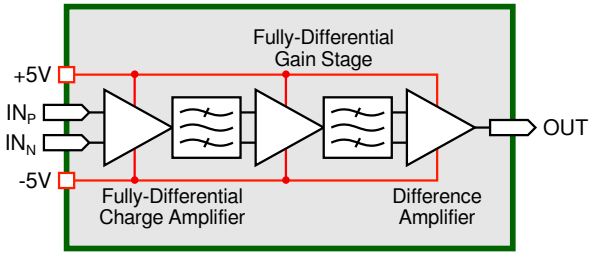
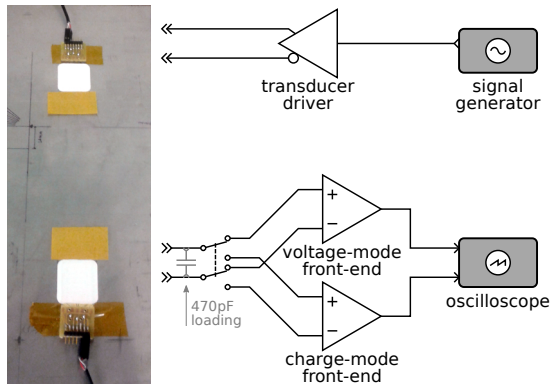


Figure 4.35: Block scheme of the fully-differential charge amplifier prototype, showing the whole signal conditioning chain.

4.4.3 *The Advantage of Charge-Mode Interfacing*

An experiment was set up to prove the benefit of using a charge amplifier in the presence of unwanted capacitive sensor loading.

Two IDTs were taped to an aluminum plate and used to pitch / catch a Lamb wave packet (see Figure 4.36). Reception was performed with an instrumentation amplifier (the front-end described in Section 3.2.1), and the prototype charge amplifier presented above.

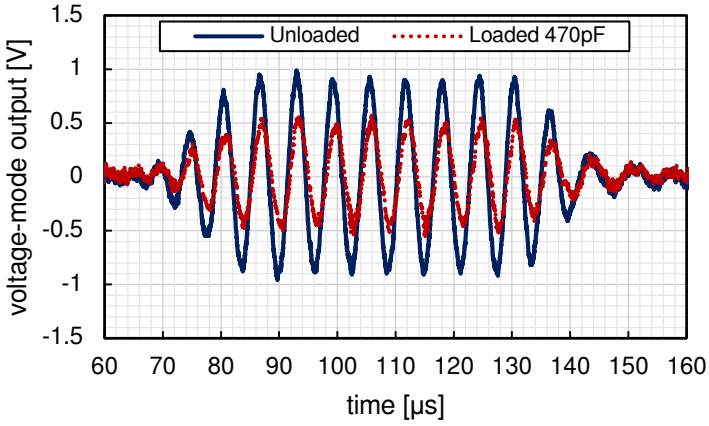


(a) (b)

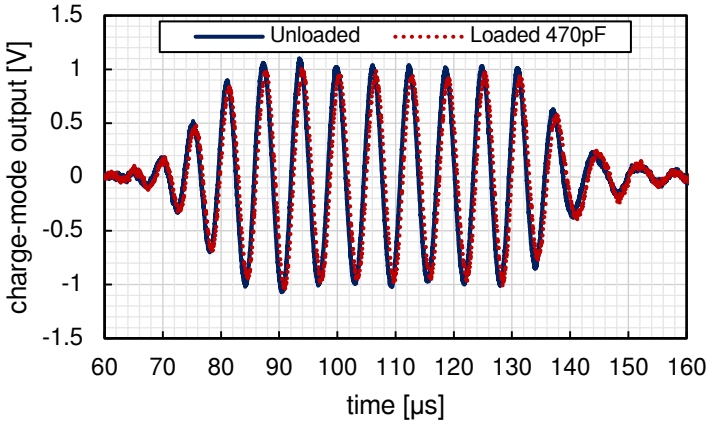
Figure 4.36: Setup used to compare voltage and charge-mode interfacing: (a) IDTs taped to an aluminum plate (1.2 mm thick) at a distance of 150 mm; (b) schematic depiction of the instrumentation.

A tone burst centered at 160 kHz was transmitted with one IDT, and the signal received by the other IDT was alternately routed to one of the two pre-amplifiers, and acquired with the oscilloscope. The measurements were repeated after adding a 470 pF capacitor across the receiving IDT terminals, and the results can be compared in Figure 4.37 (The two front-ends had slightly different overall gain, but the electrical connection of the transducer was kept the same).

The plots clearly show that loading the transducer affected in a significant way only the voltage-mode receiver, while the signal conditioned with the charge amplifier is almost identical to the unloaded case.



(a)



(b)

Figure 4.37: Comparison of the signals received with and without additional capacitive loading of the sensor: (a) voltage-mode front-end; (b) charge-mode front-end.

4.4.4 *Improving the Charge Amplifier*

The limitations of the fully-differential charge amplifier design presented above are mainly connected to the performance of commercially available operational amplifiers. It is clear from the expression of the input impedance (Equation 4.15) that increasing the gain of the amplifier comes at the cost of increasing its input impedance, unless the open-loop gain of op-amp U_1 can somehow be increased too.

The fully-differential charge amplifier was designed using a FET-input op-amp (Texas Instruments OPA657) with rather large open-loop DC gain (70 dB) and GBW (1.6 GHz), and a bias current so low ($\pm$2 pA) that it could be easily supplied through the very large feedback resistors R_F with negligible voltage drop. This device required a supply voltage between 8 V and 10 V.

The sought after improvements of the charge amplifier included increasing the charge conversion gain, at the same time decreasing the input impedance, and reducing the supply voltage to 5 V, or less.

Operational amplifiers with better open-loop performance and reduced supply voltage are available in bipolar technology, like the Texas Instruments LMH6629. The adoption of such component, however, arose the question of how to provide the input biasing current, as bipolar op-amps require a significant one (in the tens of microamps).

Without going into ASIC territory, the solution to the biasing problem was found by introducing an input buffering stage built with a MOSFET differential pair, as shown in Figure 4.38. The matched NMOS devices were commercially available as discrete components from Advanced Linear Devices, part number ALD1101A.

The new, buffered charge amplifier retained most of the functional characteristics of the previous version, with the proper distinctions. Apart from buffering the input bias current of U_1, the differential pair was also used to further increase the open-loop gain: cascading the differential pair (with gain $A_{D,pair}$) and op-amp U_1 (with open-loop gain A_{OL}) resulted in a combined open-loop gain of $A_{COL} = A_{D,pair} \cdot A_{OL}$.

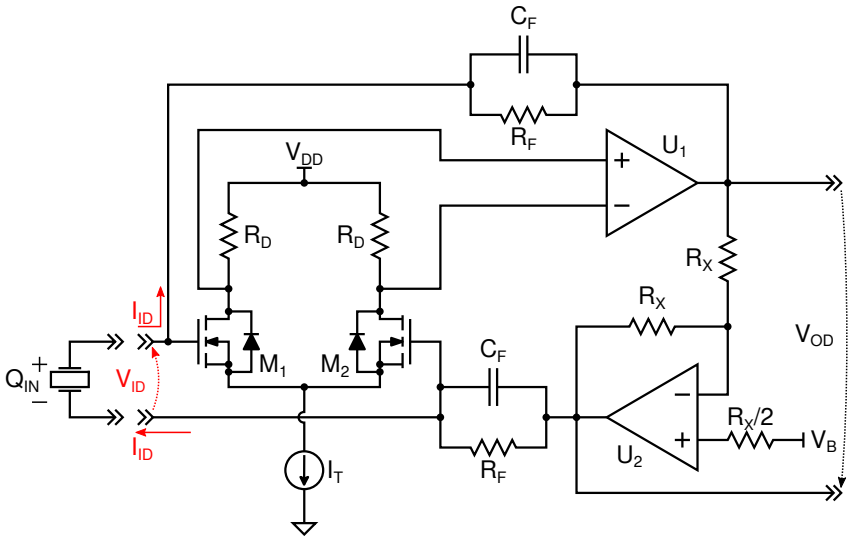


Figure 4.38: Simplified schematic of the improved fully-differential charge amplifier.

This parameter defined the differential input impedance of the new topology according to Equation 4.17.

$$Z_{IN} = \frac{V_{ID}}{I_{ID}} = \frac{2 \cdot (R_F \parallel C_F)}{1 + 2 \cdot A_{COL}} \tag{4.17}$$

4.4.4.1 *Charge Amplifier Design Guidelines*

Neglecting the additional differential pair for the time being, some general design considerations can be done regarding the charge conversion transfer function of the amplifier, and how it is affected by the parasitic components present at the inputs.

A lumped-element equivalent network of the input parasitic components is shown in Figure 4.39. The various elements included there are related to both the charge source (piezoelectric transducer), and the actual design of the amplifier prototype board used for debugging and characterization. The origin of such components is anticipated here, and will be expanded later in Section 4.4.6: the two R_{series} represent the on-resistance of the analog multiplexer, C_{stray} models the

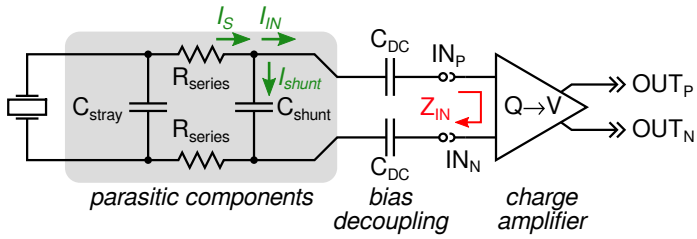


Figure 4.39: Lumped element equivalent network of the parasitic components present at the inputs of the charge amplifier.

parasitic (i. e., non-active) capacitance of the source and of the multiplexer inputs, C_{shunt} models the parasitic capacitance of the multiplexer outputs, C_{DC} are the DC blocking capacitors placed to prevent the multiplexer from affecting the bias point of the charge amplifier.

CONVERSION GAIN AND FREQUENCY RESPONSE The mid-band charge conversion gain of the buffered charge amplifier is defined by the feedback capacitors as $A_{DM} = 2/C_F$. The pole that sets the -3dB high-pass cut-off frequency of the transfer function is determined by R_F and C_F:

$$f_{HP(-3dB)} = \frac{1}{2\pi R_F C_F} \tag{4.18}$$

The low-pass frequency, however, can be easily defined only if a set of approximations are respected. Assuming that C_{stray} is known, and that the total impedance seen across the rightmost terminals of R_{series} is dominated by its real component R_{IN}:

$$f_{LP(-3dB)} = \frac{1}{2\pi \left(R_{series} + R_{IN}\right) C_{stray}} \tag{4.19}$$

However, the assumptions under which the previous expression holds are very strict and, since the input impedance of the charge amplifier tends to be capacitive, the low-pass frequency can only be set by deliberately increasing R_{series} until it prevails over the capacitive component, which is clearly a bad idea, since doing so would also increase the overall load impedance seen by the piezoelectric source.

Consider now the components C_{shunt}, C_{DC}, and Z_{IN}: they form a current divider where the actual signal injected into the amplifier can be calculated with Equation 4.20.

$$\begin{aligned}\frac{I_{IN}}{I_S} &= \frac{\frac{sC_{DC}}{2+sZ_{IN}C_{DC}}}{\frac{sC_{DC}}{2+sZ_{IN}C_{DC}} + sC_{shunt}} = \\ &= \frac{1}{\left(1+2\frac{C_{shunt}}{C_{DC}}\right)\left(1+\frac{sZ_{IN}C_{DC}C_{shunt}}{C_{DC}+2C_{shunt}}\right)}\end{aligned} \tag{4.20}$$

The left-hand factor of the denominator shows that the ratio between C_{shunt} and C_{DC} determines an attenuation of the input signal, and thus C_{DC} should be maximized.

The right-hand factor is frequency-dependent, but can be approximated to Equation 4.21 under the assumption that Z_{IN} is behaving like a capacitor, C_{IN}. This assumption is reasonable when, referring to Equation 4.17, C_F dominates the feedback impedance and A_{COL} has yet to start rolling off.

$$\begin{aligned}\frac{I_{IN}}{I_S} &\approx \frac{1}{\left(1+2\frac{C_{shunt}}{C_{DC}}\right)\left[1+\frac{sC_{DC}C_{shunt}}{sC_{IN}(C_{DC}+2C_{shunt})}\right]} = \\ &= \frac{1}{\left(1+2\frac{C_{shunt}}{C_{DC}}\right)\left(1+\frac{1}{C_{IN}}\cdot\frac{C_{DC}C_{shunt}}{C_{DC}+2C_{shunt}}\right)}\end{aligned} \tag{4.21}$$

The approximate Equation 4.21 shows that the right-hand factor also contributes a broadband attenuation, in this case exacerbated by an increase of either C_{DC} or C_{shunt}, while C_{IN} counteracts the effect. At higher frequency, when the combined open-loop gain A_{COL} starts decreasing and phase-shifting, Z_{IN} loses its capacitive behavior, and a pole is determined by C_{DC} and C_{shunt}.

The conclusion is that, in the absence of significant series resistance between the source and the charge amplifier inputs, the high-frequency behavior of the transfer function is ultimately defined by the open-loop gain, as acting on the other elements of the input network leads to unwanted collateral effects within the passband region.

4.4.4.2 *Additional Differential Pair*

Despite the potential to increase the combined open-loop gain of the charge amplifier, the additional FET differential pair stage had several operating point constraints imposed by the other circuit components, such that the final $A_{D,pair}$ was rather low.

The differential pair performance could have been increased by adopting common analog design techniques, such as using active loads instead of resistors. This path, however, was not ventured, as the fact that this design was made with discrete components resulted in the following circumstances:

- There is a very limited choice of off-the-shelf matched MOSFET pairs (or arrays), and obviously their geometry cannot be adjusted to the application requirements.
- The packages of said devices are big. Increasing the number of MOSFETs in a discrete design leads to a significant increase in circuit board area.
- Discrete, matched MOSFETs arrays are not cheap.
- Resistors with tight tolerance and extended value range are widely available as discrete components.

With reference to Figure 4.38, it is observed the gate voltage of the differential pair corresponds to the DC voltage present at both op-amps output terminals, and is set through V_B. Since the amplifier outputs are the nodes that experience the largest voltage swing during normal operation, it was advisable to keep them biased at mid-supply to reduce nonlinearities. Therefore, the FETs gate voltage was fixed at 2.5 V.

The drain nodes of the FETs, on the other hand, are directly connected to the input terminals of U_1, meaning that they must respect the common-mode input range of the op-amp. The input terminals of the LMH6629 had a large flexibility in the bias point they could accept, up to 3.8 V according to the datasheet.

Eventually, the operating point of the differential pair was set with 2.5 V at the MOSFET gates, and a tail current $I_T = 15$ mA (the tail generator was a discrete NPN BJT current mirror made with a Nexperia BCM61B). Using two precision ($\pm 0.1\%$) load resistors $R_D = 270\ \Omega$, the DC drain voltage of the pair was 2.9 V, while the source terminals rested at 110 mV. At this operating point, the small signal transconductance of the two FETs was $g_m \approx 7$ mS.

When calculating the differential pair gain $A_{D,pair}$, the loading introduced by op-amp U_1 had to be factored in. Unfortunately, the LMH6629 used in the proposed implementation did not have a specified differential input resistance, nor its simulation macro-model was declared accurate with regards to this characteristic: in the absence of official data, simulation results were used as a best guess.

The nominal (unloaded) gain of the differential pair was $A_{D,pair} = g_m R_D = 1.89$, simulations performed by adding U_1 as load showed the gain decreasing to $A_{D,pair} = 1.72$, or 4.7 dB.

The loading introduced by U_1 had also major effects on the bandwidth. Usually, the frequency response of a MOSFET differential pair is determined by the Miller multiplication of the gate-drain capacitance [147, sec. 6.6], however, given the very low gain of this implementation, the frequency response was actually determined by the input capacitance of U_1. Even with such loading, simulations showed that the differential pair bandwidth was wider than the open-loop frequency response of the operational-amplifier.

It is worth noting that U_1 could considerably affect the differential pair frequency response also through the Miller multiplication of any capacitance connected between its inverting input pin and the output (shown as C_M in Figure 4.40). Given the very large open-loop gain of the LMH6629, even a tiny, 1 pF feedback capacitance would have resulted in several nanofarads of additional differential pair loading, and this is the reason why introducing a C_M was avoided during the design.

4.4.4.3 *Stability and Frequency Compensation*

The stability of differential circuits can be tricky to analyze due to the existence of multiple feedback paths and the effect of common-mode feedback [148, 149]. Fortunately, the proposed charge amplifier topology was such that all the feedback loops could be cut open at only one point, shown in red in Figure 4.40, thus defining a single loop gain G_{LOOP}.

Though the low-frequency behavior of the loop gain could be evaluated analytically, the crossover frequency of G_{LOOP} was determined by the interplay of the high-frequency transfer functions of the various active building blocks of the circuit, making this analysis a daunting task that could be effectively approached only through simulation.

The low frequency behavior of the loop gain, however, still provided an important insight into the stability of the charge amplifier.

Equation 4.22 approximates G_{LOOP} at low frequency by assuming that the various gain factors of the active components are flat. The expression refers to the component designators of Figure 4.38, and includes the total capacitance C_{SRC} present at the charge amplifier inputs (i. e., due to both transducer and parasitics).

$$G_{LOOP(LF)} \approx -2A_{COL}\frac{1+sR_FC_F}{1+sR_F\left(C_{SRC}+C_F\right)} \tag{4.22}$$

The equation above shows that the source capacitance contributes in defining the first pole of the loop gain. It can be thus inferred that increasing the source capacitance would pull the loop gain crossover to lower frequency, thus increasing the gain margin. This assumption, however, needs to be checked against the high-frequency phase of G_{LOOP}, which might not be strictly monotonic, leading to the possibility of a reduction in phase margin for certain ranges of C_{SRC}.

All things considered, the effect of C_{SRC} at low frequency still suggests that compensation of the charge amplifier should be performed for the minimum expected source capacitance. In our implementation, such a minimum was provided by the parasitic capacitances introduced by the input multiplexer ($\sim$ 17.5 pF).

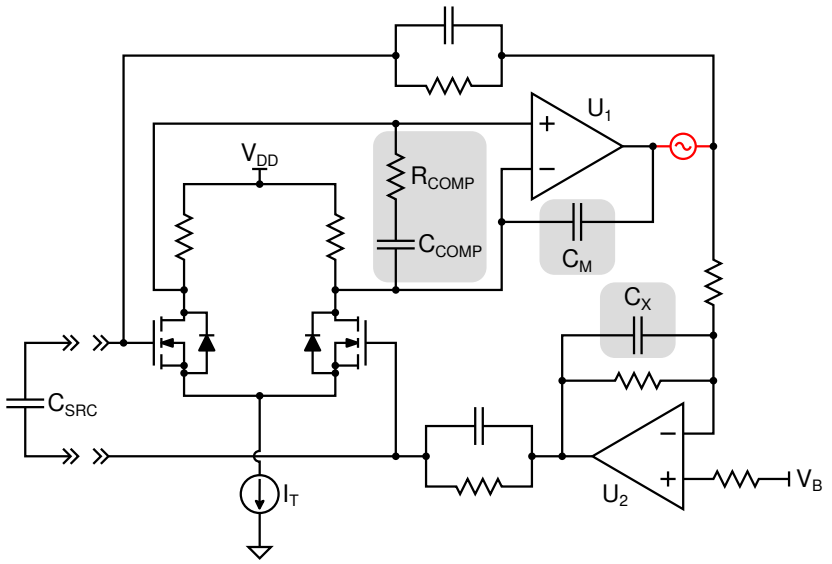


Figure 4.40: Schematic of the components that can be used to compensate the buffered charge amplifier.

Using the circuit simulator, the loop gain was evaluated by including a model of the multiplexer, and the phase margin increased to ~ 70° by introducing the passives highlighted in Figure 4.40 (R_{COMP}, C_{COMP}, and C_X), except C_M (for, as explained in the previous section, the adoption of such component is detrimental). The simulated loop gain of the final, compensated prototype with minimum source capacitance is plotted in Figure 4.41.

The stability analysis and compensation explained above did not include the effects connected to loading of the charge amplifier outputs. This is because of the characteristics of the cascaded stage, a Texas Instruments LMH6517, that did not really affect the loop gain of the charge amplifiers at the frequency of interest.

4.4.4.4 *Evaluation of the Input Impedance*

The input impedance of the proposed charge amplifier could not be measured directly without designing a specific instrument. However, circuit simulations were used to get an idea about the performance

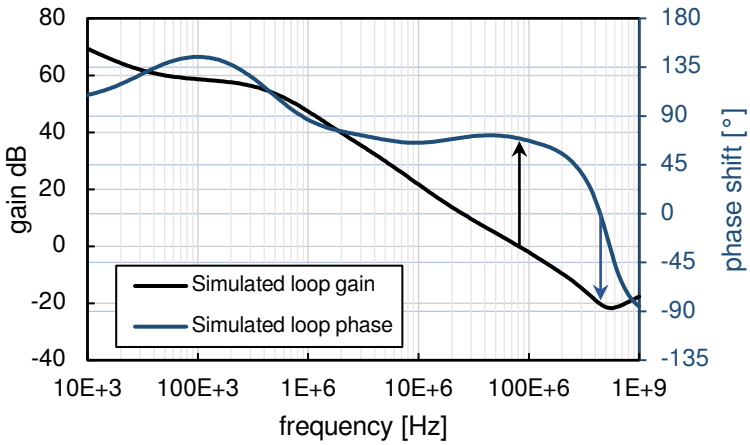


Figure 4.41: Simulated loop gain of the charge amplifier after compensation, with minimum source capacitance (17.5 pF). Phase and gain margins are indicated with arrows.

of the proposed circuit, and how it compared to the original topology described in Section 4.4.2.

The plot of Figure 4.42 shows the input impedance of the fully-differential charge amplifier, alongside that of the improved charge amplifier. Since frequency compensation acted directly on the combined open-loop gain A_{COL}, the input impedance of the buffered charge amplifier is shown for the compensated variant. Note that these simulations do not account for the parasitic components shown in Figure 4.39, they only show the impedance seen at the charge amplifier's own inputs.

4.4.4.5 *Characterization of the Amplifier*

Some definitions need to be given before diving into the characterization of the charge amplifier.

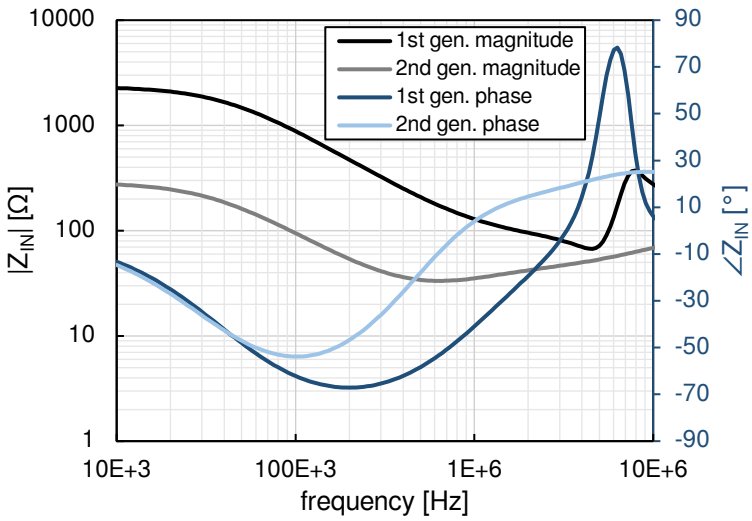


Figure 4.42: Simulated input impedance of the first (Figure 4.34) and second generation (Figure 4.38) charge amplifiers, including the effects of frequency compensation.

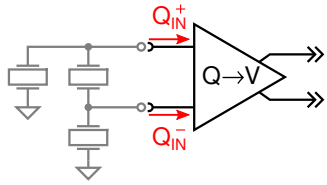


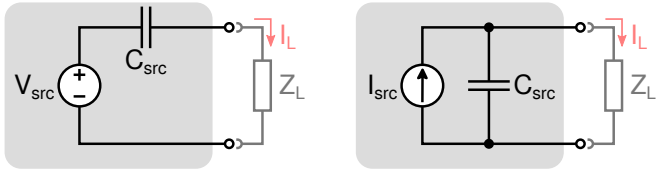
Figure 4.43: Definition of the charge flow in a differential configuration.

With reference to Figure 4.43, the differential and common-mode charge signals injected at the inputs of the amplifier are defined as follows:

$$\begin{aligned} Q_{I,DM} &= \frac{Q_{IN}^{+} - Q_{IN}^{-}}{2} \\ Q_{I,CM} &= Q_{IN}^{+} + Q_{IN}^{-} \end{aligned} \tag{4.23}$$

These definitions will be maintained throughout this section.

A PROPER CHARGE SOURCE A charge source can be made with either one of the dual circuits shown in Figure 4.44, corresponding to the *Thévenin* and a *Norton* equivalent sources. Their equivalence, however, is not as straightforward as it may seem at first glance.



(a) (b)

Figure 4.44: Equivalent charge source models: (a) Thévenin; (b) Norton.

Consider both the equivalent sources shown in Figure 4.44 closed on a low-impedance load, such that $Z_L \ll Z_{src}$ within the bandwidth of interest. The output charge signal is represented by the time integral of the current delivered to the load (i_L) or, in the Laplace domain, by I_L/s.

Assume that the source of Figure 4.44a is driven with an AC signal of constant amplitude; since the voltage divider between C_{src} and the load is largely dominated by the source capacitance, the output charge signal will remain practically constant in amplitude as the AC frequency is swept.

In the case of Figure 4.44b, the current divider formed between C_{src} and Z_L is dominated by the load, which sinks almost the totality of the current. Therefore, if the input AC current signal is kept at a constant amplitude through the frequency sweep, the actual charge signal delivered to the load will shrink with increasing frequency.

As a matter of fact, one approach may be better and easier to implement than the other, depending on the measurements that have to be performed, and the instrumentation at hand. In this work, only voltage-based equivalent sources were used.

MEASURING THE DIFFERENTIAL AMPLIFICATION A purely differential charge source was built using a FDA (Texas Instruments

LMH6552) in single-ended to differential configuration (active balun), and adding two capacitors of equal value (C_{source}= 3.3 pF) in series with the outputs. The total capacitance was therefore 1.65 pF, a value sufficiently low to result in a source impedance considerably higher than the charge amplifier's simulated input impedance up to 10 MHz.

A simplified schematic of the charge source and the measurement setup is shown in Figure 4.45, a picture of the charge source board is shown in Figure 4.46.

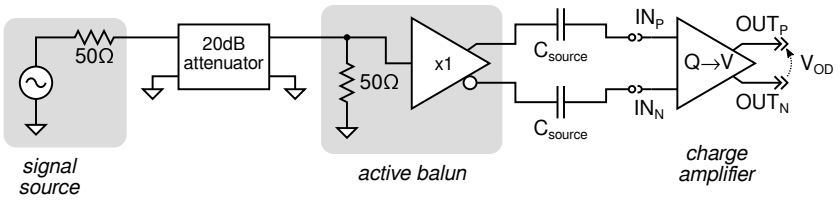


Figure 4.45: Simplified direct measurement setup for the charge amplifier differential-mode gain.

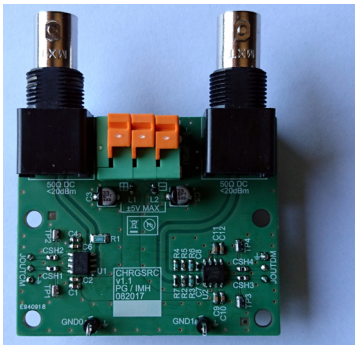


Figure 4.46: Picture of the differential-mode charge source. Board size is 60×50 mm.

Under the condition that the voltage divider seen from the balun (i. e., the FDA outputs) was largely dominated by the two source capacitors, the differential amplitude of the charge signal injected by the source could be approximated as:

$$|Q_{source}| = |V_{source}| \frac{C_{source}}{2} \tag{4.24}$$

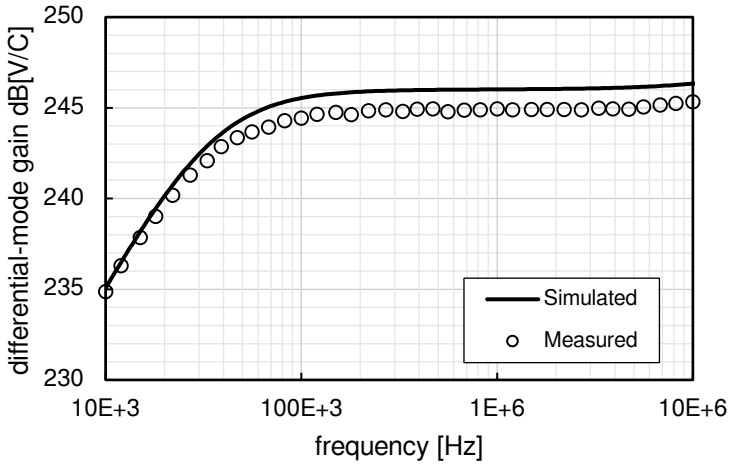
The actual transfer function between the benchtop signal generator and the differential outputs of the active balun was measured on its own to extrapolate a gain / phase correction factor that was later applied to the charge amplifier measurements.

With the input signal thus characterized, the differential charge-to-voltage conversion transfer function could be measured, and the result is compared with the simulation in Figure 4.47.

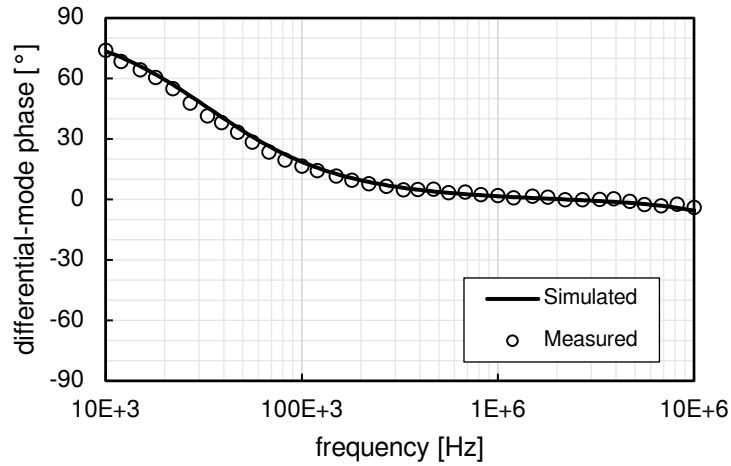
COMMON-MODE REJECTION While directly measuring the differential response of the charge amplifier was a rather simple task that could be solved with the adoption of a special balun, measuring the common-mode response was another thing entirely.

To gain some perspective on the matter, one can start by looking at the usual way differential, voltage-input amplifiers are characterized: by connecting a single-ended voltage source to the short-circuited inputs of the amplifier, the injection of a pure common-mode signal is guaranteed, and the common-mode gain can be directly measured.

The importance of measuring the common-mode gain directly cannot be overstated. Any differential amplifier is expected to provide a significant common-mode rejection ratio (CMRR) and, depending on the circuit performance, the disparity between differential and common-mode gain could be many orders of magnitude. In those situations, trying to indirectly extrapolate the common-mode from measurements where both contributions are present becomes an insurmountable task, as the *resolution limits* of the instrumentation will obliterate the common-mode contribution buried within the differential signal.



(a)



(b)

Figure 4.47: Simulated and measured differential transfer function of the buffered charge amplifier: (a) gain; (b) phase.

INDIRECT COMMON-MODE GAIN EXTRAPOLATION The resolution required to indirectly extract the common-mode gain from a mixed measurement can be estimated by considering the setup illustrated in Figure 4.48, which was one of the many possible measurements approaches considered during this work.

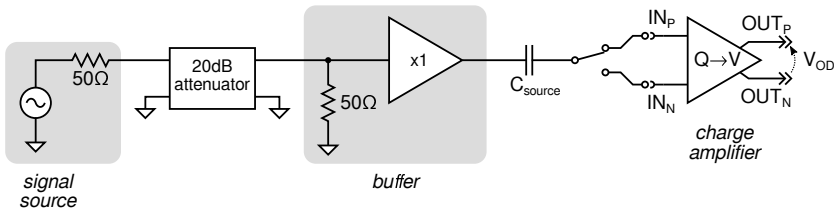


Figure 4.48: Simplified indirect measurement setup for the charge amplifier common-mode gain.

A single ended charge source is used to apply the same input signal alternately to the positive and negative inputs of the charge amplifier, while no signal is injected inside the other terminal. Assuming that the input signal does not drift between measurements, the two resulting traces acquired at the charge amplifier outputs will be composed of a common-mode contribution (identical in both cases), and a differential-mode contribution with same magnitude but inverted phase.

If we indicate with V'_{OD} the output measured with the source connected to IN_P, and V''_{OD} the one measured with the source connected to IN_N, the common-mode output can be extracted with a simple computation:

$$\begin{aligned} V_{OD,CM} &= \frac{V'_{OD} + V''_{OD}}{2} = \\ &= \frac{(V_{OD,CM} + V_{OD,DM}) + (V_{OD,CM} - V_{OD,DM})}{2} \end{aligned} \tag{4.25}$$

Unfortunately, calculating the expression above becomes far from simple if done in the digital domain, after the two output traces have been acquired.

The resolution needed to properly appreciate the common-mode signal in the presence of a differential mode can be evaluated roughly

by assuming that the CMRR of the charge amplifier under test is known.

With reference to the setup of Figure 4.48, the input differential and common-mode charge signals are known and related by $Q_{I,DM} = Q_{I,CM}/2$, hence the ratio between the differential and common-mode components of V_{OD} is exactly half the CMRR, or:

$$\frac{V_{OD,DM}}{V_{OD,CM}} = \frac{Q_{I,DM} \cdot A_{DM}}{Q_{I,CM} \cdot A_{CM}} = \frac{A_{DM}}{2A_{CM}} \tag{4.26}$$

When sampling V_{OD} with an ADC, assuming that the signal is scaled to the full dynamic range, the ratio between differential and common-mode signals translates into a minimum required $SNR_{dB} \geqslant CMRR_{dB} - 6.02$. For an ideal ADC, the SNR due to quantization corresponds to $SNR_{dB} = 6.02 \cdot N + 1.76$, where N is the number of bits [150]. The minimum number of bits required to avoid obliterating the common-mode signal is thus:

$$N \geqslant \frac{(CMRR_{dB} - 6.02 - 1.76)}{6.02} \tag{4.27}$$

As an example, assume that the CMRR of the amplifier at a certain frequency is 80 dB: the absolute minimum number of bits required as per the above equation is 12, and this estimate completely neglects the presence of noise. Since most oscilloscopes have an effective number of bits (ENOB) around $6 \sim 8$, trying to indirectly extrapolate the common-mode signal by performing operations on digitally acquired waveforms appears to be ill-advised.

A different approach might involve performing the common-mode signal extraction in the analog domain. Although probably feasible, this method requires a significant design effort to build the required instrumentation.

DIRECT COMMON-MODE GAIN MEASUREMENT Theoretically, a pure common-mode charge —or current— signal could be injected into a differential amplifier by connecting its input ports in series (as opposed to voltage-mode differential amplifiers, where the inputs need to be shunted). This connection unfortunately requires that

the two input ports have separate return terminals (not the circuit ground), which was clearly not the case in the proposed charge amplifier. The alternative was building a dual charge source with matched outputs.

The problem of directly measuring the common-mode charge conversion gain has already been addressed in [151], where the authors used two *Norton* equivalent sources to build a common-mode charge source that required only a single capacitor. An equal current signal was injected by two current-feedback amplifiers configured as V-to-I converters bridged across the source capacitor terminals, thus avoiding the need to use two capacitance-matched sources.

The common-mode source built for this work used a single voltage buffer with its output connected to two source capacitors in parallel, which were in turn attached to the positive and negative inputs of the charge amplifier. A simplified representation is shown in Figure 4.49, while the full schematic can be found in Appendix B.

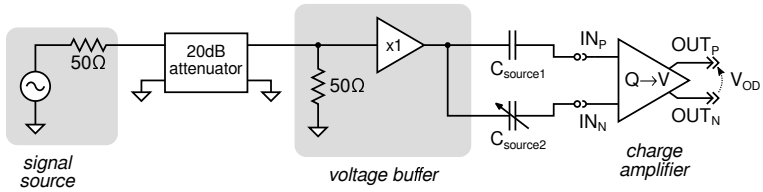


Figure 4.49: Simplified direct measurement setup for the charge amplifier common-mode gain.

$C_{source1}$ was a fixed, 2 pF thin-film capacitor, while $C_{source2}$ was actually a network including a precision trimmer, specifically crafted to provide a worst-case fine adjustment range of about 150 fF around the nominal value of $C_{source1}$, enough to cover all the combined tolerance mismatches of the capacitors. A picture of the common-mode charge source board is shown in Figure 4.50.

Trimming the source was necessary because no commercially available capacitor could provide a sufficiently tight tolerance to reduce the spurious differential-mode signal to an acceptably small amplitude.

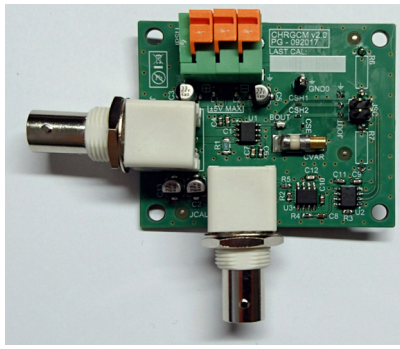


Figure 4.50: Picture of the common-mode charge source. Board size is 60×50 mm.

Ideally, the trimming process should aim at a condition where $C_{source1}$=$C_{source2}$: in that case the charge signals injected at the two inputs of the amplifier would be identical, and no differential-mode would be present. This approach, however, fails to address the effects of *unbalanced input impedance* of the charge amplifier itself, as the topology is *non-symmetrical* and therefore a certain amount of single-ended input impedance mismatch is present. This mismatch becomes even more significant at high frequency, where the impedance of the source capacitors is lower.

An attempt at direct calibration of the two capacitors was done regardless, using a high-CMRR difference amplifier specifically included on the charge source circuit board (the schematic can be found in Appendix B). As expected, the attempt failed to provide satisfying results due to systematic unbalances affecting the calibration procedure.

In light of the previous considerations, a different calibration technique was pursued: one that involved the charge amplifier itself.

The idea was to trim $C_{source2}$ *online*, when connected to the charge amplifier, by observing and trying to minimize the amplifier's output signal, which would also take care of the intrinsic unbalance of the input impedance.

Of course this procedure hid a perilous pitfall: the minimum output of the charge amplifier did not necessarily correspond to the mi-

nimization of the differential input signal, but could be due to the mutual cancellation of the differential and common-mode contributions.

A solution to the dilemma of calibration was found through the simulator. By doing a Monte Carlo run of the charge amplifier that included all the passive component tolerances, the resulting set of common-mode gain transfer functions showed a remarkable feature: all the simulations converged at 10 MHz, as shown in Figure 4.52 (the plot only includes twenty outcomes). This point of convergence was thus used as a reference to calibrate the common-mode charge source.

The Monte Carlo simulations also showed the presence of an antiresonance peak in the common-mode gain, whose frequency changed (or the peak completely disappeared) depending on the mismatch of the passive components. This antiresonance was also observed in the measured common-mode gain, reported together with the simulations in Figure 4.52.

The common-mode rejection ratio could then be computed by dividing the differential-mode gain of Figure 4.47 by the common-mode gain of Figure 4.52, obtaining the curve plotted in Figure 4.51.

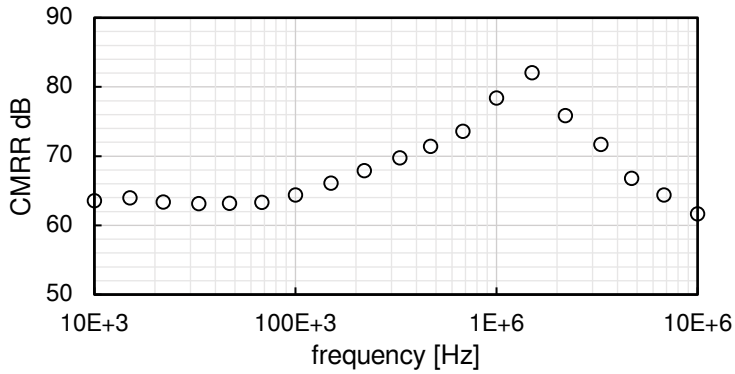
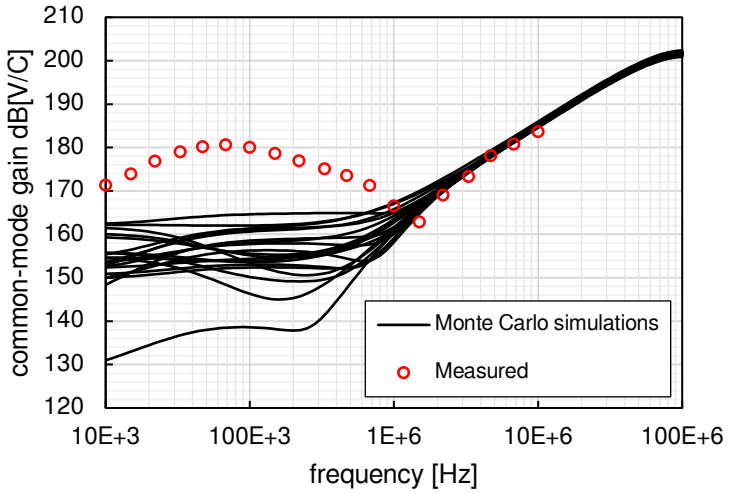
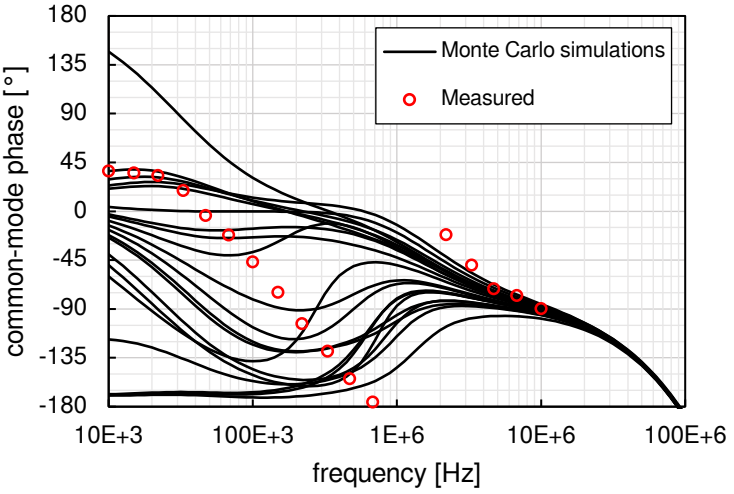


Figure 4.51: Measured common-mode rejection ratio of the buffered charge amplifier.



(a)



(b)

Figure 4.52: Simulated and measured common-mode transfer function of the buffered charge amplifier: (a) gain; (b) phase.

OUTPUT NOISE MEASUREMENTS The output noise spectral density (NSD) of the proposed charge amplifier was measured with the setup illustrated in Figure 4.53.

The differential output was converted to a single ended signal using a wide-band transformer (Coilcraft TTWB2010L), and matched to the spectrum analyzer input impedance. This matching resulted in a 1 : 2 signal attenuation at the instrument input, and a 100 Ω load at the charge amplifier outputs.

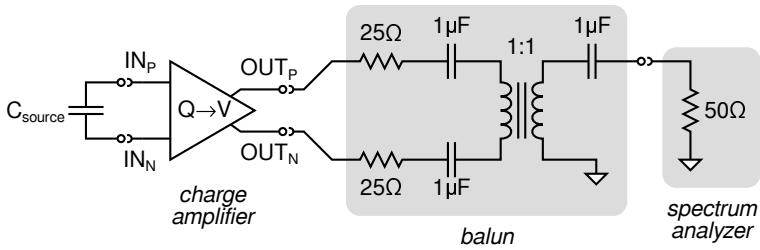


Figure 4.53: Setup used to measure the output noise of the charge amplifier.

Capacitors of increasing size were attached to the inputs to evaluate their effect on the output noise level, since the voltage gain of the charge amplifier is given by the ratio of the source and feedback capacitances.

The measurements shown in Figure 4.54 corroborate this, as increasing C_{source} resulted in a higher amplification of the input voltage noise. It should be noted that the baseline output noise shown as *open circuit* was determined by the parasitic capacitances of the analog multiplexer at the inputs.

DYNAMIC RANGE AND DISTORTION As closure to this section, a comment should be made about the dynamic range of the proposed charge amplifier. Given the very large gain (2 TV/C), and an output full-scale (FS) range of ±2 V peak-peak, the maximum input charge was about ±1 pC. The total harmonic distortion (THD) at the output of the amplifier, when closed on a 100 Ω load (same as in Figure 4.53), was measured using a 500 kHz input tone at full-scale and −1 dBFS.

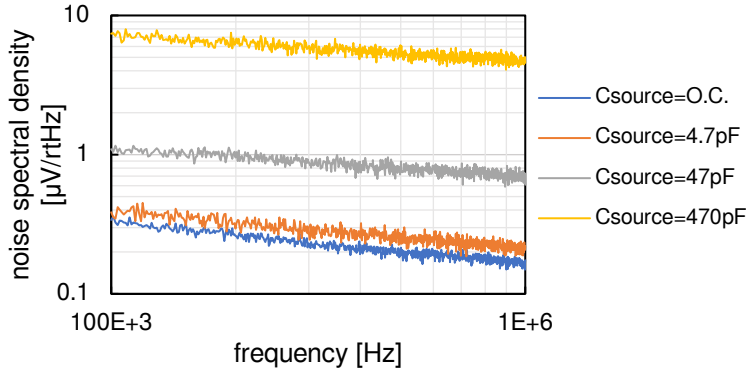


Figure 4.54: Measured output noise spectral density of the charge amplifier.

Using a signal source with an intrinsic $\text{THD}_{\text{src}} = 0.05\%$ at 500 kHz, the measured total harmonic distortion of the charge amplifier was $\text{THD}_{-1\text{dBFS}} = 0.12\%$, and $\text{THD}_{\text{FS}} = 0.13\%$.

4.4.5 *Instrumentation Amplifiers Yet Again*

It would be unreasonable to assume that a charge amplifier could be a one-size-fits-all solution for every piezoelectric sensors apt to SHM applications. Sometimes the simplicity that comes from voltage-mode interfacing, especially when using piezoceramic transducers, outweighs the benefits provided by a more complex topology like the fully-differential charge amplifier.

This is why a custom instrumentation amplifier was also designed and implemented as an alternative sensor pre-amplifier, modifying the classical three-op-amp topology to make it fully-differential. The transfer function was based on the active-mode receiver built-in the legacy SHM system, as described in Section 3.2.1.

Figure 4.55 shows a simplified schematic of the amplifier, where the output was made differential by replacing the subtractor stage with an FDA.

Instrumentation amplifiers represent one of the circuit topologies that can provide the highest input impedance. In the general case,

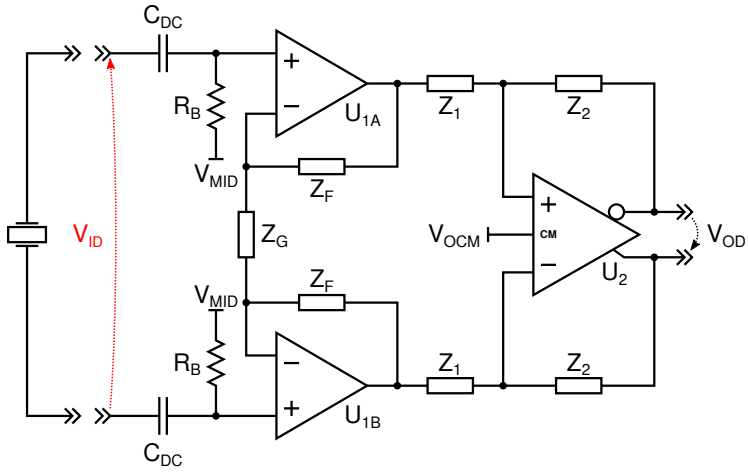


Figure 4.55: Simplified schematic of the fully-differential instrumentation amplifier.

with both inputs DC coupled to the source, the input impedance will be defined by the op-amps themselves: if those components have FET differential input stages, its value can be extremely high ($10^9 \sim 10^{12}$ Ω or more are not uncommon).

The design of instrumentation amplifiers complicates when the source is capacitive, or needs to be AC coupled. In those cases, there is a need to provide some form of DC path to a reference voltage, so that the inputs of the op-amps are biased at a valid operating point.

Since the inputs of FET-based op-amps have a very low bias current (in the order of picoamps), they usually can self-bias and reach an equilibrium DC voltage where the leakage current of the integrated ESD protection diodes is balanced. However, relying on the ESD diodes to bias the inputs should be avoided, for the actual DC operating point will be unpredictable and prone to significant thermal drift, which may bring the input stage outside of its specified common mode voltage range.

Biasing resistors are thus connected between the inputs and a reference voltage to fix the operating common-mode input voltage of the op-amps (R_B in Figure 4.55). Their value should be as high as possible, since they decrease the total input impedance of the amplifier.

In the proposed design, the dual operational amplifier U_1 was a Texas Instruments OPA2300, a CMOS device characterized by a maximum input bias current of ± 5 pA. Thanks to this very low current, 25 MΩ biasing resistors could be used without risking the introduction of significant DC offsets.

The unabridged schematic of this instrumentation amplifier can be found in Appendix B.

4.4.5.1 *Characterization of the Amplifier*

The instrumentation amplifier was characterized in two steps by first measuring the common-mode amplification, by applying a signal to the inputs shorted together, and then measuring the mixed-mode amplification, obtained by applying a signal to the positive input with the negative input grounded. The differential amplification was then computed from the two measurements.

Following the simplified schematic of Figure 4.56, the input signal is defined as $V_{IC} = [V(IN_P) + V(IN_N)]/2$, while the differential output is $V_{OD} = V(OUT_P) - V(OUT_N)$. This setup allows the direct measurement of the common-mode gain $A_{CM} = V_{OD}/V_{IC}$.

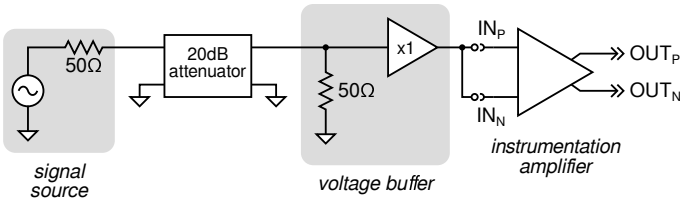


Figure 4.56: Setup used to measure the common-mode gain of the instrumentation amplifier.

With the setup shown in Figure 4.57, on the other hand, both differential ($V_{ID} = V(IN_P) - V(IN_N)$) and common-mode ($V_{IC}$) signals are injected by the source, with the common-mode amplitude being exactly half of the differential-mode. The output signal will thus be the sum of two contributions:

$$V_{OD} = V_{ID} \cdot A_{DM} + V_{IC} \cdot A_{CM} = V_{ID} \left(A_{DM} + \frac{A_{CM}}{2} \right) \tag{4.28}$$

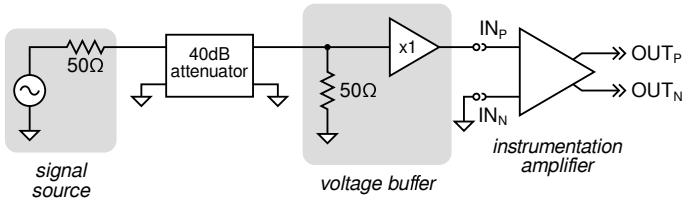


Figure 4.57: Setup used to measure the mixed-mode output of the instrumentation amplifier.

Where A_{DM} is the differential amplification, which can be now extrapolated by solving Equation 4.29.

$$A_{DM} = \frac{V_{OD}}{V_{ID}} - \frac{A_{CM}}{2} \tag{4.29}$$

The resulting differential amplification of the proposed amplifier is plotted in Figure 4.58, alongside the corresponding simulation. The common-mode rejection ratio (CMRR $= A_{DM}/A_{CM}$) is reported in Figure 4.59.

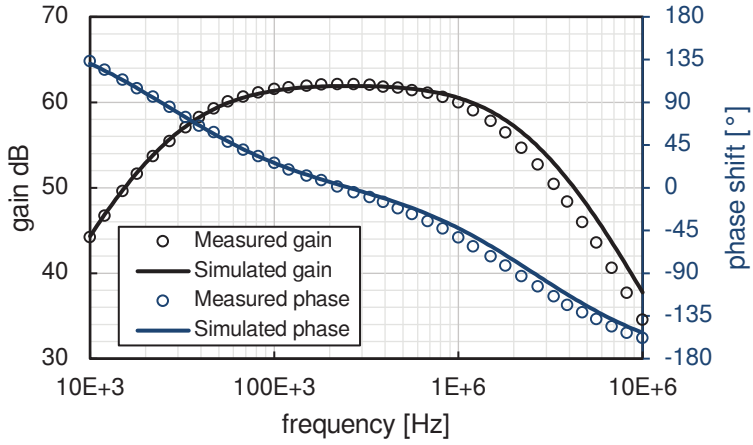


Figure 4.58: Simulated and measured transfer function of the fully-differential instrumentation amplifier.

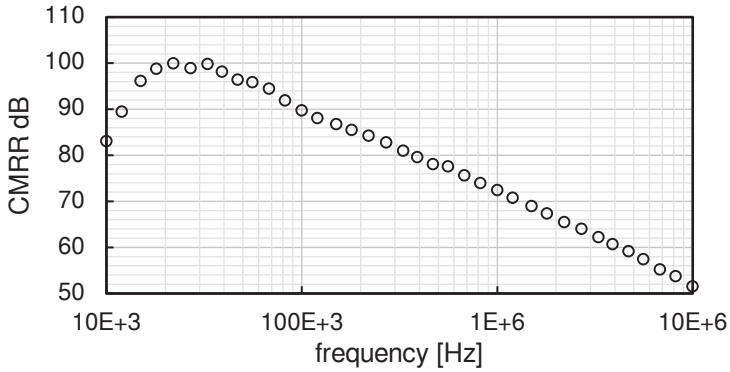


Figure 4.59: Measured common-mode rejection ratio of the fully-differential instrumentation amplifier.

4.4.6 *The Complete Analog Front-End*

Preamplifiers alone do not make for good front-ends: ancillary electronics are needed to ensure the signal is effectively acquired by the analog-to-digital converter that ties up the receiver chain. A prototype, single-channel analog front-end was thus designed including all the components needed for the task.

The preamplifiers described in Section 4.4.4 and Section 4.4.5 were both included in the prototype, placed side-by-side, their inputs and outputs swapped through analog multiplexers. The input multiplexer was a Texas Instruments TS5A23157, while the outputs were swapped with a Texas Instruments TS5A23159.

The additional cascaded stages were a digital VGA, and an anti-aliasing filter / ADC driver.

The prototype provided an isolated digital control interface and hosted several voltage regulators required to operate the electronics off of a single bus rail > 5.5 V. Figure 4.60 shows a concise block scheme of the complete analog front-end, while Figure 4.61 is a picture of the first prototype board assembled.

The DVGA (Texas Instruments LMH6517) supported gain settings between -9.5 dB and 22 dB in 0.5 dB steps, programmable through the isolated SPI interface. The AAF/ADC driver was designed fol-

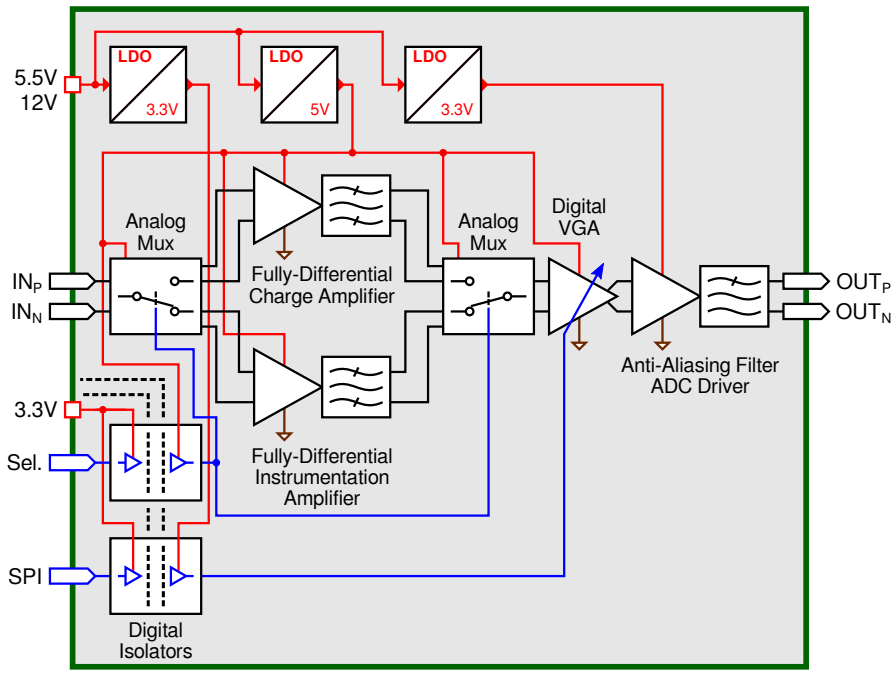


Figure 4.60: Block scheme of the single-channel analog front-end prototype, showing the whole signal conditioning chain, the control interfaces, and the power architecture.

lowing the manufacturer's guidelines to directly interface with the ADS52J90 ADC. Overall, the usable analog front-end bandwidth was between 100 kHz and 1 MHz.

The last revision of the prototype schematics, including all the corrections introduced during the debugging phase, can be found in Appendix B.

The task of turning the final revision of this prototype front-end into an eight-channel module is ongoing. Although the prototype PCB area was pretty generous (100×80 mm), most of the space was wasted to add test-points and generally increase the ease of access while debugging the electronics (the vast majority of the components were placed on one side of the circuit board). Some of the integrated circuits adopted in the prototype are also available in dual or

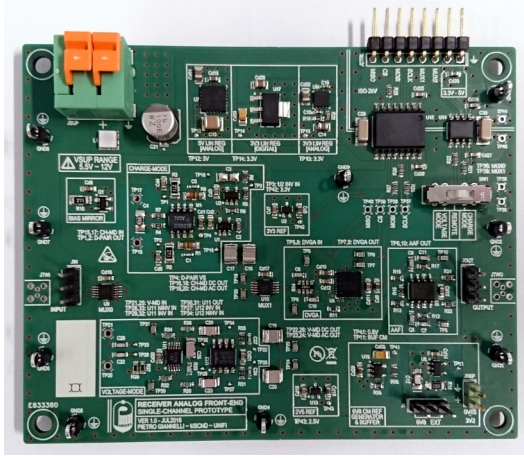


Figure 4.61: Picture of the first single-channel analog front-end prototype. Board size is 100×80 mm.

quadruple version, and the point-of-load regulators should not need being increased in number (they will possibly be replaced with parts supporting higher load current). The target area of the multi-channel front-end is currently set at ~ 30 cm².

Part III

UNTRODDEN TRAILS

5

COMPLETING THE TESTBENCH SYSTEM

The electronics developed so far have covered the transmission and reception blocks of the Pandora daughter card, plus a subsection of the soft design tasked with operating the driver module.

Starting from the daughter card block scheme presented in the previous chapter, here reproduced in Figure 5.1, let us review the remaining modules and their possible implementation.

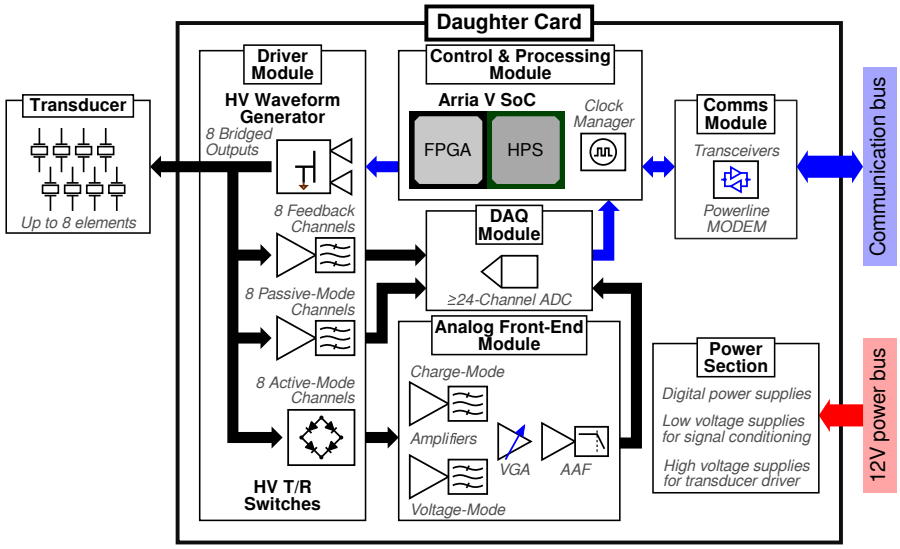


Figure 5.1: Target architecture of a daughter card.

5.1 ACQUIRING THE DATA

A multichannel ADC has already been selected to acquire all the analog signals conditioned on the daughter card, the Texas Instruments

ADS52J90: a device that includes 16 independent ADCs multiplexed 2 : 1 to 32 input channels.

The ADS52J90 resolution can be set to either 10-bit, 12-bit, or 14-bit, and the supported sampling rate per channel (when operating in 32-channel mode) goes from the absolute minimum of 2.5 MSps, to a maximum of 50 MSps (at 10-bit resolution), or 32.5 MSps (at 14-bit resolution).

24 out of the 32 inbound channels are already assigned to sampling the 8 active-mode signals, 8 passive-mode signals, and 8 feedback signals. The remaining 8 channels are currently free and may be possibly used to acquire the data from other sensors.

Clocking will be managed by the Texas Instruments LMK0482X, as it is currently used on both the Arria V SoC development kit and the ADS52J90 evaluation module, and there is no real reason to change it. The converter will operate at two rates: *fast* for sampling in active-mode (e. g., 20 MSps), and *slow* for passive-mode (5 MSps). The system may actually scale the clock rather than decimating the sampled data stream to save power while in passive-mode.

Though fully integrated analog front-ends for ultrasound applications do exist that provide high-performance multichannel LNAs, filters, and ADCs (see, for instance, the Texas Instruments AFE58JD32), they were not considered for this testbench architecture, as it was deemed more important to maintain a complete control over the signal chain at this stage.

5.2 A MATTER OF POWER

5.2.1 *Main Power Bus*

A single, 12 V bus bar is planned to power all the daughter cards in parallel, and the cards themselves are supposed to internally perform all the conversions needed to supply their own electronics. Since the daughter cards require a number of different voltage rails, connecting several external power buses would be problematic for a couple of reasons:

- Such power architecture would not be scalable.
- From the point of view of a wired sensor network, increasing the number of wires should be avoided.

The off-line power supply unit generating the 12 V bus does not have particular requirements at this time, except that the specified output voltage range should remain within 10–14 V. The maximum power rating will be decided upon completion of the daughter card hardware.

5.2.2 *Local Power Converters*

The initial driver module prototype, described in Section 4.3.1, included a first attempt at providing a high-performance power architecture for the driver power stage, which unfortunately failed at actually improving the performance.

Apart from the fast transient response requirements, an important feature that will increase versatility during the experiments is a programmable output voltage (up to the maximum ± 100 V supported by the pulser chips). Moreover, in order to allow the possibility of driving the transducers in continuous wave, the high-voltage power supplies should be able to drop their output to ± 5 V, or provide secondary, low-voltage supplies that take over in those cases.

The adoption of post-regulators in the high-voltage supply chain might still be able to improve the transient response, but the cost in terms of increased system complexity will have to be carefully considered, as such regulators need to be custom-designed (probably using discrete components, and thus bulky), and also provide output voltage programmability.

5.3 SOFTWARE INTEGRATION

Firmware running on Arria V SoC HPS will be moved from the current baremetal implementation to a real-time operating system (RTOS). This upgrade will ease the integration of various software

components and still guarantee the real-time capabilities required for a successful coordination between all the daughter cards.

One of the SHM usage scenarios where real-time operation matters is passive-mode detection and localization. The legacy system described in Chapter 3 performed the passive-mode tasks with moderate simplicity thanks to the convergence of all transducer inbound signal paths to the same data converter. In the Pandora architecture, however, the electronics of each transducer are separate, and passive-mode monitoring becomes a distributed task that must be handled by the software over a shared physical layer.

Moving away from a baremetal firmware is also an essential step to safeguard software portability in the future, in the event of an embedded architecture update.

5.4 CARD INTERACTION AND THE BACKPLANE

The final piece of the Pandora tesbench architecture is the backplane: the board that will connect together a collection of daughter card, allowing them to interact between each other.

The communication module design of the daughter card is strictly connected to the bus architecture that will be realized on the backplane. Given the hybrid topology envisioned for the wired sensor network, the backplane should in principle be able to set-up arbitrary *virtual circuits* between any two (or more) daughter cards by using a digital cross-bar matrix, thus mimicking an arbitrary interconnection topology between sensor nodes.

The daughter card communication module will include at least two independent transceiver, and be able to execute some form of switching between them. Currently, the inter-card communication protocol, that will eventually become the sensor network protocol, has not been decided.

Powerline communications will be tested on the 12 V bus bar that supplies all the daughter cards. In order to do so, each card will be equipped with specific powerline modems.

Aside from the emulated network infrastructure, the backplane will also host embedded processor performing the tasks of a base station. A block scheme is shown in Figure 5.2.

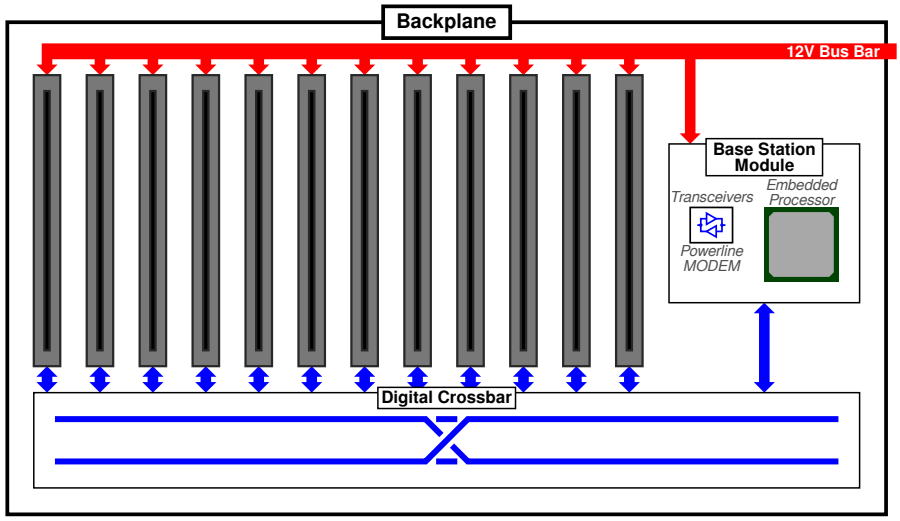
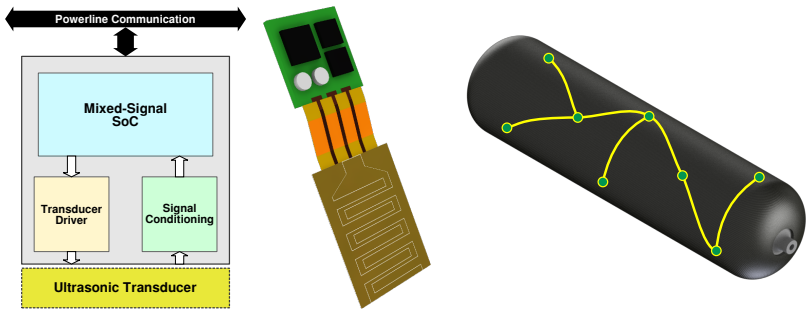


Figure 5.2: Early-stage block scheme of the planned backplane.

6 TOWARD SHM SENSOR NETWORKS

While the actual development of a SHM sensor network is a long way off, this chapter gives an idea of what could be achievable with such system.



(a) (b) (c)

Figure 6.1: A possible sensor node design with attached IDT: (a) node block scheme; (b) node rendering; (c) rendering of a CPV equipped with a sensor network.

A sensor network deployed on the surface of a test object will bring back the ability to perform Lamb wave tomography, improving the technique that was first implemented in the former SHM system [47]. Tomographic techniques have been explored thoroughly in the literature by using transducer scanning systems [152–155]: in the case of a sensor network, however, there is an added layer of complexity connected to the fixed position of the nodes.

Having multiple transducers attached at various points on the target structure could be exploited as a large-scale distributed transmission array, with multiple Lamb wave sources transmitting at the same time [156].

The presence of smart sensor nodes, and a relatively dense interconnection network, can provide some degree of redundancy to the SHM system, where failing sensor nodes will not compromise the operation of the system at large. Of course the thickening of the interconnection network goes against the minimum-obstruction policy that was one of the original goals of the sensor network architecture, but it is a trade-off that should be considered nonetheless.

From the point of view of harnessing, powerline communications represent a way to achieve the minimum amount of cabling required to route the sensor network, albeit at the cost of reduced bandwidth.

A problem that is deeply ingrained in sensor networks that need to cooperate in the ways described above is how to achieve and maintain inter-node synchronization. Although the topic has not been addressed so far, the problem of synchronization in measurement and control networks is well known, and will be approached starting from the provisions of the IEEE 1588 standard [157].

7 A CONCLUSION

The word *conclusion* might seem a bit misplaced at this point but, having reached the end of this dissertation, it is only appropriate to wrap up what has been presented so far.

The work presented in this dissertation covered multiple facets of the development of a testbench system intended to be a versatile research platform for structural health monitoring. The system was devised as a keystone between pure laboratory research activity, and real-world applications where sensor network represent the most promising way to implement structural health monitoring.

The design was approached by trying to follow the most logical path: one that starts from the target application—performing structural health monitoring on composite pressure vessels with guided-wave techniques—continues through the transducers, and finishes with the design of the instrumentation hardware.

The following sections summarize the main results achieved during the research activity.

7.1 TRANSDUCERS

Work on the transducers started from interdigital devices made with piezopolymer film, an existing and proven design already adopted in prior experiments and projects to generate and receive Lamb waves on plate-like structures [47].

Additional sensing elements were included on the piezopolymer film, exploiting the ability of etching arbitrary patterns on the metal coating [158]: local temperature sensing was made possible through a resistive temperature device, and a circular element, modeled after commercial piezoceramic devices, was introduced to allow omnidirectional sensing for impact detection and localization [111].

The first prototype of an interdigital transducer with independent finger connection was presented. The new design leverages the multichannel capabilities that are being built-in the Pandora testbench system, and will be used as an array for Lamb wave generation.

A new manufacturing process for embedding piezopolymer transducers inside flex circuits was preliminarily tested. Although the initial results were quite unsatisfactory, as bonding between PVDF and polyimide could not be achieved with standard sheet adhesive at low temperature, the idea has the potential to seamlessly bring together electronics and piezopolymer transducers.

7.2 TESTBENCH SYSTEM

The Pandora architecture was defined, along with the steps needed to progress towards the realization of wired sensor networks for structural health monitoring.

The development process started with the design of a testbench system that aimed at emulating the components of a sensor network for structural health monitoring, and thus needed to integrate electronics specific to the application (ultrasonic transducer drivers and analog front-ends).

For what concerns the transmission part, an eight-channel, five-level class-D transducer driver was designed and tested. The proposed transmitter can generate arbitrary signals with a bandwidth up to 1 MHz and amplitude up to ± 96 V using a custom multilevel coding scheme. Signal generation is handled by an FPGA core that ensure inter-channel synchronization.

The signal generation technique presented in this dissertation followed a somewhat uncommon approach at switch-mode ultrasound signal generation, and required the design and construction of several hardware and software components from scratch. Albeit much work can still be done to address the various problems encountered during the development, what has been done so far represents a complete *proof-of-concept* of the proposed technique.

After investigating the advantages brought by charge-mode interfacing of high-impedance piezoelectric sensors [159], an improved variant of the differential-input, differential-output charge amplifier was developed providing 2 TV/C of conversion gain, while maintaining $< 100\ \Omega$ input impedance within the 100 kHz–1 MHz bandwidth. This amplifier only requires a single, 5 V supply rail.

The new charge amplifier was merged in a dual-role analog front-end alongside a fully-differential instrumentation amplifier: the two circuits are swapped using analog multiplexers. The proposed analog front-end, which is a single-channel prototype of the multichannel signal conditioning module of the Pandora testbench system, also includes a digital VGA and the anti-aliasing filter / ADC driver.

7.2.1 *Improvements Over the Former System*

Project Pandora started as a follow up to the prototype SHM system described in Chapter 3. The testbench system design tried to both address the limitations described in Section 3.4, and add new features that could be interesting from a research perspective.

Although still early stage, the architecture envisaged for the new system will lift one of the most fundamental problems of the former system: its lack of scalability.

The new transducers improve the versatility in transmission and reception, opening new possibilities (like separate active-mode and passive-mode sensing, and phased array excitation) that were previously precluded.

The transducer driver can handle up to eight channels and allows true arbitrary waveform generation over a wide bandwidth. None of this was possible with the previous pulser. The driver module also provides separate sensing paths for passive-mode and output feedback, all having their own connection to the data converter.

The signal conditioning electronics have been diversified with two kinds of pre-amplifiers, are now completely differential, and provide improved T/R switching.

7.3 FUTURE WORK

Chapters 5 and 6 have described in which direction project Pandora will be moving to fulfill its original plans. It would be unfair, however, to claim that the components developed and covered in this dissertation do not need further improvement and refinement. A succinct list of topics that would benefit from further effort is reported below.

There is a need for the general improvement of PVDF transducer manufacturing technology, especially in consideration of their envisioned integration with the node electronics. Expanding the PVDF-inflex idea can represent a good starting point.

Transitioning to multi-element transducers will lead to re-thinking both their electrode patterns, as many geometries are now possible, and their electrical interface, including cabling and connectors, which have a high risk of becoming too bulky.

The ultrasound driver will need an in-depth study and improvement of its encoding algorithm, which is now elementary, but also, from a hardware perspective, interesting work could be done on closing the feedback loop and designing a new, programmable high-voltage power architecture for the pulsers.

The receiver front-end still presents some details that need fixing, such as the biasing of the charge amplifier differential stage, which is now sub-optimal. Putting together a multichannel circuit will be the logical next step to add another module to the Pandora daughter card.

7.4 FINAL REMARKS

Even though the testbench system remains a work-in-progress, and a wired sensor network is a long way off, most of the design effort was directed at those that are arguably two of the most important pieces of the whole architecture: the transmitter, and the receiver.

Using those two essential components, and of course the transducers, an experimental phase can be started to evaluate and improve

health monitoring techniques and algorithms, while the development of the remaining parts of the testbench architecture is carried out in parallel: the ability to perform some, even elementary experimentation during the hardware design phase can provide invaluable feedback to the designers.

Part IV

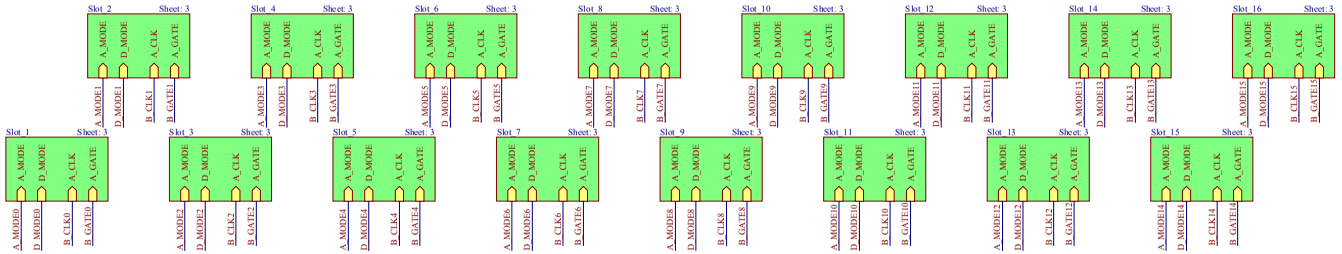
APPENDIX

A

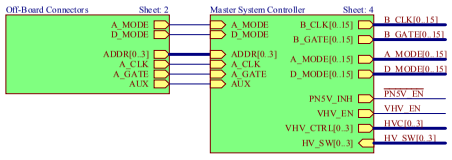
LEGACY SYSTEM ELECTRICAL SCHEMATICS

BACKPLANE

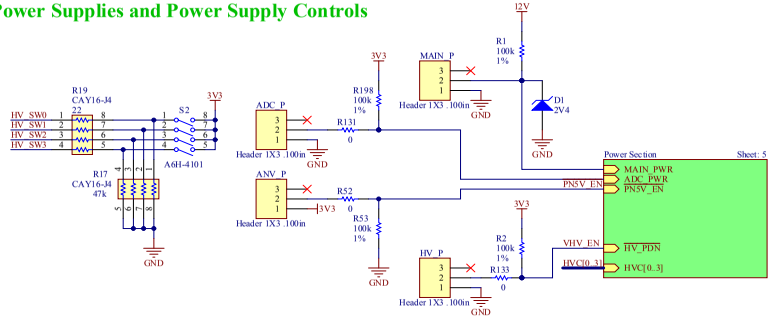
Analog US-Front End Slots



On-Board Electronics



Power Supplies and Power Supply Controls



Global power supply (framed brick, universal input):
TDK-Lambda HWS30A-12/A

Power entry module (w/ switch and 1A fuse):
Schaffner FN283-1-0

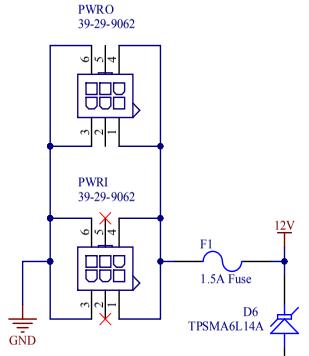
12V power good indicator:
Lumex SSI-LXH600GD12V150

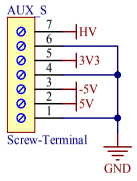
Front panel power switch:
NKK JWM11BA2A-A

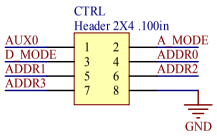
Backplane power good indicator:
Dialight 559-1301-007F w/ 750Ω series resistor

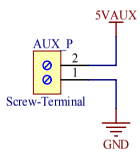
High voltage active indicator:
Dialight 559-0203-007F

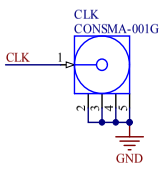
Title: **Backplane Interconnections**			
Organization: **USCND**	Project: **Prototype Backplane**		
Version: 0.7	Revision: Initial	Date: 5/23/2014	
Author: P. Giannelli	Approved By: L. Capineri		
File name: Backplane_Interconnections.SchDoc	Sheet: 1 of 9		

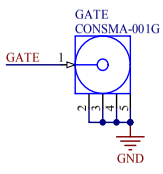


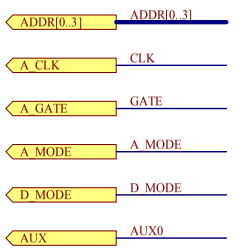








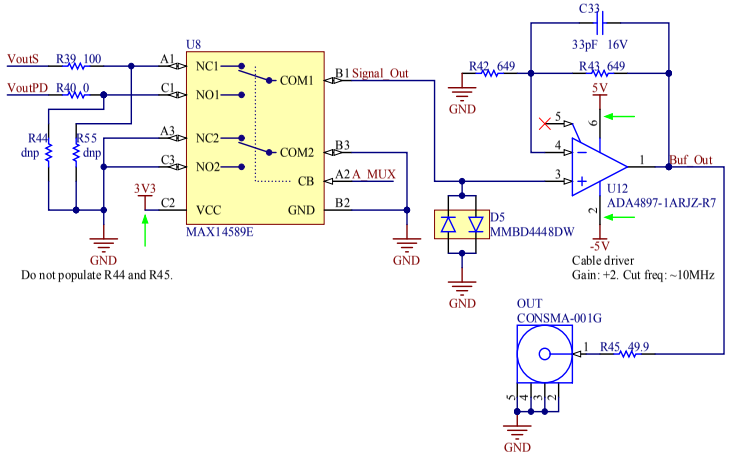




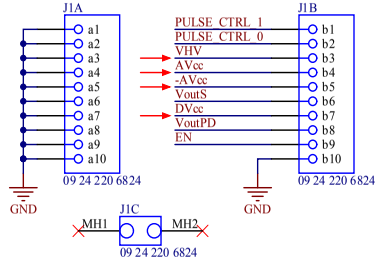
Title: **Off-Board Connectors**			
Organization: **USCND**	Project: **Prototype Backplane**		
Version: 0.7	Revision: Initial	Date: 5/23/2014	
Author: P. Giannelli	Approved By: L. Capineri		
File name: Off-Board_Connectors.SchDoc	Sheet: 2 of 9		

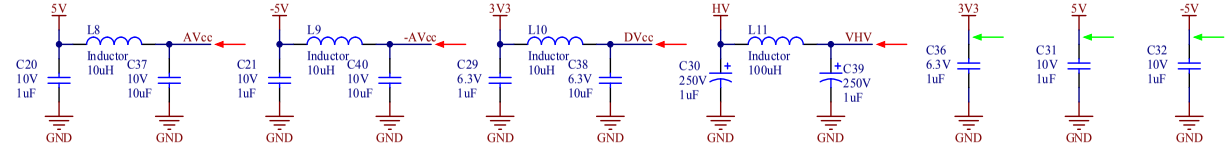
This schematic uses the Front-End's original net naming. Upper level schematics use the backplane's own naming.

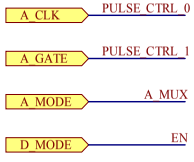
Analog Output Mux + Cable Driver

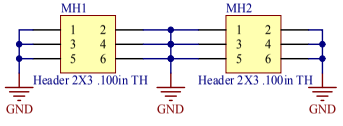


Front-End Connector

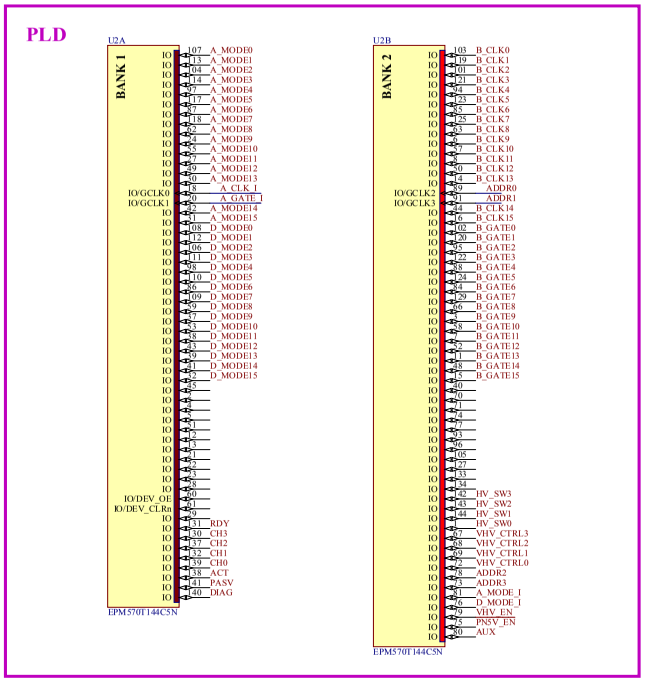


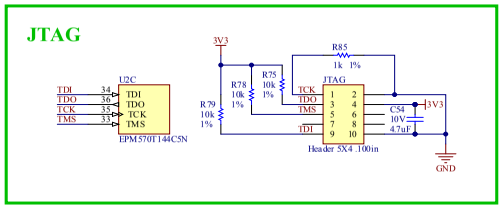


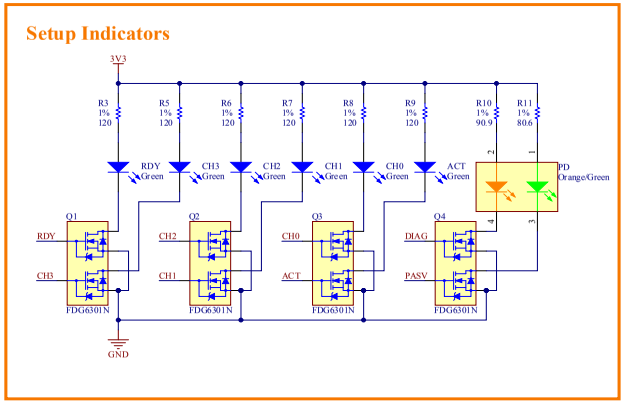


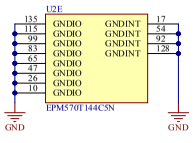


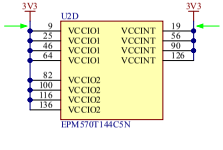
Title: **Daughter Card Slot**			
Organization: **USCND**	Project: **Prototype Backplane**		
Version: 0.7	Revision: Initial	Date: 5/23/2014	
Author: P. Giannelli	Approved By: L. Capineri		
File name: Daughter_Card_Slot.SchDoc	Sheet: 3 of 9		

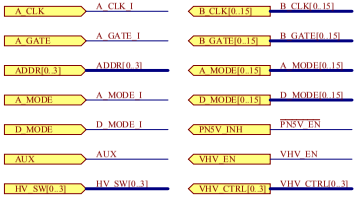


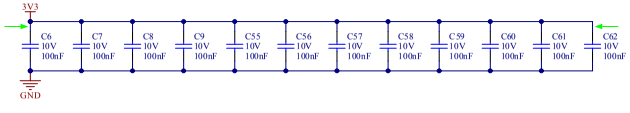






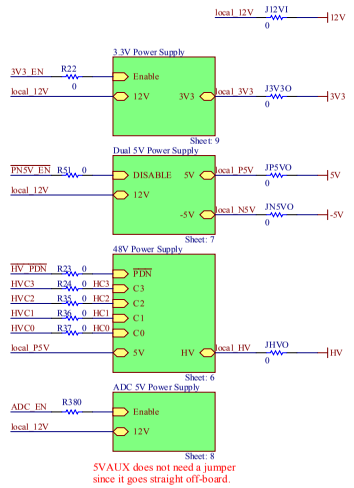






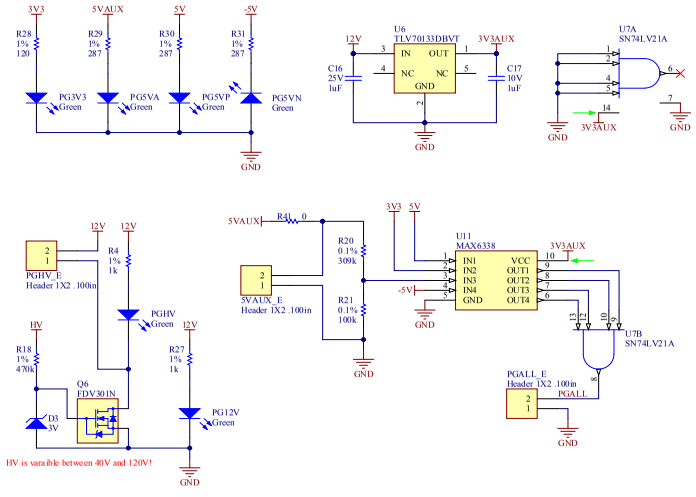
Title:	Master System Controller		
Organization: USCND	Project: Prototype Backplane		
Version: 0.7	Revision: Initial	Date: 5/23/2014	
Author: P. Giannelli	Approved By: L. Capineri		
File name: Master System Controller.SchDoc	Sheet: 4 of 9		

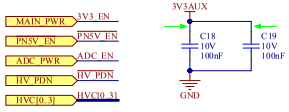
Power Converters



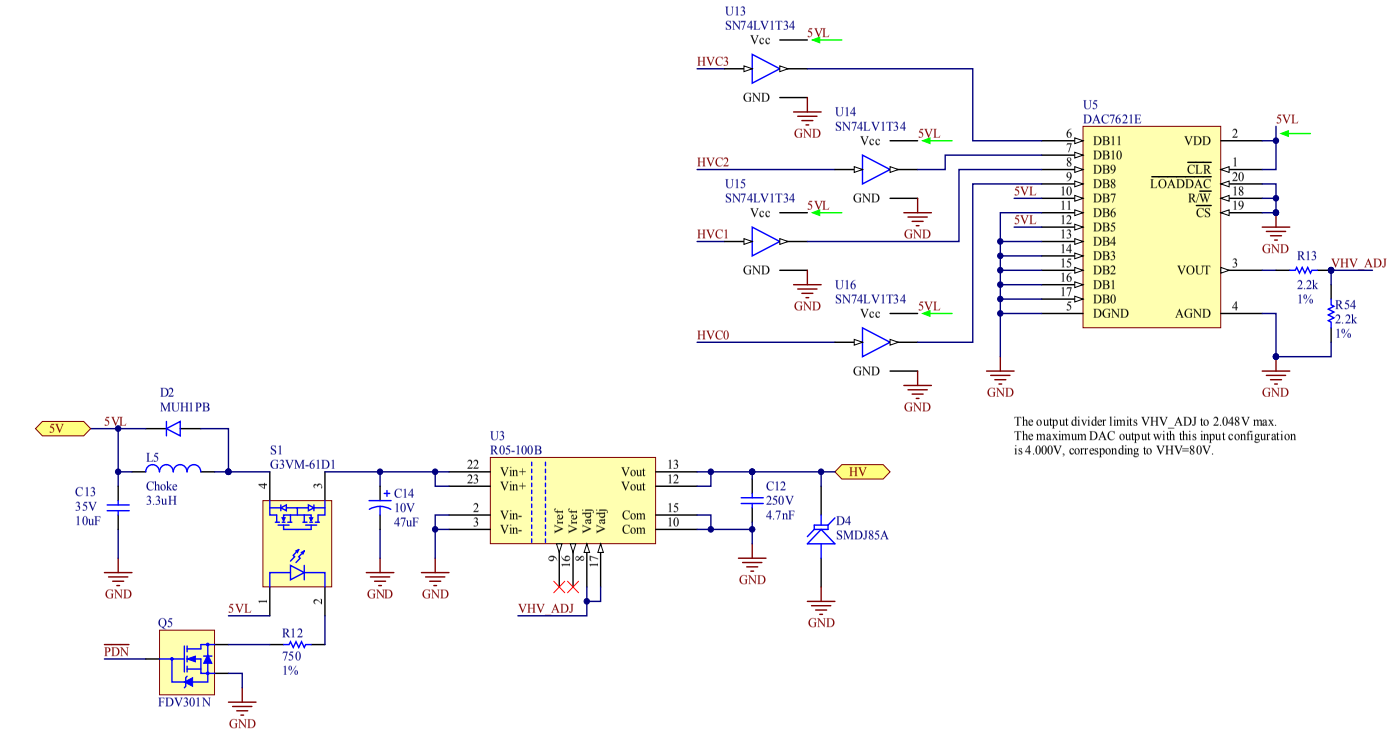
5VAUX does not need a jumper since it goes straight off-board.

Power Diagnostics

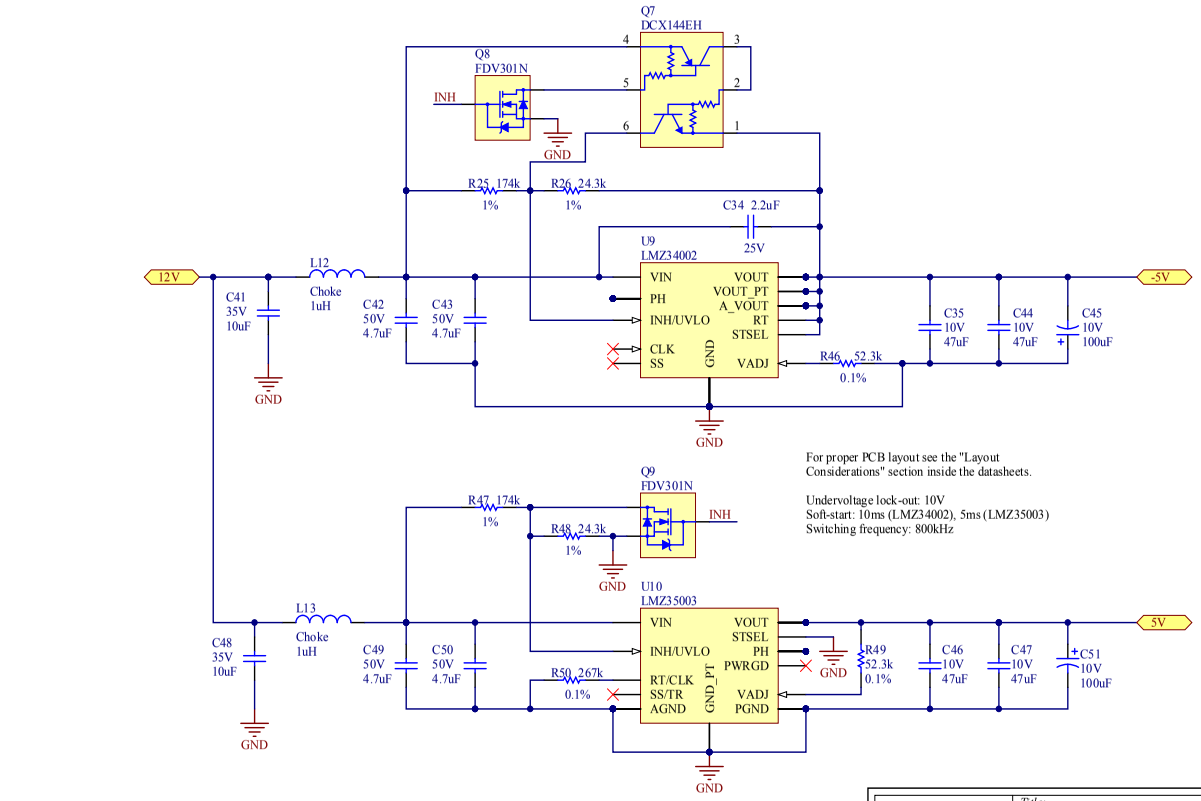




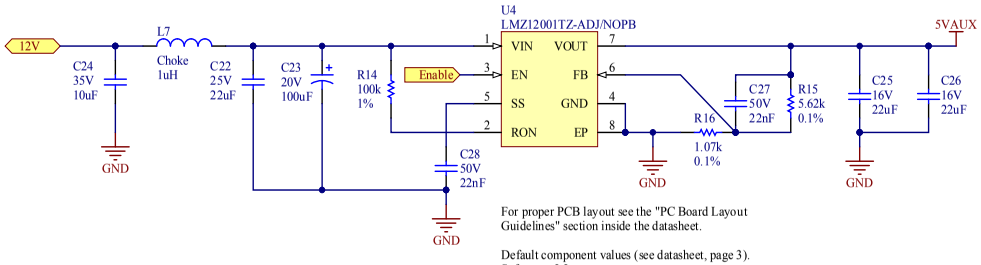
Title:	Power Section		
Organization: USCND		Project: Prototype Backplane	
Version: 0.7		Revision: Initial	Date: 5/23/2014
Author: P. Giannelli		Approved By: L. Capineri	
File name: Power_Section.SchDoc		Sheet: 5 of 9	



Title:	48V RECOM Power Stage		
Organization: USCND	Project: Prototype Backplane		
Version: 0.7	Revision: Initial	Date: 5/23/2014	
Author: P. Giannelli	Approved By: L. Capineri		
File name: 48V_RECOM.SchDoc	Sheet: 6 of 9		



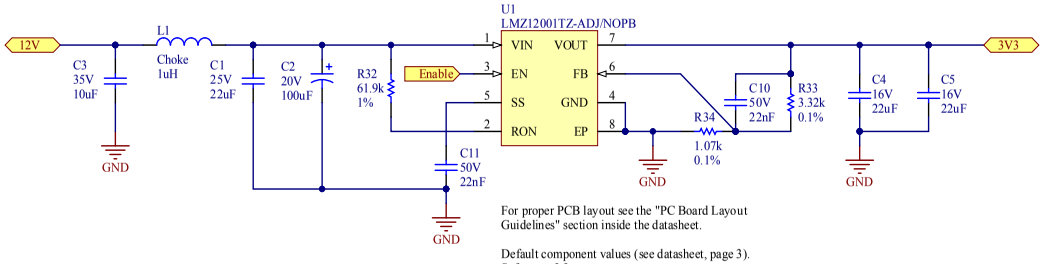
Title:	**Dual ±5V Power Supply**
Organization: **USCND**	Project: **Prototype Backplane**
Version: 0.7	Revision: Initial / Date: 5/23/2014
Author: P. Giannelli	Approved By: L. Capineri
File name: Dual_5V_Supply.SchDoc	Sheet: 7 of 9



For proper PCB layout see the "PC Board Layout Guidelines" section inside the datasheet.

Default component values (see datasheet, page 3).
Soft-start: 2.2ms
Switching frequency: 380kHz

Title:	**ADC 5V Power Supply**		
Organization: **USCND**	Project: **Prototype Backplane**		
Version: 0.7	Revision: Initial	Date: 5/23/2014	
Author: P. Giannelli	Approved By: L. Capineri		
File name: ADC_5V_Supply.SchDoc	Sheet: 8 of 9		

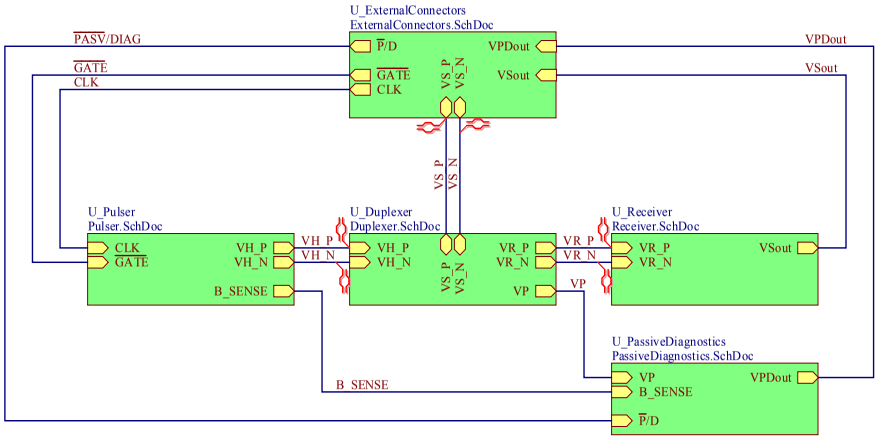


For proper PCB layout see the "PC Board Layout Guidelines" section inside the datasheet.

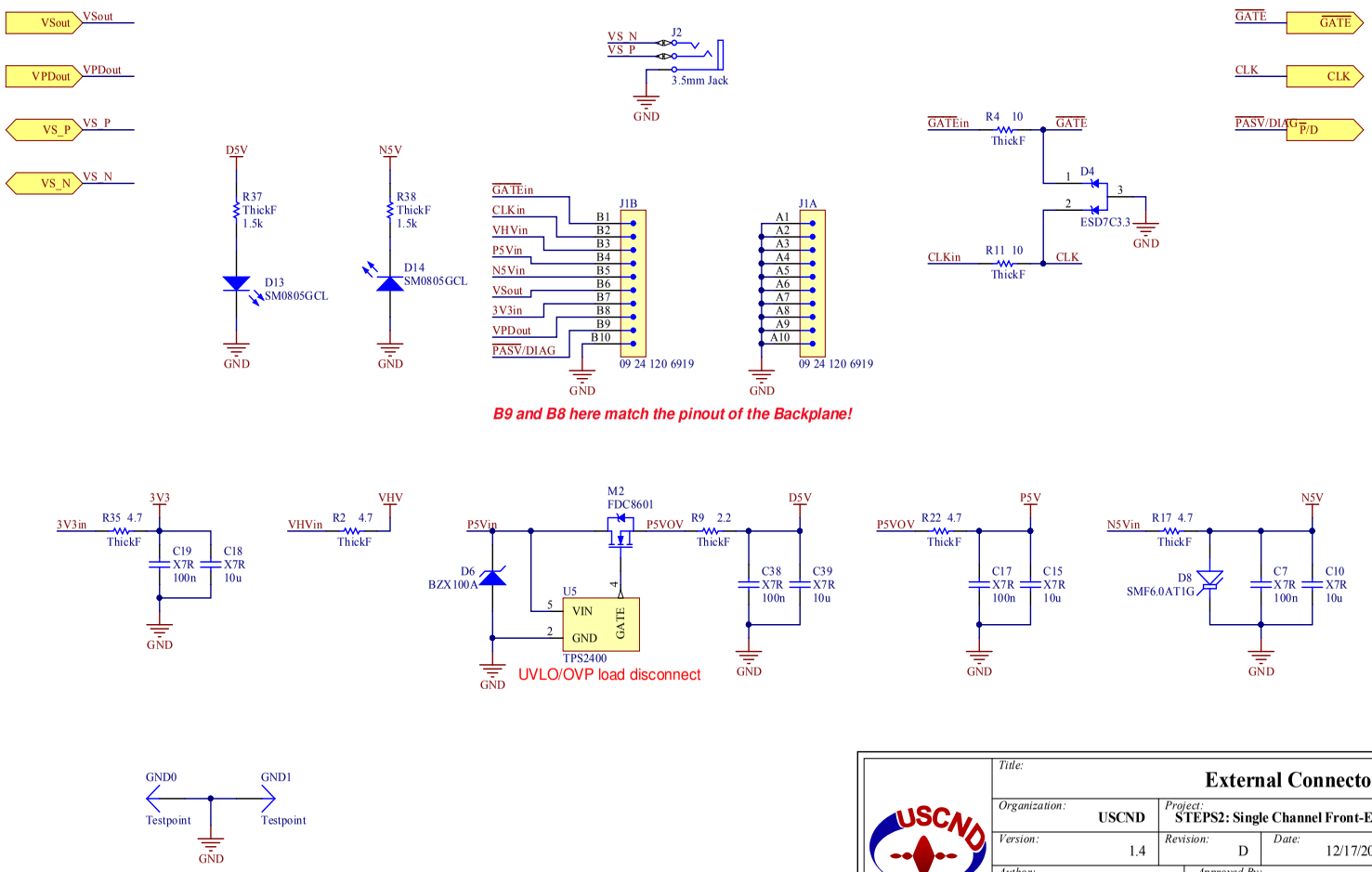
Default component values (see datasheet, page 3).
Soft-start: 2.2ms
Switching frequency: 620kHz

Title:	**3.3V Power Supply**		
Organization: **USCND**	Project: **Prototype Backplane**		
Version: 0.7	Revision: Initial	Date: 5/23/2014	
Author: P. Giannelli	Approved By: L. Capineri		
File name: 3V3_Main_Supply.SchDoc	Sheet: 9 of 9		

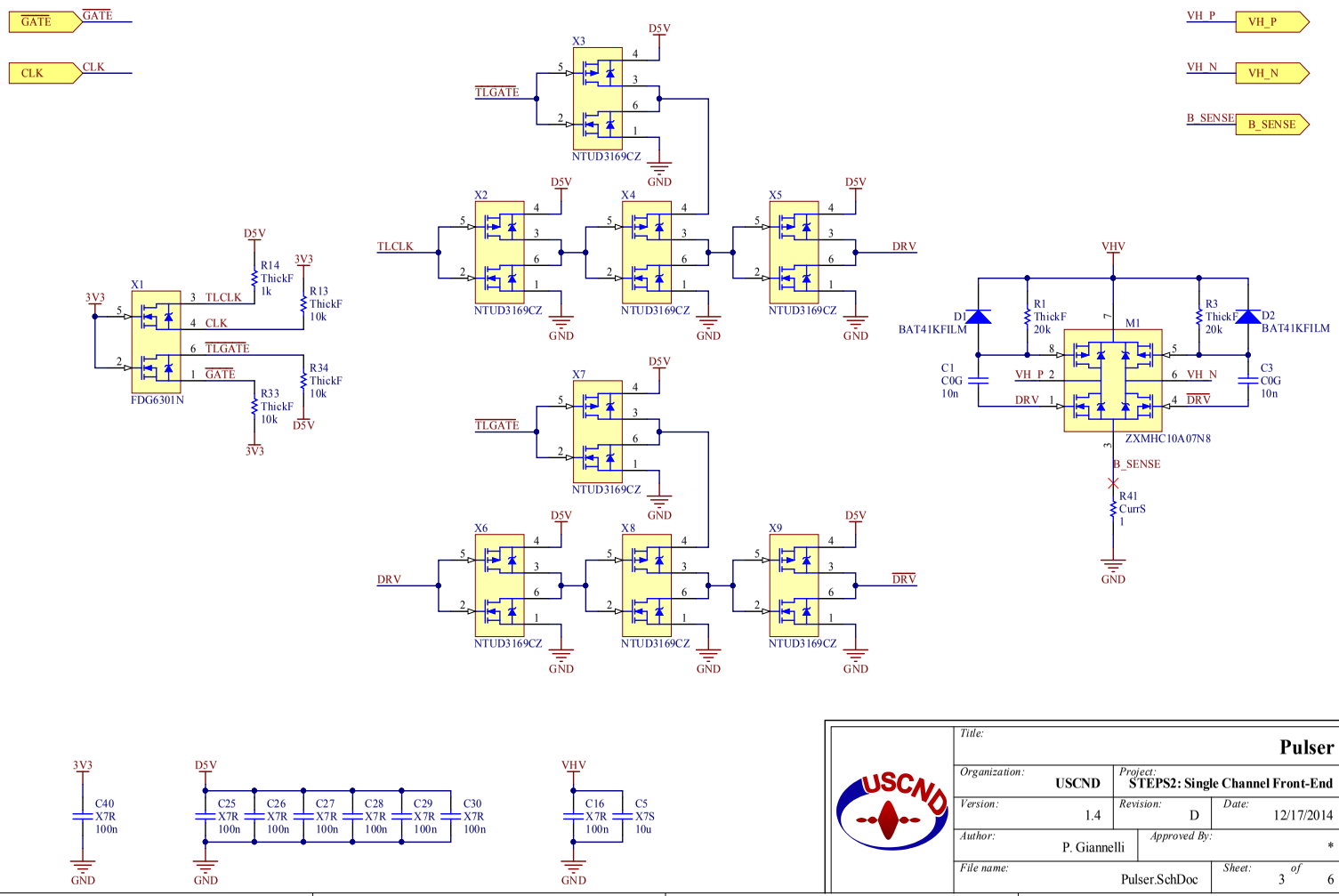
ANALOG FRONT-END



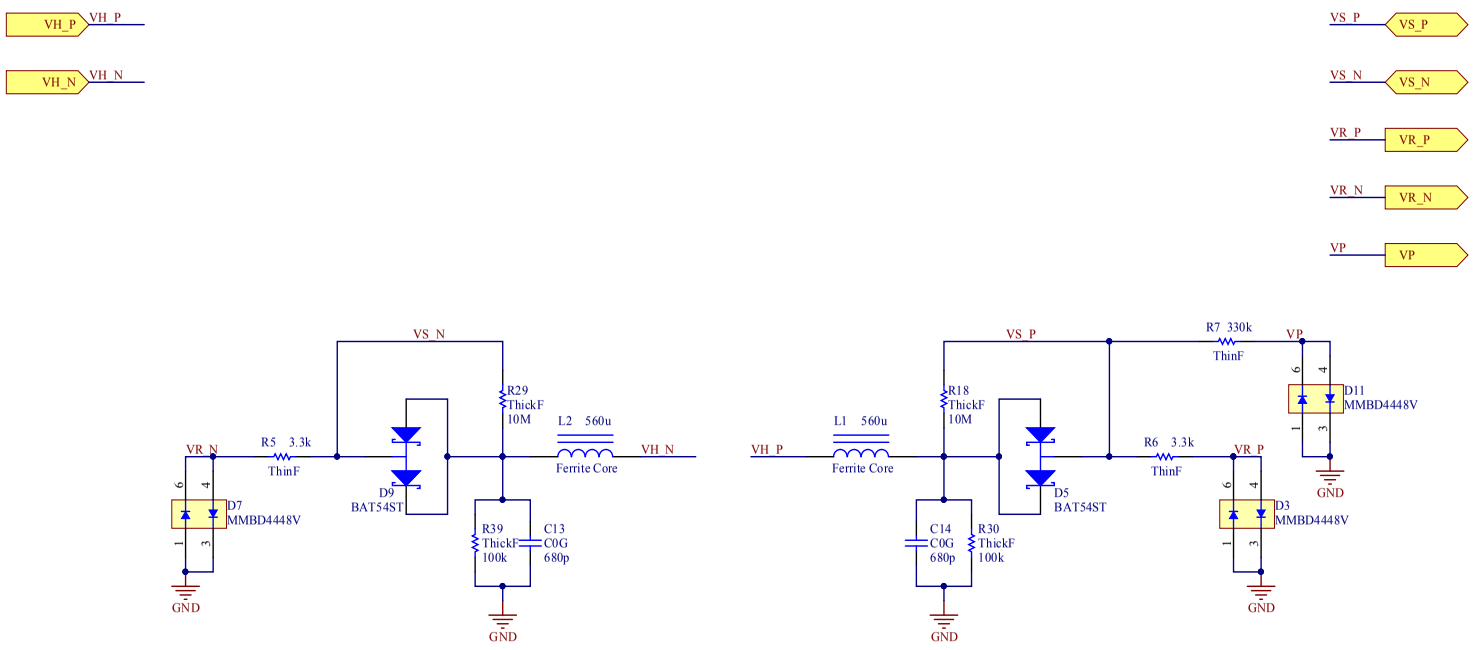
Title:	**Top Level Schematic**
Organization: **USCND**	Project: **STEPS2: Single Channel Front-End**
Version: 1.4	Revision: D — Date: 12/17/2014
Author: P. Giannelli	Approved By: *
File name: TopLevelSchematic.SchDoc	Sheet: 1 of 6



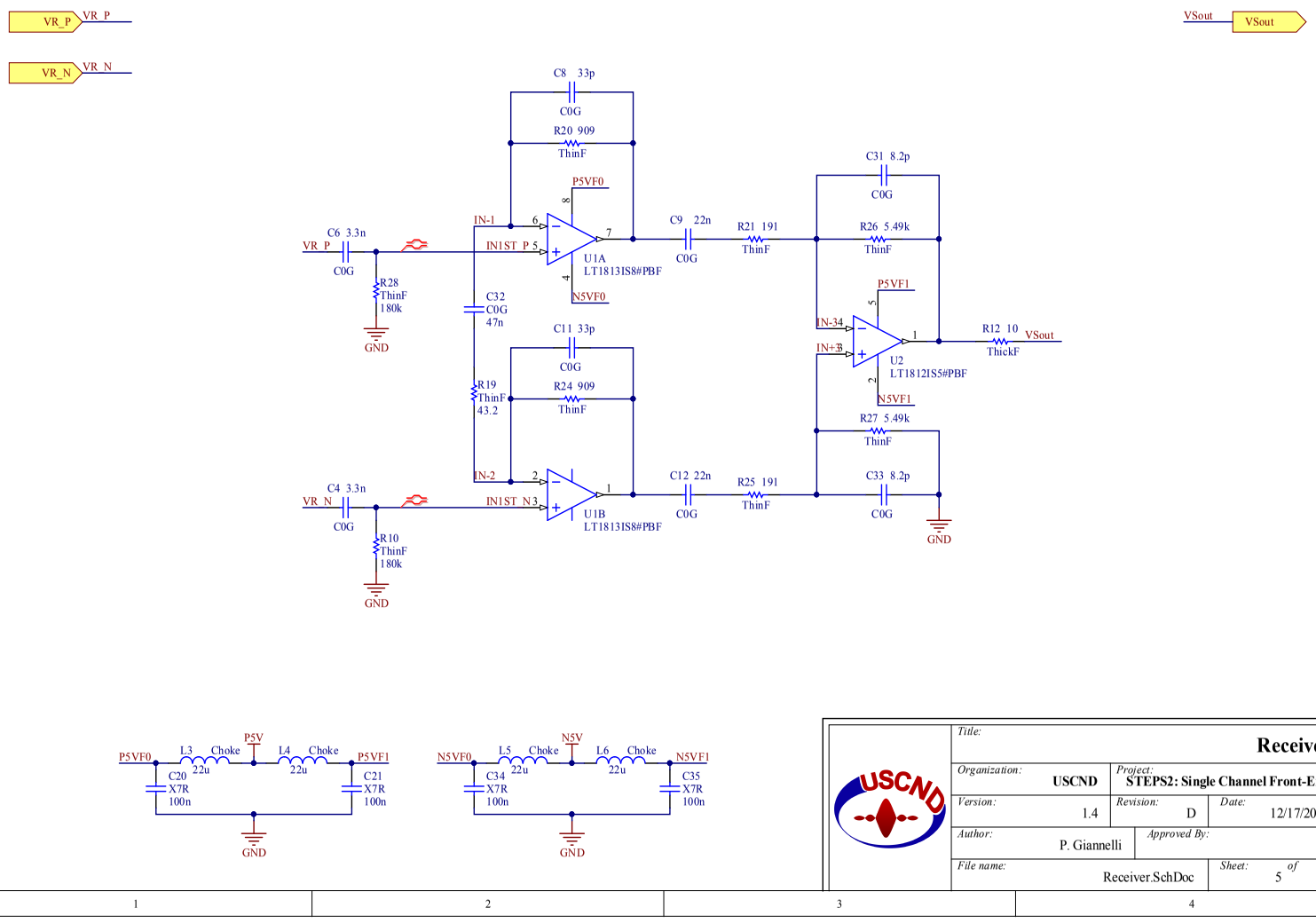
Title:	**External Connectors**
Organization: USCND	Project: STEPS2: Single Channel Front-End
Version: 1.4	Revision: D — Date: 12/17/2014
Author: P. Giannelli	Approved By: *
File name: ExternalConnectors.SchDoc	Sheet: 2 of 6



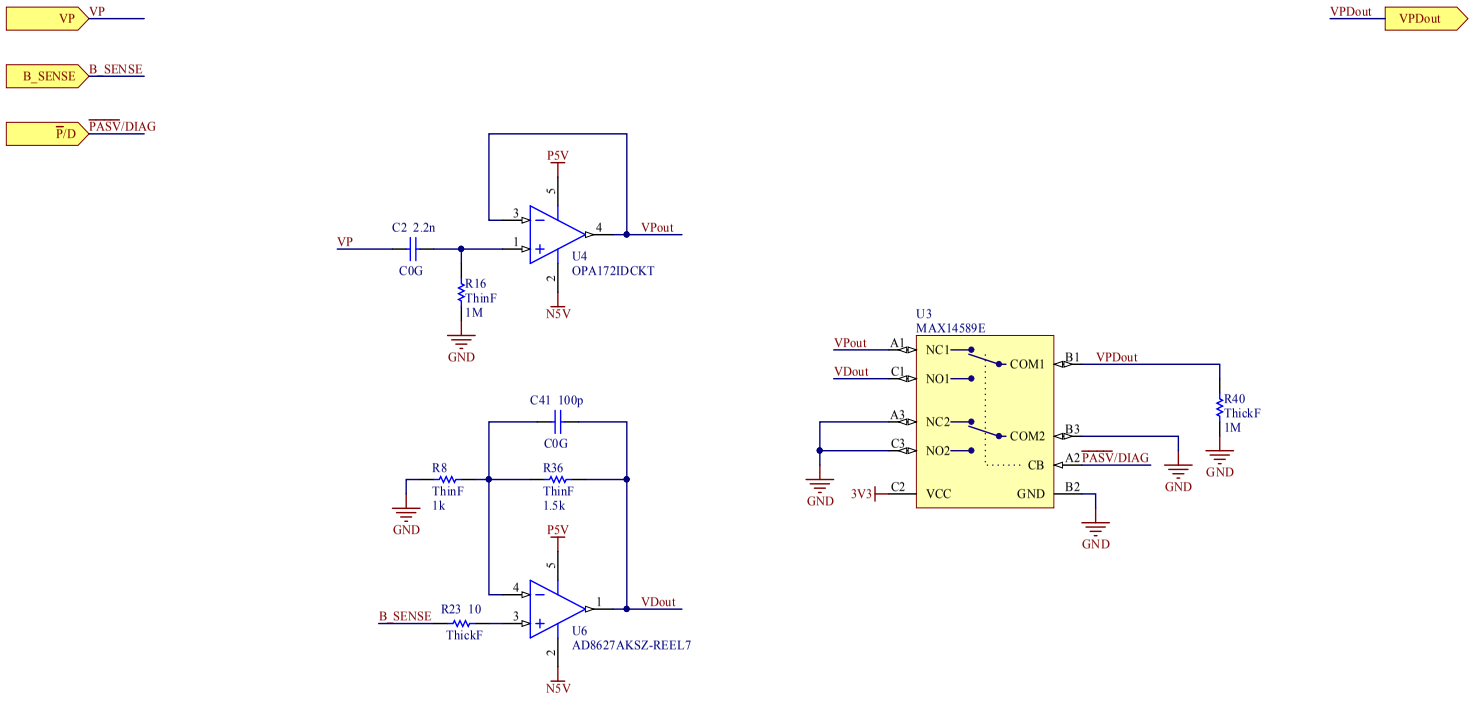
Title:	**Pulser**		
Organization: **USCND**	Project: **STEPS2: Single Channel Front-End**		
Version: 1.4	Revision: D	Date: 12/17/2014	
Author: P. Giannelli	Approved By: *		
File name: Pulser.SchDoc	Sheet: 3 of 6		



Title:	**Duplexer**		
Organization: **USCND**	Project: **STEPS2: Single Channel Front-End**		
Version: 1.4	Revision: D	Date: 12/17/2014	
Author: P. Giannelli	Approved By: *		
File name: Duplexer.SchDoc	Sheet: 4 of 6		



Title:	**Receiver**		
Organization: **USCND**	Project: **STEPS2: Single Channel Front-End**		
Version: 1.4	Revision: D	Date: 12/17/2014	
Author: P. Giannelli	Approved By: *		
File name: Receiver.SchDoc	Sheet: 5 of 6		

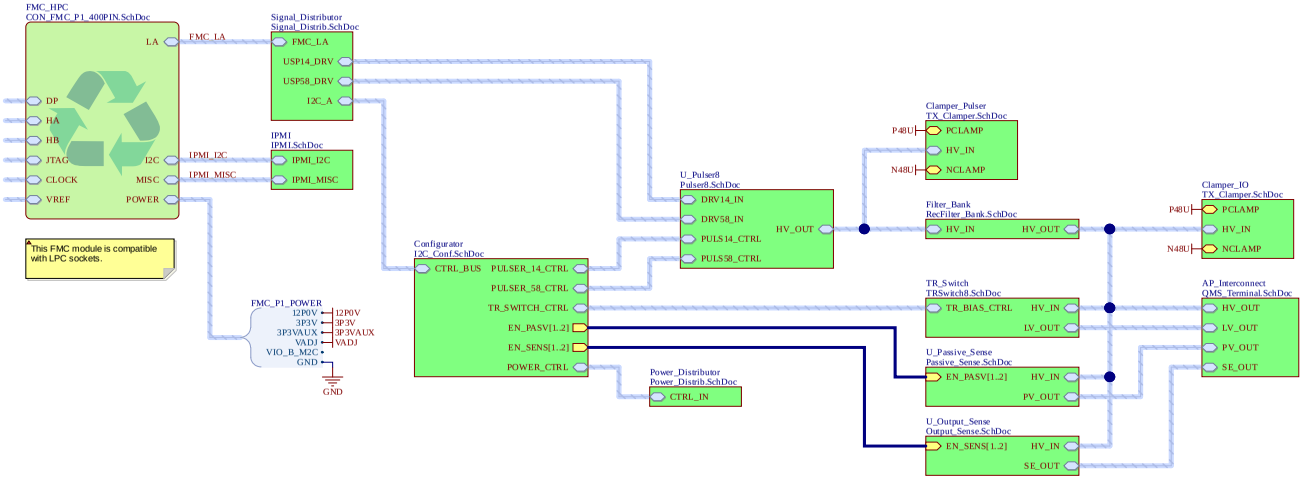


Title:	**Passive and Diagnostics**		
Organization: **USCND**	Project: **STEPS2: Single Channel Front-End**		
Version: 1.4	Revision: D	Date: 12/17/2014	
Author: P. Giannelli	Approved By: *		
File name: PassiveDiagnostics.SchDoc	Sheet: 6 of 6		

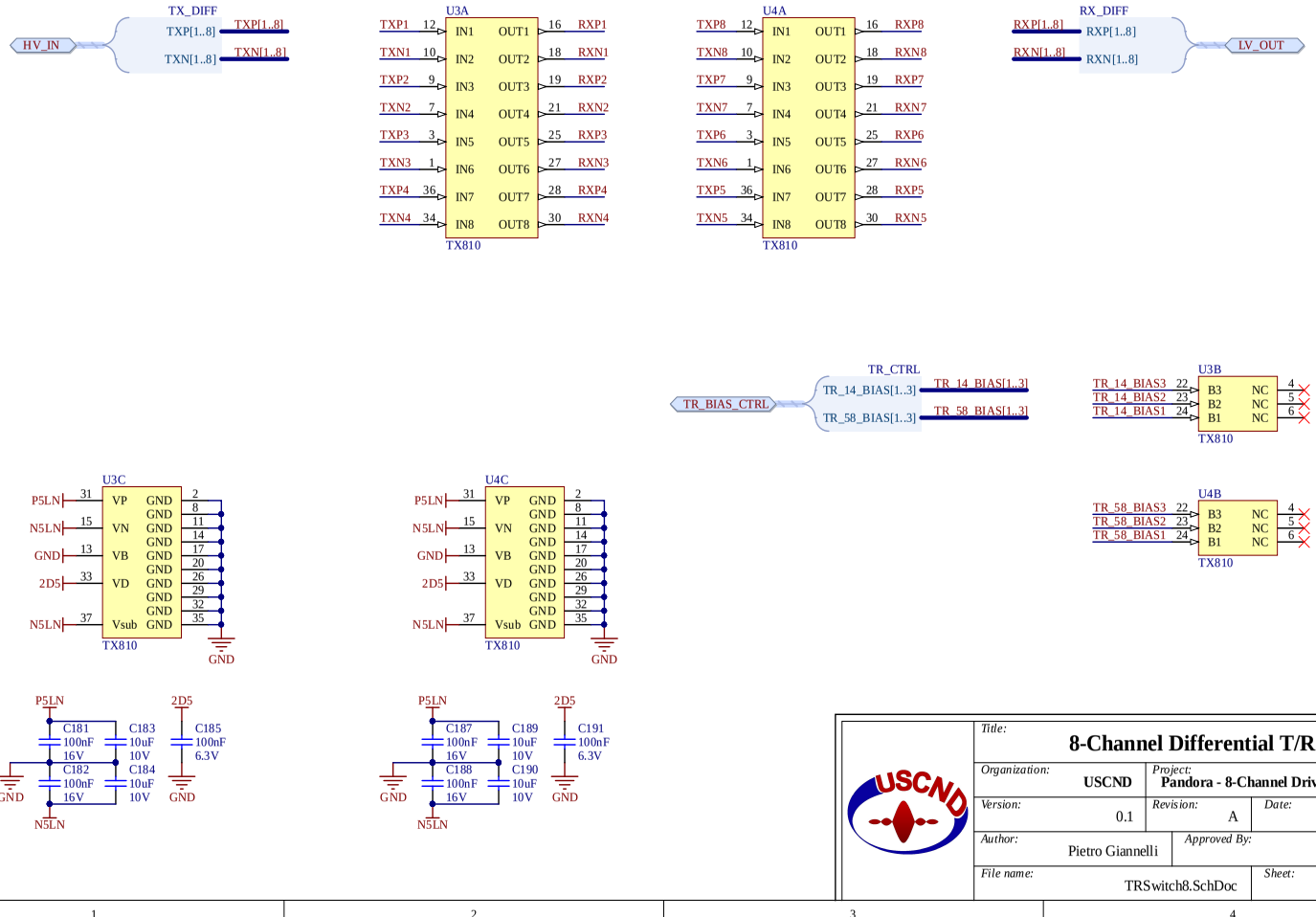
B

PANDORA ELECTRICAL SCHEMATICS

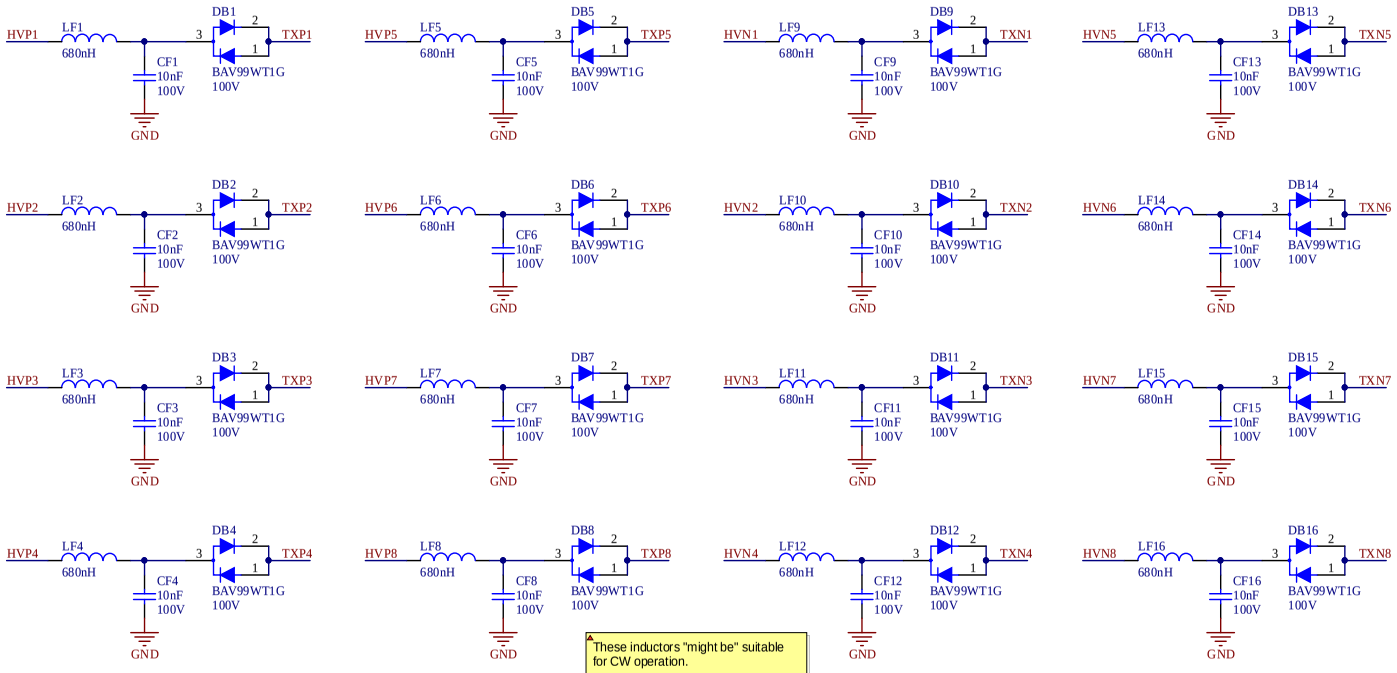
TRANSDUCER DRIVER MODULE



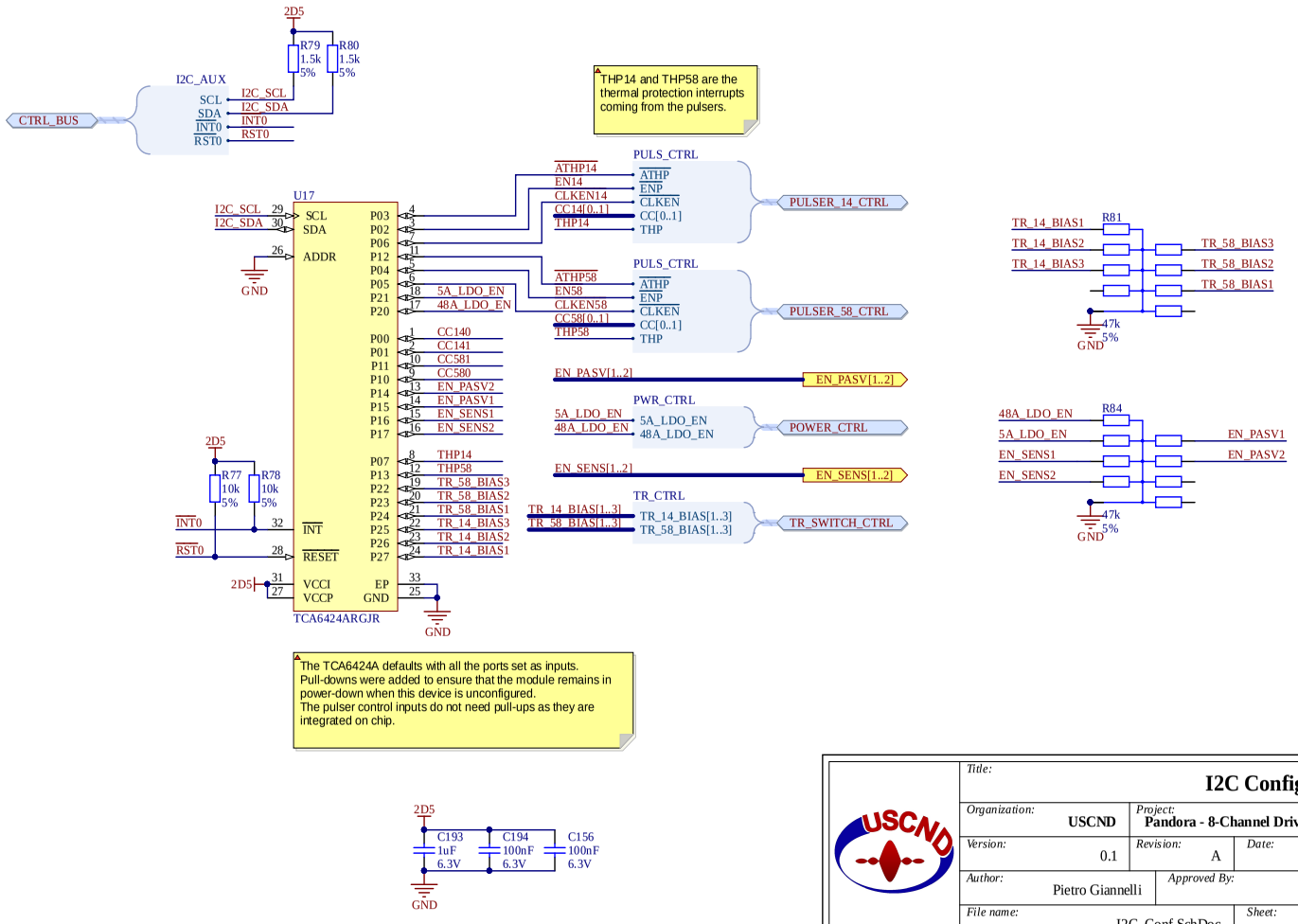
Title:	**Root Schematic**		
Organization: **USCND**	Project: **Pandora - 8-Channel Driver Module**		
Version: 0.1	Revision: A	Date: 05/10/2017	
Author: Pietro Giannelli	Approved By: *		
File name: Root_Schematic.SchDoc	Sheet: 1 of 13		



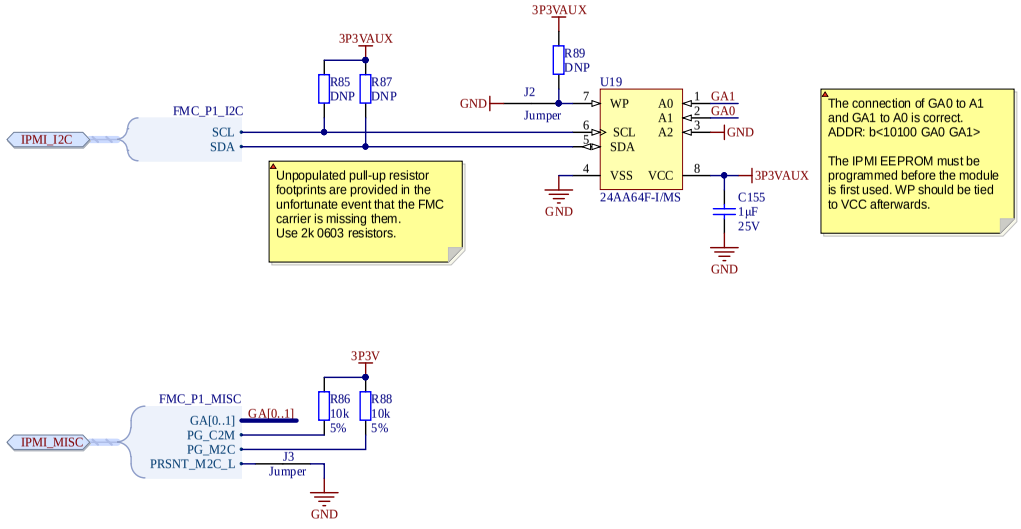
Title:	**8-Channel Differential T/R Switch**
Organization: **USCND**	Project: **Pandora - 8-Channel Driver Module**
Version: 0.1	Revision: A — Date: 05/10/2017
Author: Pietro Giannelli	Approved By: *
File name: TRSwitch8.SchDoc	Sheet: 2 of 13



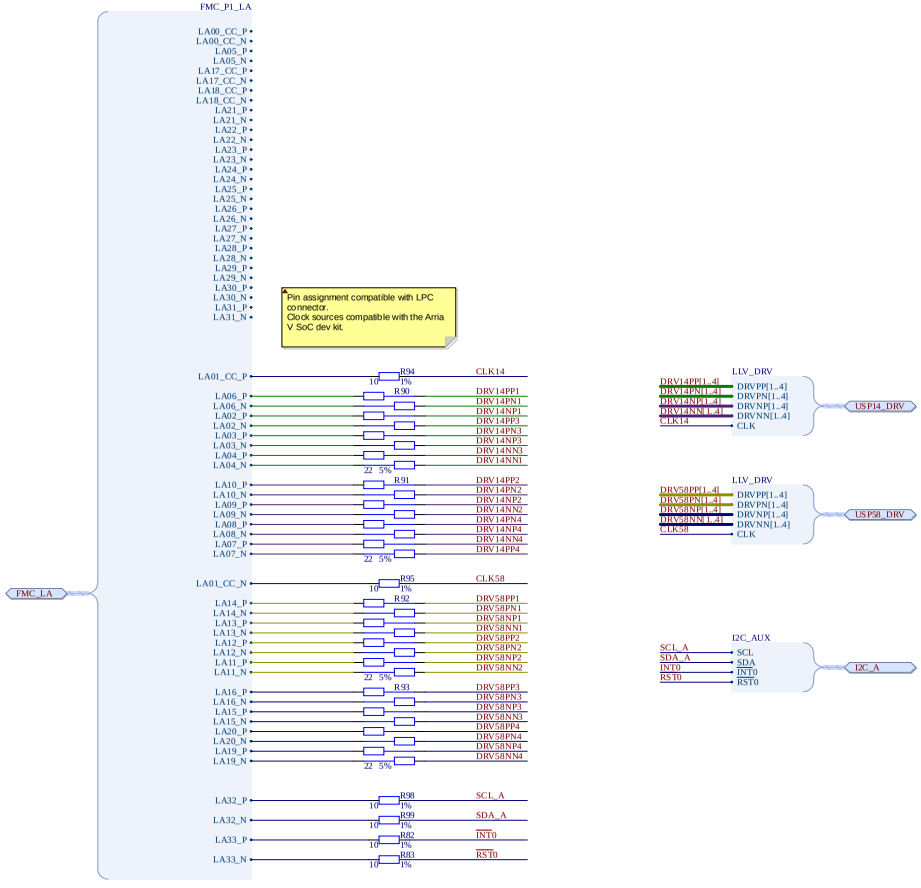
Title:	**Reconstruction Filter Bank**		
Organization: **USCND**	Project: **Pandora - 8-Channel Driver Module**		
Version: 0.1	Revision: A	Date: 05/10/2017	
Author: Pietro Giannelli	Approved By: *		
File name: RecFilter_Bank.SchDoc	Sheet: 3 of 13		



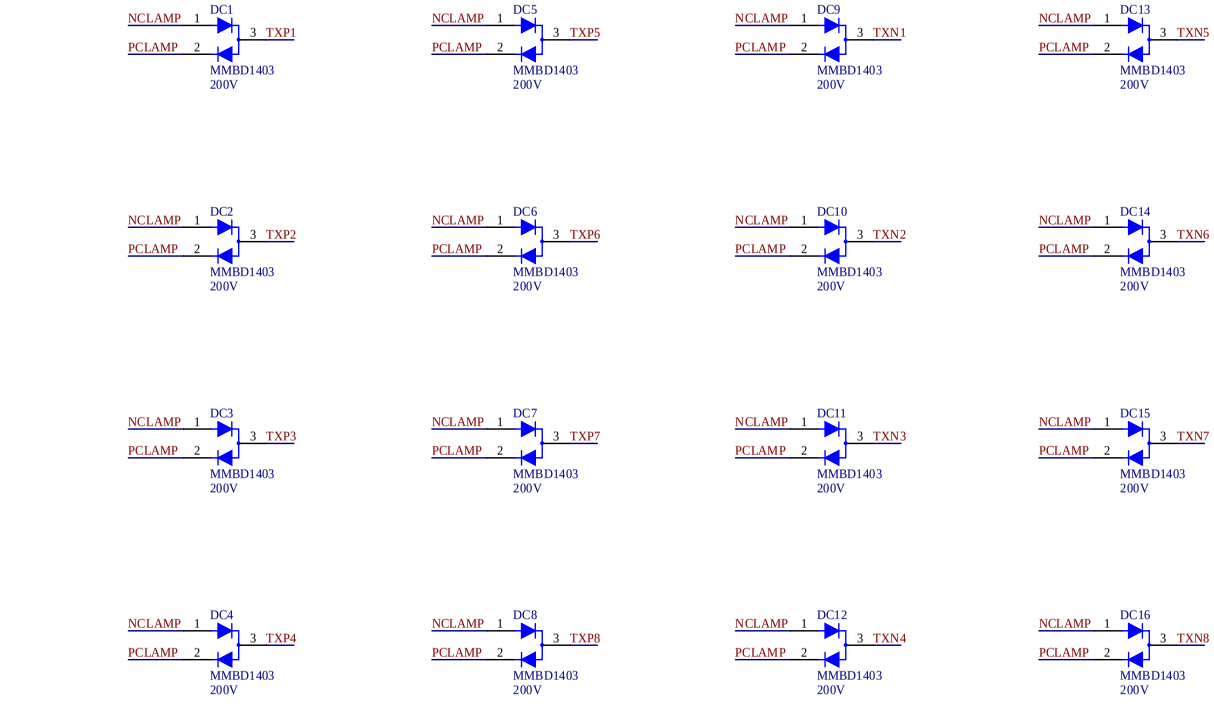
Title:	**I2C Configurator**
Organization: **USCND**	Project: **Pandora - 8-Channel Driver Module**
Version: 0.1	Revision: A — Date: 05/10/2017
Author: Pietro Giannelli	Approved By: *
File name: I2C_Conf.SchDoc	Sheet: 4 of 13



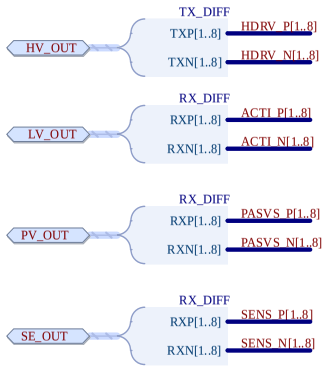
Title: **IPMI**			
Organization: **USCND**	Project: **Pandora - 8-Channel Driver Module**		
Version: 0.1	Revision: A	Date: 05/10/2017	
Author: Pietro Giannelli	Approved By: *		
File name: IPMI.SchDoc	Sheet: 5 of 13		

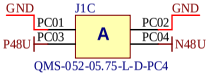


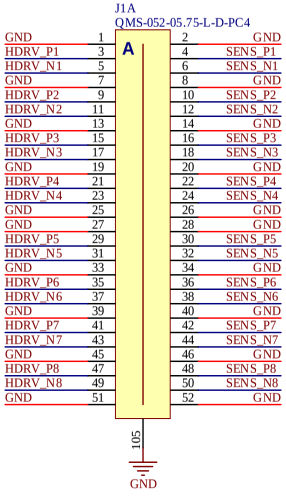
Title:	**FMC Signal Distributor**		
Organization: **USCND**	Project: **Pandora - 8-Channel Driver Module**		
Version: 0.1	Revision: A	Date: 05/10/2017	
Author: Pietro Giannelli	Approved By: *		
File name: Signal_Distrib.SchDoc	Sheet: 6 of 13		

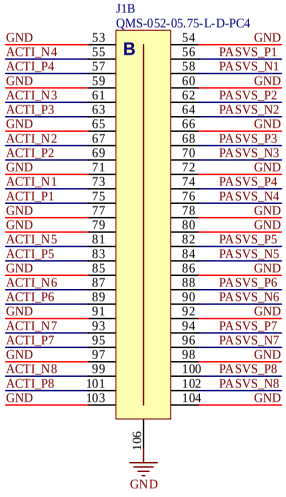


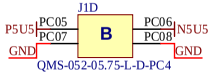
Title:	**Protection Clamps**		
Organization: **USCND**	Project: **Pandora - 8-Channel Driver Module**		
Version: 0.1	Revision: A	Date: 05/10/2017	
Author: Pietro Giannelli	Approved By: *		
File name: TX_Clamper.SchDoc	Sheet: 7 of 13		



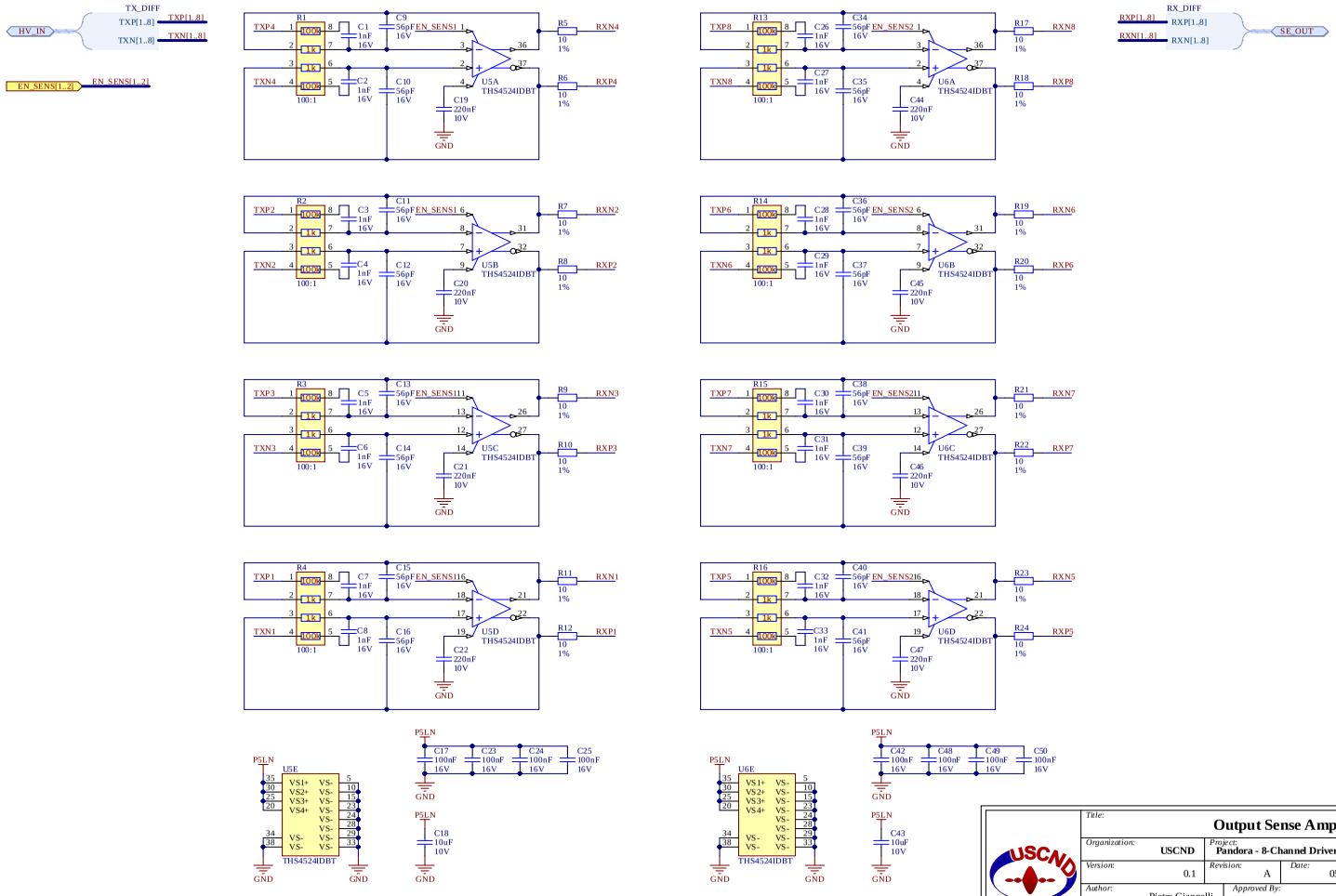


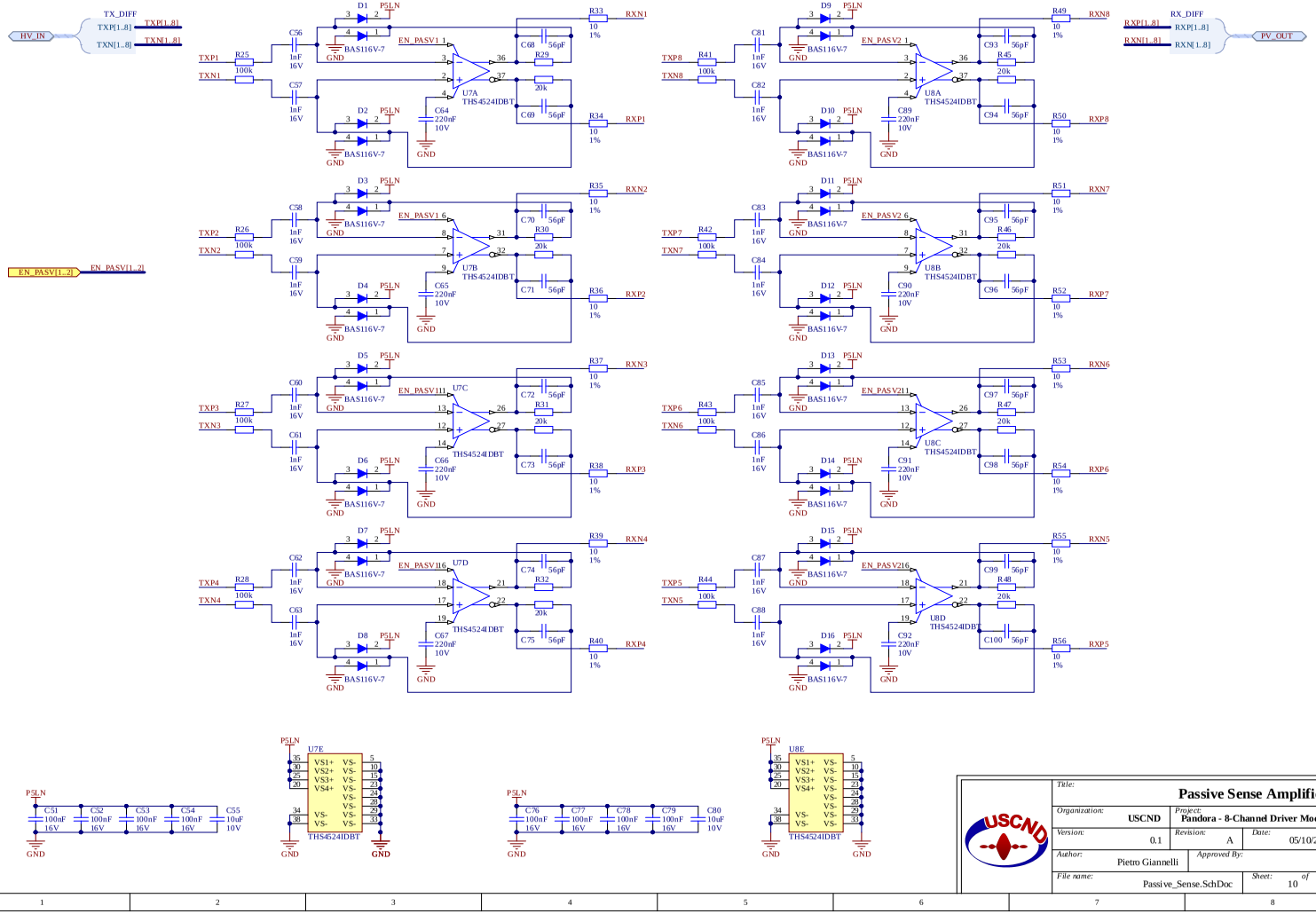




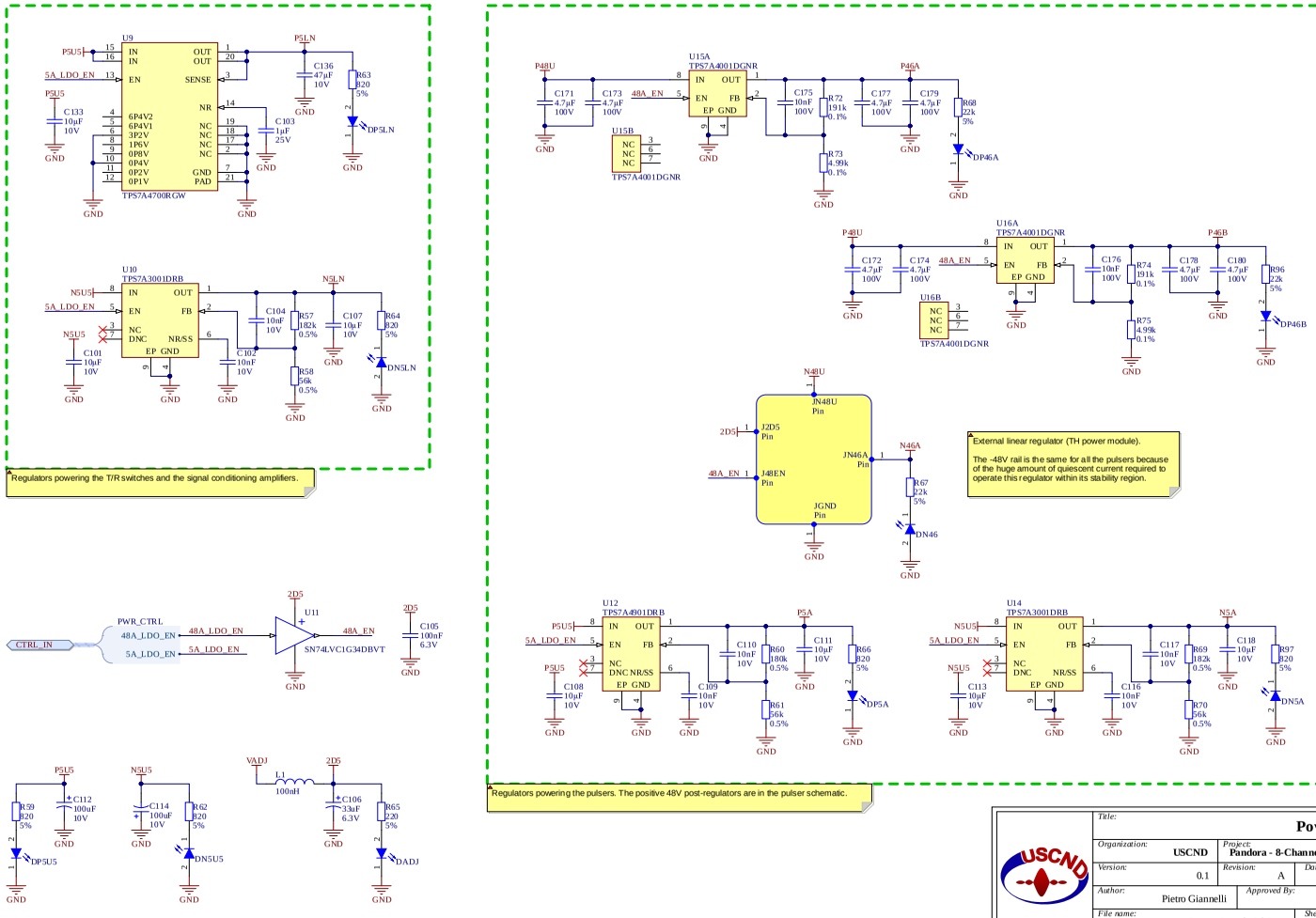


Title: **QMS Terminal**			
Organization: **USCND**	Project: **Pandora - 8-Channel Driver Module**		
Version: 0.1	Revision: A	Date: 05/10/2017	
Author: Pietro Giannelli	Approved By: *		
File name: QMS_Terminal.SchDoc	Sheet: 8 of 13		

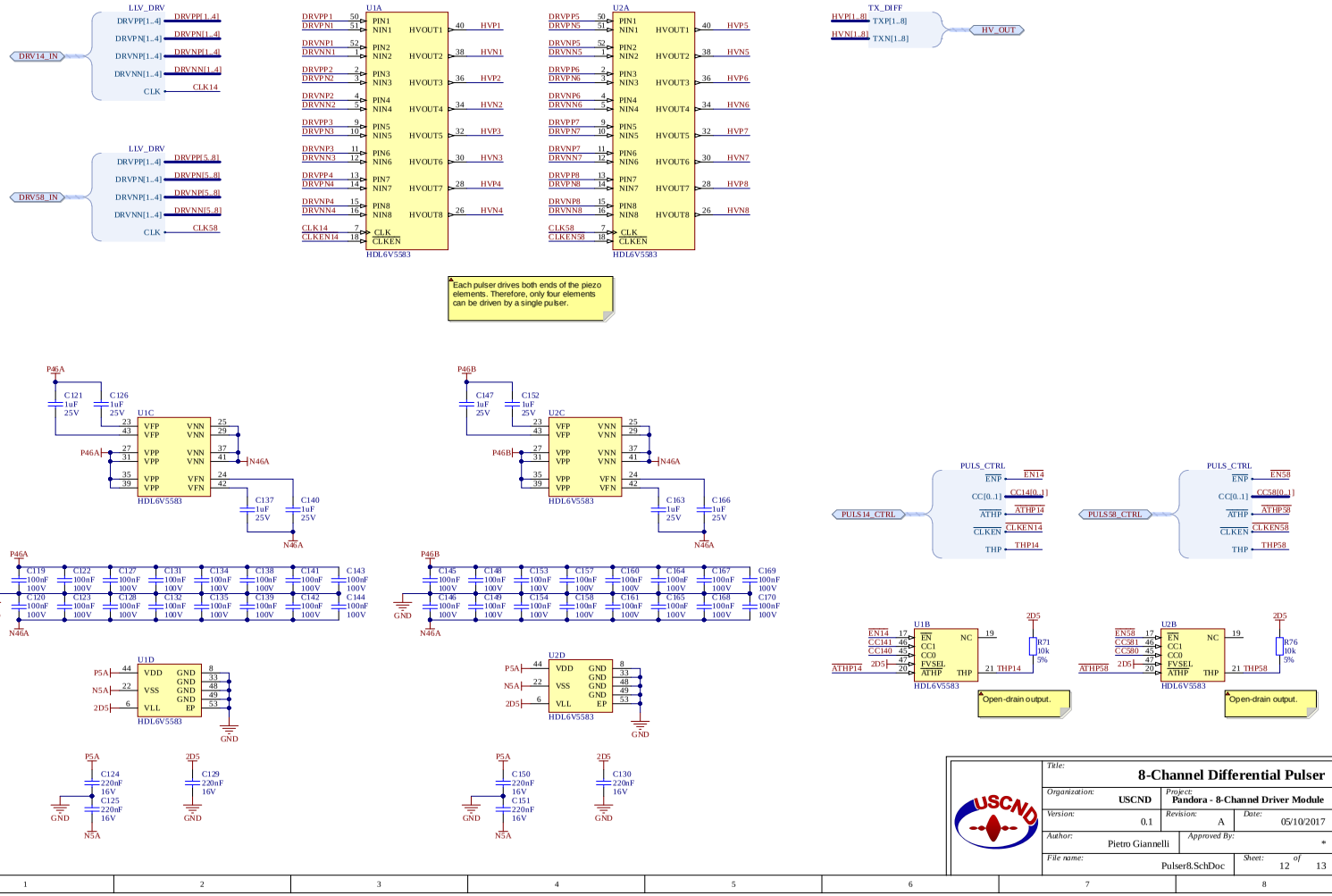

TX_DIFF
HV_IN
TXP[1..8]
TXN[1..8]
TXP[1..8]
TXN[1..8]
EN_SENS[1..2]
EN_SENS[1..2]
RX_DIFF
RXP[1..8]
RXN[1..8]
SE_OUT
R1
R2
R3
R4
R13
R14
R15
R16
100R
1K
100:1
C1
C2
C3
C4
C5
C6
C7
C8
C26
C27
C28
C29
C30
C31
C32
C33
1nF
16V
C9
C10
C11
C12
C13
C14
C15
C16
C34
C35
C36
C37
C38
C39
C40
C41
56pF
16V
C19
C20
C21
C22
C44
C45
C46
C47
220nF
10V
EN_SENS1
EN_SENS2
EN_SENS111
EN_SENS116
EN_SENS211
EN_SENS216
U5A
U5B
U5C
U5D
U6A
U6B
U6C
U6D
THS4524IDBT
R5
R6
R7
R8
R9
R10
R11
R12
R17
R18
R19
R20
R21
R22
R23
R24
10
1%
RXN4
RXP4
RXN2
RXP2
RXN3
RXP3
RXN1
RXP1
RXN8
RXP8
RXN6
RXP6
RXN7
RXP7
RXN5
RXP5
GND
P5LN
U5E
U6E
C17
C18
C23
C24
C25
C42
C43
C48
C49
C50
100nF
10uF
VS1+
VS2+
VS3+
VS4+
VS-
Title:
Output Sense Amplifiers
Organization:
USCND
Project:
Pandora - 8-Channel Driver Module
Version:
0.1
Revision:
A
Date:
05/10/2017
Author:
Pietro Giannelli
Approved By:
*
File name:
Output_Sense.SchDoc
Sheet:
9
of
13

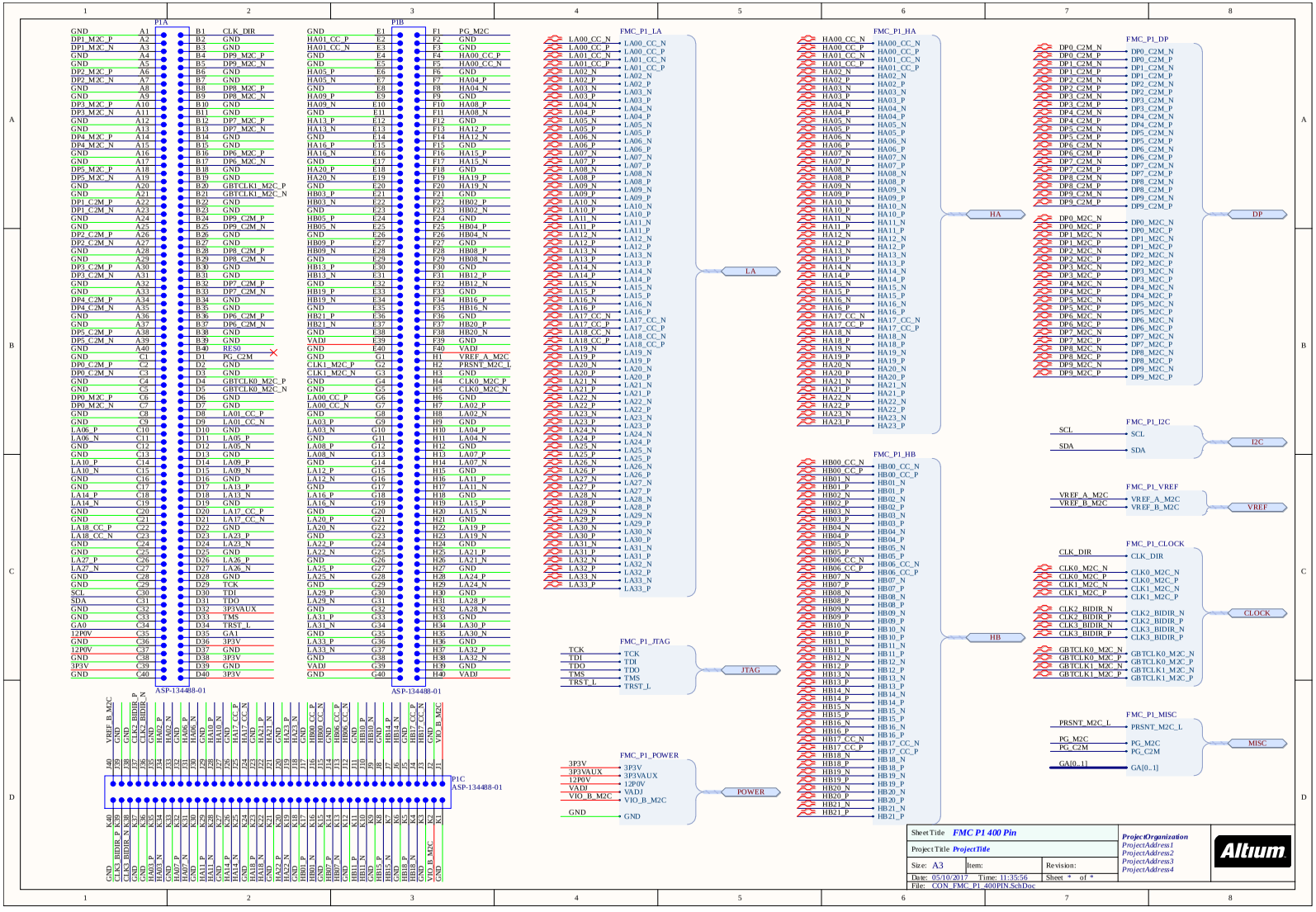


Title:	**Passive Sense Amplifiers**
Organization: **USCND**	Project: **Pandora - 8-Channel Driver Module**
Version: 0.1	Revision: A
Date: 05/10/2017	
Author: Pietro Giannelli	Approved By: *
File name: Passive_Sense.SchDoc	Sheet: 10 of 13

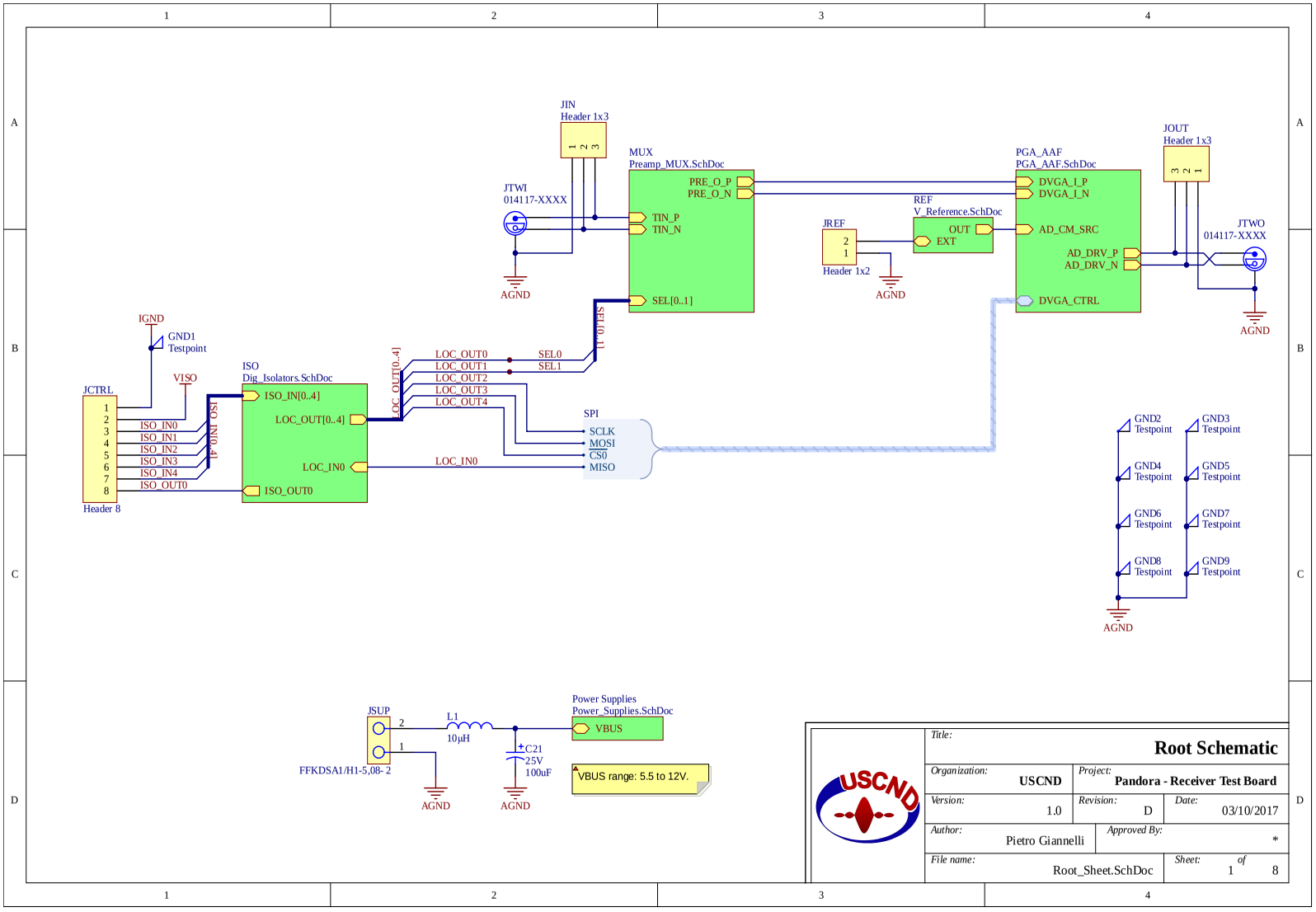


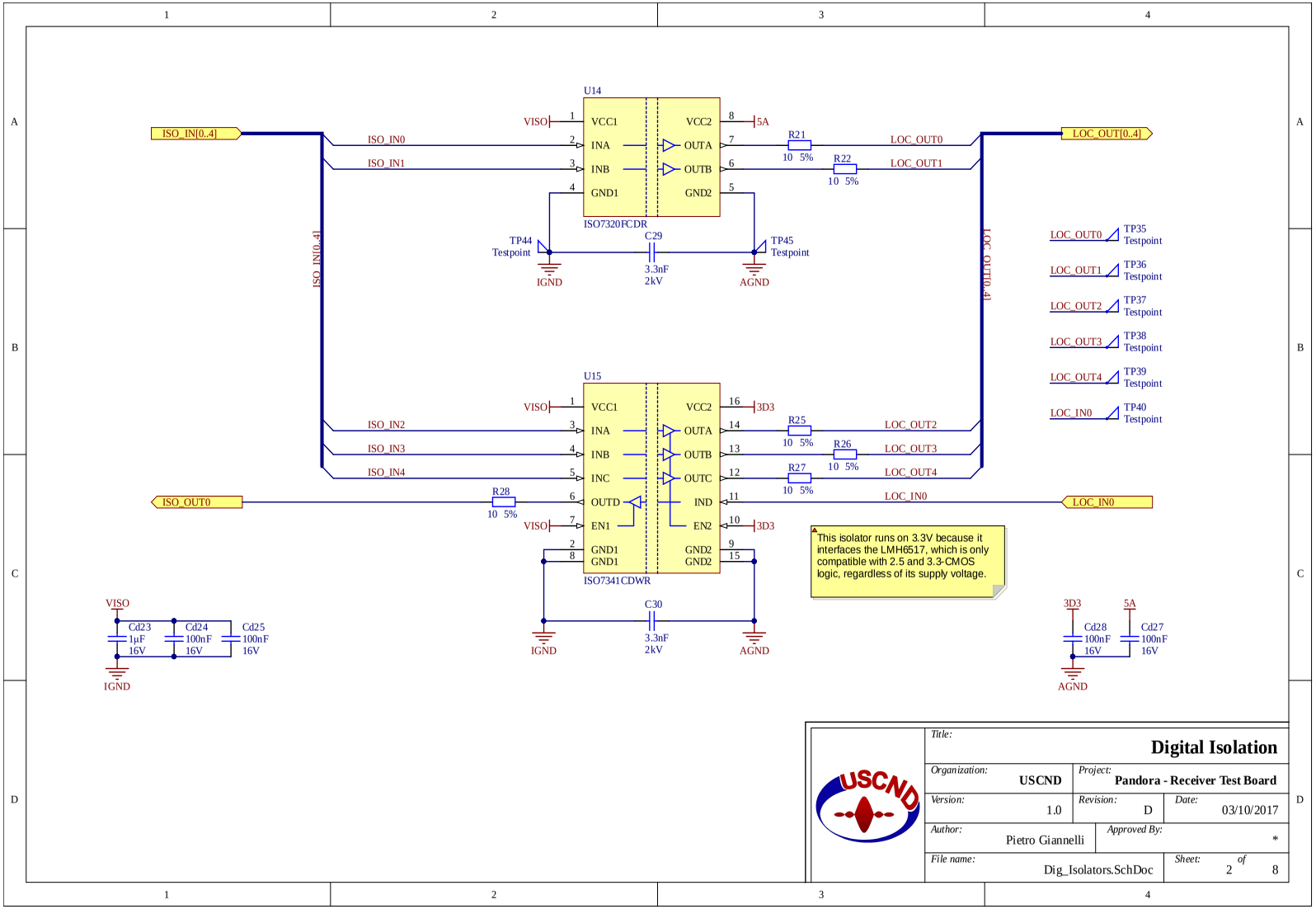
Title:	**Power Section**
Organization:	USCND
Project:	Pandora - 8-Channel Driver Module
Version:	0.1
Revision:	A
Date:	05/10/2017
Author:	Pietro Giannelli
Approved By:	*
File name:	Power_Distrib.SchDoc
Sheet:	11 of 13


LIV_DRV
DRV14_IN
DRVPP[1..4]
DRVPN[1..4]
DRVNP[1..4]
DRVNN[1..4]
CLK
CLK14
LIV_DRV
DRV58_IN
DRVPP[5..8]
DRVPN[5..8]
DRVNP[5..8]
DRVNN[5..8]
CLK58
U1A
U2A
HDL6V5583
Each pulser drives both ends of the piezo elements. Therefore, only four elements can be driven by a single pulser.
TX_DIFF
HVP[1..8]
HVN[1..8]
TXP[1..8]
TXN[1..8]
HV_OUT
P46A
P46B
U1C
U2C
N46A
GND
U1D
U2D
P5A
N5A
2D5
PULS14_CTRL
PULS58_CTRL
PULS_CTRL
U1B
U2B
Open-drain output.
8-Channel Differential Pulser
USCND
Pandora - 8-Channel Driver Module
0.1
A
05/10/2017
Pietro Giannelli
Pulser8.SchDoc
12
13

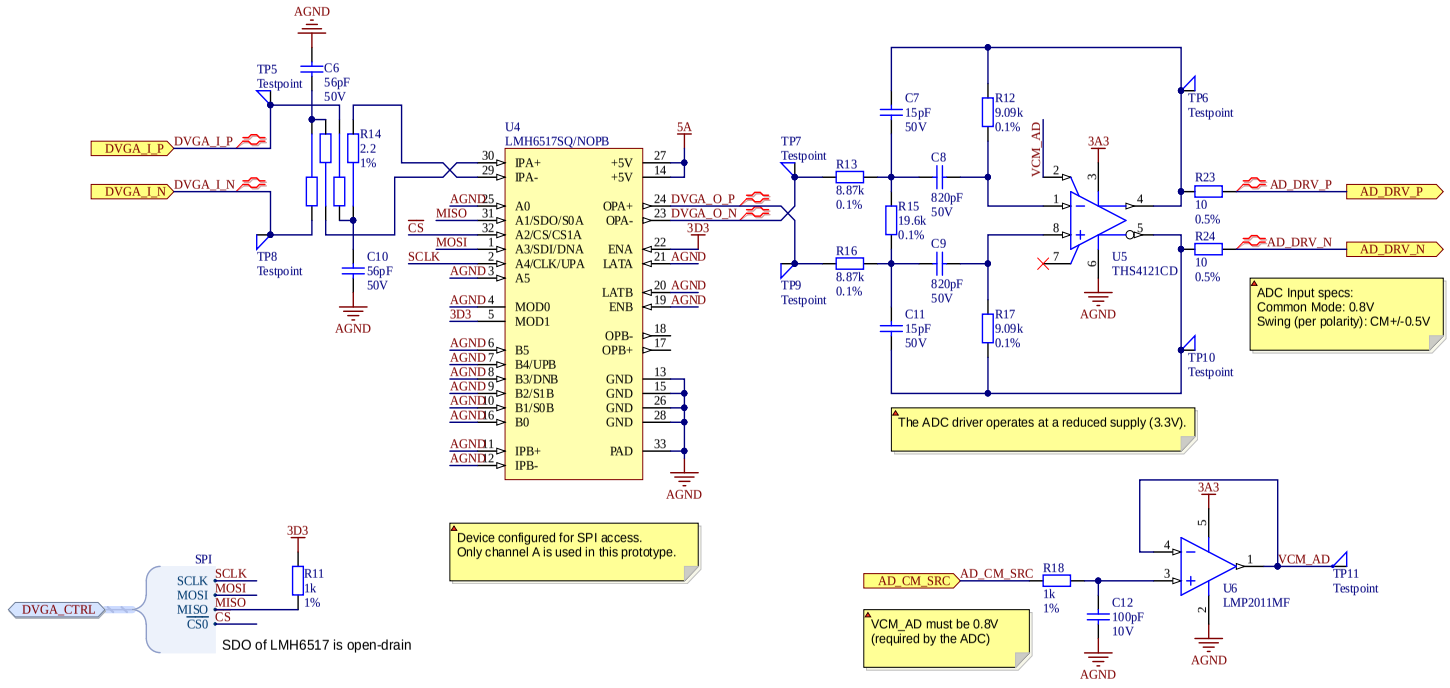

P1A
ASP-134488-01
P1B
ASP-134488-01
P1C
ASP-134488-01
FMC_P1_LA
LA
FMC_P1_HA
HA
FMC_P1_DP
DP
FMC_P1_I2C
I2C
FMC_P1_HB
HB
FMC_P1_VREF
VREF
FMC_P1_CLOCK
CLOCK
FMC_P1_JTAG
JTAG
FMC_P1_POWER
POWER
FMC_P1_MISC
MISC
Sheet Title FMC P1 400 Pin
Project Title ProjectTitle
Size: A3
Item:
Revision:
Date: 05/10/2017
Time: 11:35:56
Sheet * of *
File: CON_FMC_P1_400PIN.SchDoc
ProjectOrganization
ProjectAddress1
ProjectAddress2
ProjectAddress3
ProjectAddress4
Altium

SINGLE-CHANNEL ANALOG FRONT-END PROTOTYPE

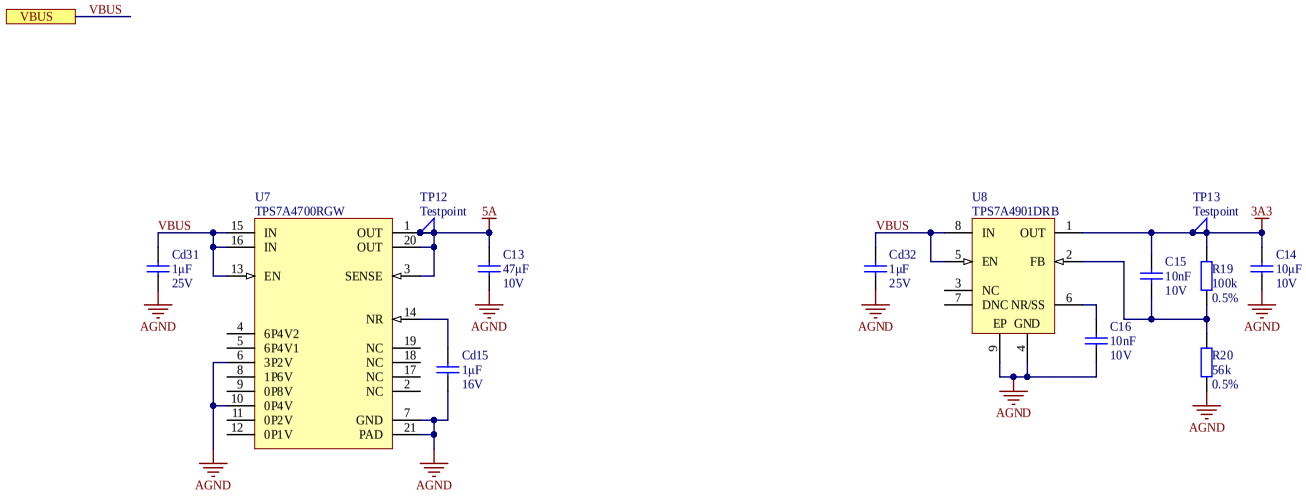

JIN
Header 1x3
JTWI
014117-XXXX
AGND
MUX
Preamp_MUX.SchDoc
PRE_O_P
PRE_O_N
TIN_P
TIN_N
SEL[0..1]
SEL[0..1]
JREF
Header 1x2
REF
V_Reference.SchDoc
OUT
EXT
PGA_AAF
PGA_AAF.SchDoc
DVGA_I_P
DVGA_I_N
AD_CM_SRC
AD_DRV_P
AD_DRV_N
DVGA_CTRL
JOUT
Header 1x3
JTWO
014117-XXXX
IGND
GND1
Testpoint
VISO
JCTRL
Header 8
ISO_IN0
ISO_IN1
ISO_IN2
ISO_IN3
ISO_IN4
ISO_OUT0
ISO
Dig_Isolators.SchDoc
ISO_IN[0..4]
LOC_OUT[0..4]
LOC_IN0
ISO_OUT0
LOC_OUT[0..4]
LOC_OUT0
LOC_OUT1
LOC_OUT2
LOC_OUT3
LOC_OUT4
SEL0
SEL1
LOC_IN0
SPI
SCLK
MOSI
CS0
MISO
GND2 Testpoint
GND3 Testpoint
GND4 Testpoint
GND5 Testpoint
GND6 Testpoint
GND7 Testpoint
GND8 Testpoint
GND9 Testpoint
JSUP
FFKDSA1/H1-5,08- 2
L1
10µH
C21
25V
100uF
Power Supplies
Power_Supplies.SchDoc
VBUS
VBUS range: 5.5 to 12V.
Title:
Root Schematic
Organization:
USCND
Project:
Pandora - Receiver Test Board
Version:
1.0
Revision:
D
Date:
03/10/2017
Author:
Pietro Giannelli
Approved By:
*
File name:
Root_Sheet.SchDoc
Sheet:
1
of
8



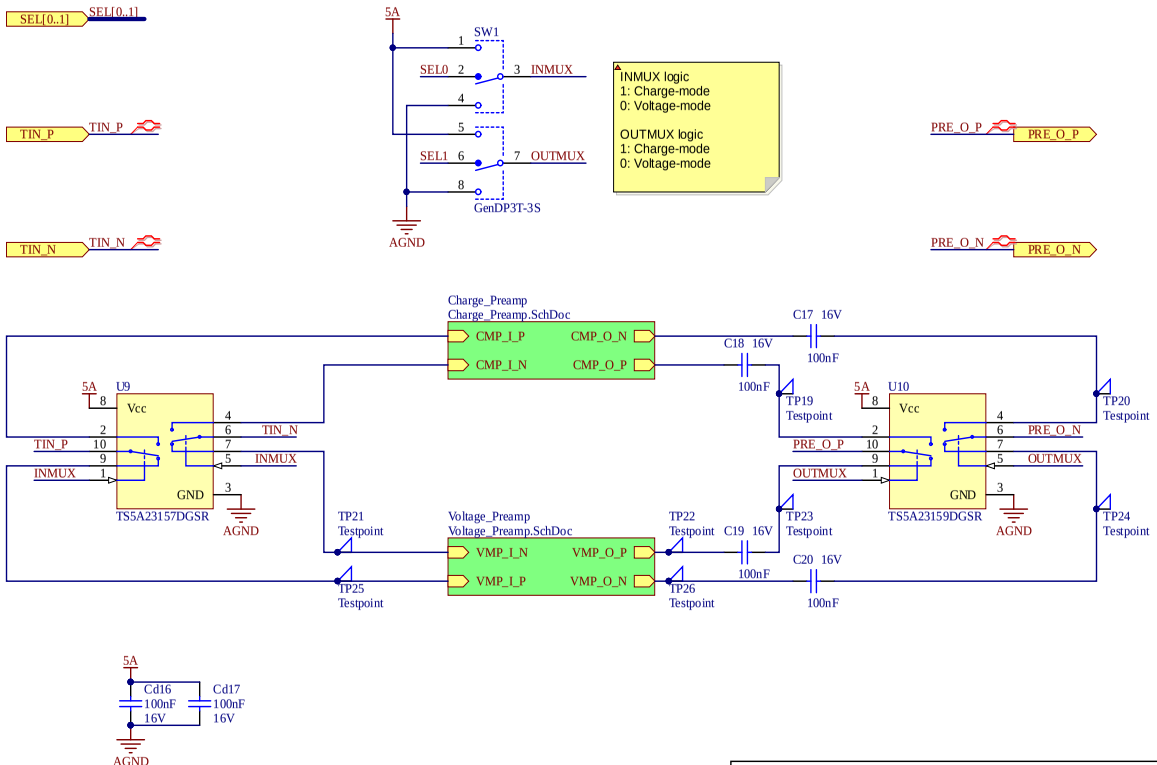
Title:	**Digital Isolation**
Organization: **USCND**	Project: **Pandora - Receiver Test Board**
Version: 1.0	Revision: D — Date: 03/10/2017
Author: Pietro Giannelli	Approved By: *
File name: Dig_Isolators.SchDoc	Sheet: 2 of 8



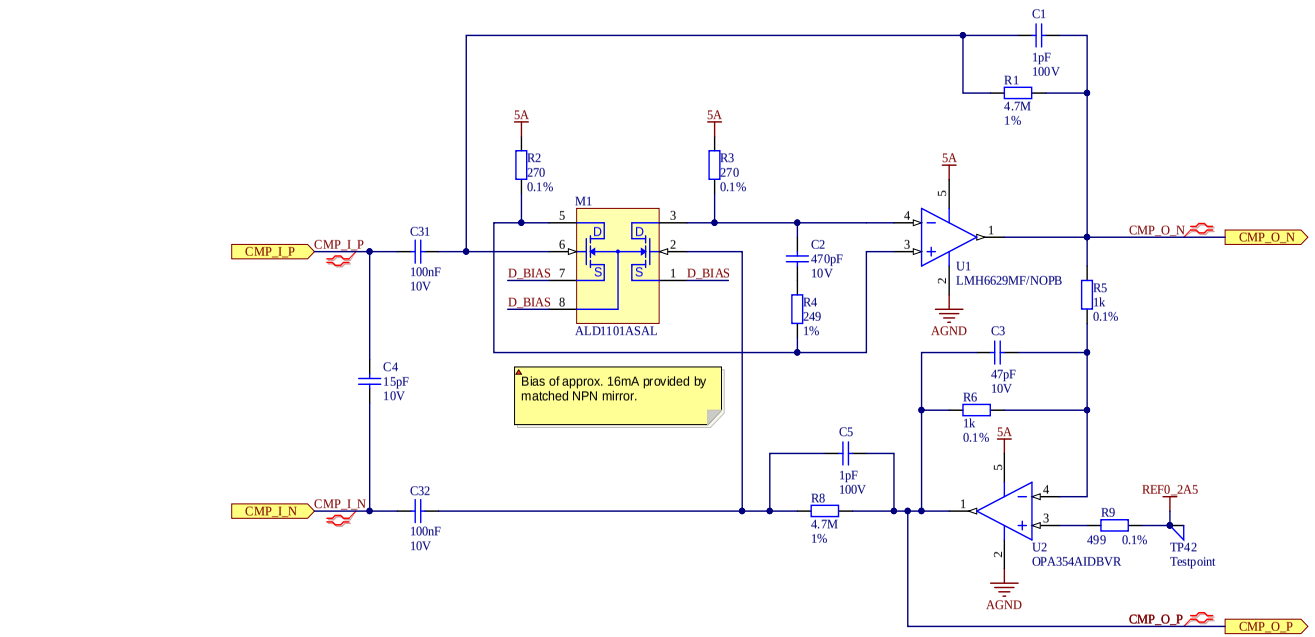
Title:	**Variable Gain Amplifier and AA Filter**
Organization:	USCND
Project:	Pandora - Receiver Test Board
Version:	1.0
Revision:	D
Date:	03/10/2017
Author:	Pietro Giannelli
Approved By:	*
File name:	PGA_AAF.SchDoc
Sheet:	3 of 8

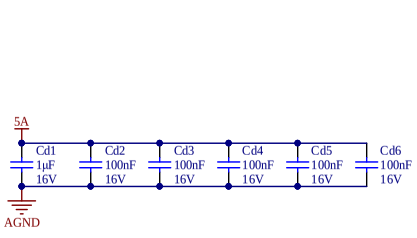


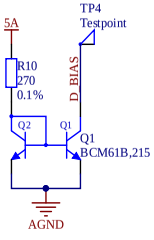
Title: **Power Supplies**			
Organization: **USCND**	Project: **Pandora - Receiver Test Board**		
Version: 1.0	Revision: D	Date: 03/10/2017	
Author: Pietro Giannelli	Approved By: *		
File name: Power_Supplies.SchDoc	Sheet: 4 of 8		

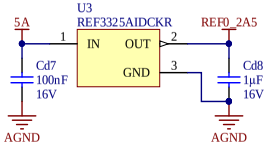


Title:	**Pre-Amplifier Multiplexing**
Organization: **USCND**	Project: **Pandora - Receiver Test Board**
Version: 1.0	Revision: D — Date: 03/10/2017
Author: Pietro Giannelli	Approved By: *
File name: Preamp_MUX.SchDoc	Sheet: 5 of 8

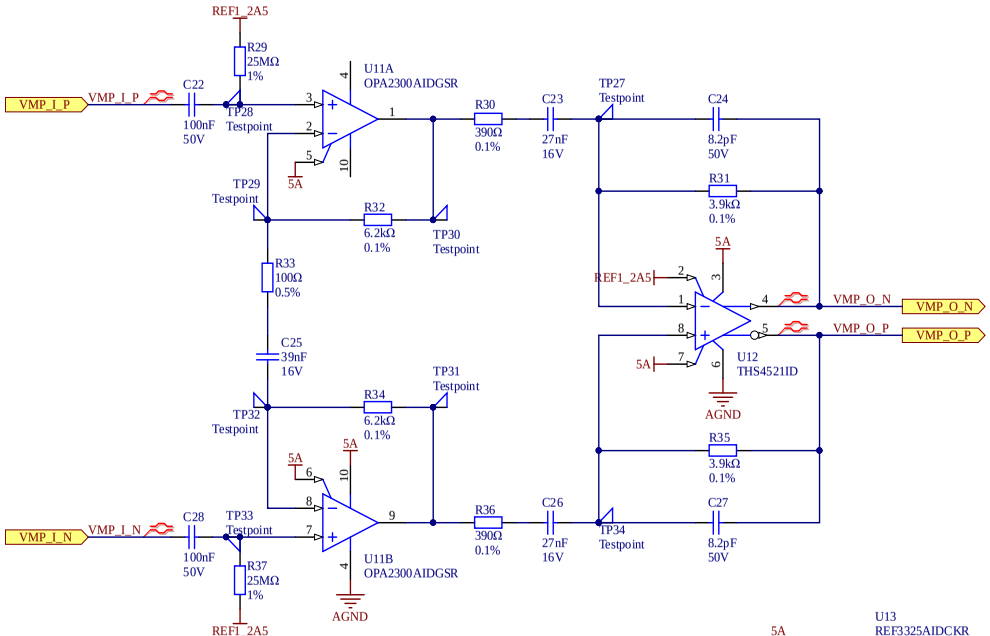


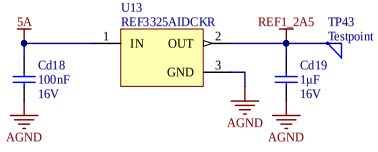


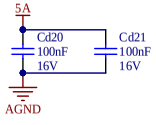




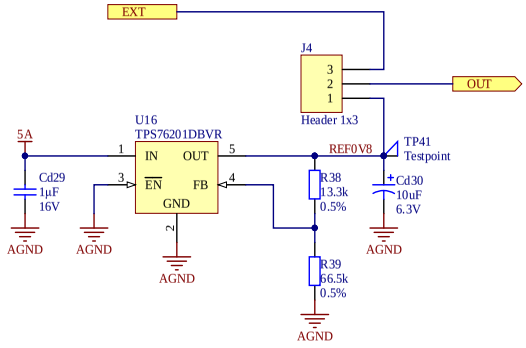
Title: **Charge-Mode Pre-Amplifier**		
Organization: **USCND**	Project: **Pandora - Receiver Test Board**	
Version: 1.0	Revision: D	Date: 03/10/2017
Author: Pietro Giannelli	Approved By: *	
File name: Charge_Preamp.SchDoc	Sheet: 6 of 8	





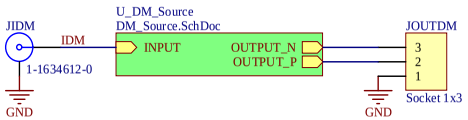


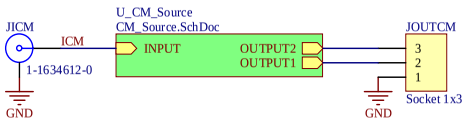
Title: **Voltage-Mode Pre-Amplifier**			
Organization: **USCND**	Project: **Pandora - Receiver Test Board**		
Version: 1.0	Revision: D	Date: 03/10/2017	
Author: Pietro Giannelli	Approved By: *		
File name: Voltage_Preamp.SchDoc	Sheet: 7 of 8		

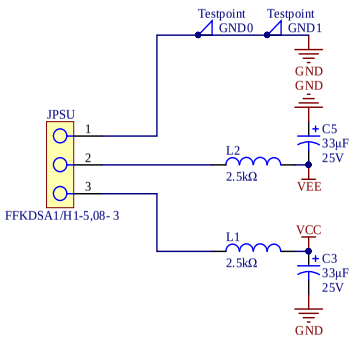


Title: **0.8V CM Reference Generator**			
Organization: **USCND**	Project: **Pandora - Receiver Test Board**		
Version: 1.0	Revision: D	Date: 03/10/2017	
Author: Pietro Giannelli	Approved By: *		
File name: V_Reference.SchDoc	Sheet: 8 of 8		

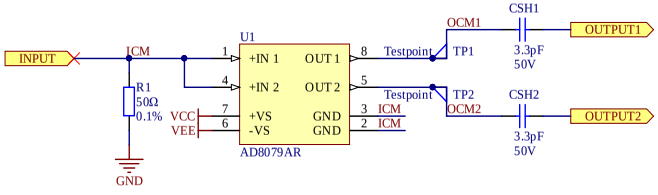
DIFFERENTIAL CHARGE SOURCE

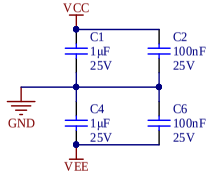




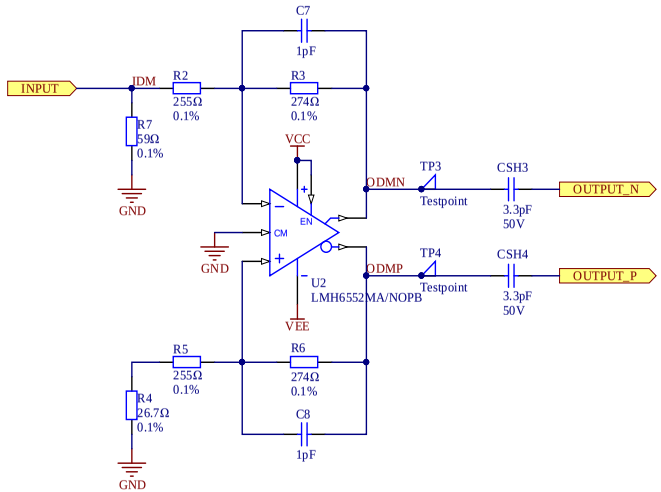


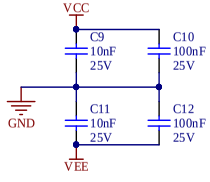
	Title: **Root Schematic**		
	Organization: **USCND**	Project: **Charge Source**	
	Version: 1.1	Revision: Initial	Date: 06/10/2017
	Author: Pietro Giannelli	Approved By: *	
	File name: RootSchematic.SchDoc	Sheet: 1 of 3	





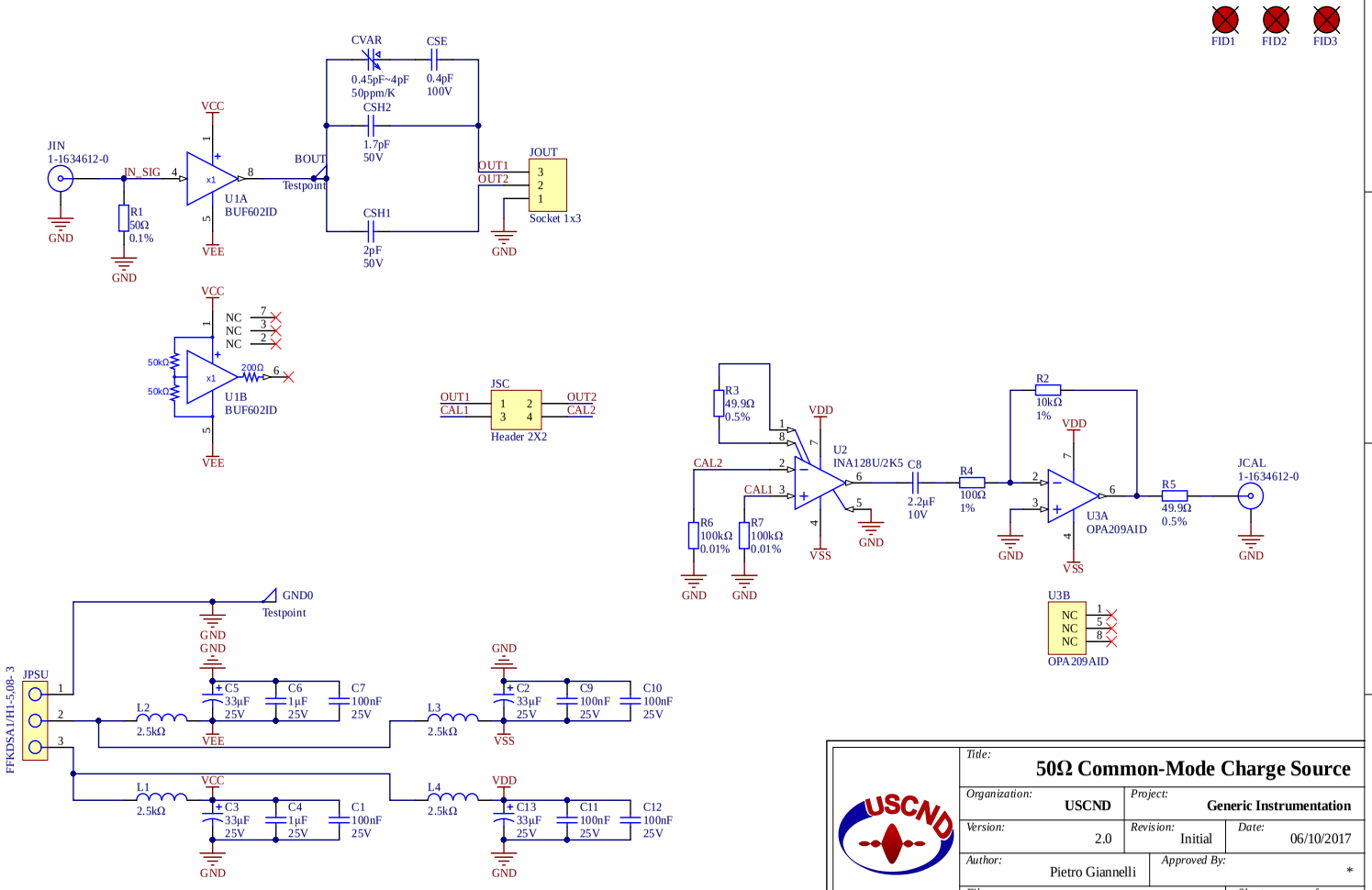
Title:	**Common-Mode Charge Source**
Organization: **USCND**	Project: **Charge Source**
Version: 1.1	Revision: Initial / Date: 06/10/2017
Author: Pietro Giannelli	Approved By: *
File name: CM_Source.SchDoc	Sheet: 2 of 3





Title: **Differential-Mode Charge Source**			
Organization: **USCND**	Project: **Charge Source**		
Version: 1.1	Revision: Initial	Date: 06/10/2017	
Author: Pietro Giannelli	Approved By: *		
File name: DM_Source.SchDoc	Sheet: 3 of 3		

COMMON-MODE CHARGE SOURCE



Title:	**50Ω Common-Mode Charge Source**
Organization: **USCND**	Project: **Generic Instrumentation**
Version: 2.0	Revision: Initial / Date: 06/10/2017
Author: Pietro Giannelli	Approved By: *
File name: RootSchematic.SchDoc	Sheet: 1 of 1

C

PULSE WIDTH ENCODER

```
%% PWEncoder for The Arbitrary Waveform Pulser
% Project Pandora - Pietro Giannelli, 2016-2017

% Encodes an arbitrary signal of finite duration into a pulse-width
% stream of arbitrary duty resolution.

% Changelog:
% 20161201 - Extended to half bridge (positive-negative)
% 20161202 - Low-level masking correction
% 20161212 - Added encoded stream output (16-bit word)
% 20161230 - Added fully differential support w/ 32-bit output
% 20170103 - Added alternate level 1 and 3 encoders
% 20170114 - Using only crossover modulations (no level 2 and 4)
% 20170315 - Added UART communications to PulserElementsSoC [removed]
% 20170330 - Added continuous modulation w/ reduced output range
% 20170411 - Added full-dynamic range extension - added file output

clearvars;

%% Output file name
output_file='Encoded stream.txt';

%% Pulser configuration parameters
awp8_sysclk = 100e6; % FPGA decoder clock
min_pw=20e-9; % Minimum pulse width

%% Encoder parameters
fsys=awp8_sysclk; % Decoder system clock [Hz]
fpwe=fsys/20; % Encoder source sample rate [Hz]
pwe_steps=fsys/fpwe; % Duration of a PWE period in fsys cycles
assert(mod(fsys,fpwe) == 0, 'System clock must be a multiple of the sample rate');
% There is also another requirement, that fsys/fpwe be an EVEN number. This
% encoder strongly relies on using 0.5 duty ratios.
assert(mod(pwe_steps,2) == 0, 'Duty quantization must be even');
assert(2*min_pw < 1/fpwe, 'Sample rate is too high for this pulser');
Gpre=1; % Pre-processing gain
Opre=0; % Pre-processing offset

% Note: the encoder input dynamic range is [-2;2], corresponding to an
% output of [-2HV;2HV]

%% Minimum and maximum duty ratios
```

```
Dmin=fpwe*min_pw;
Dmax=1-Dmin;
% Total number of duty steps (ignoring Dmin, Dmax saturation)
Dlev=uint16(pwe_steps);
% Dmin and Dmax in number of duty steps
Dqmin=uint16(ceil(min_pw*fsys));
Dqmax=Dlev-Dqmin;
% Therefore, the final value of encoded duty per switch must be an integer
% between Dqmin and Dqmax. 0 and Dlev are also acceptable duties.

% Note that Dqmin is used here to define the thresholds in order to
% avoid inconsistent banding caused by PW quantization errors!
actDmin=double(Dqmin)/double(Dlev);
% actDmin will likely be higher than Dmin.

%% Load the source stream from file
% If the source was sampled at rate different from fpwe, it must be
% resampled first!
instream=dlmread('CW_for_AWG.txt');
Nsamp=length(instream);

%% Encoder data structures
% Dq - Encoder output matrix
% Rows: encoded stream frames (one per input sample)
% Columns: corresponding switch [PP PN NP NN]
Dq=uint16(zeros(Nsamp,4));

%% Encoder core
for cx=1:Nsamp
    Cs=Gpre*instream(cx)+Opre; % Applying pre-scaling and offset

    Cframe=uint16([0 0 0 0]); % Current frame temporary storage vector
    % Columns: corresponding switch [PP PN NP NN]

    % Rectification
    if Cs>=0 % The special case where the sample is 0 can be handled by both
        pbias=1; % Positive bias true
    else
        Cs=-Cs; % Flip the sample
        pbias=0; % Positive bias false
    end
    % From now on the original polarity of the sample Cs is irrelevant to
    % the encoder. The output frame is properly re-assembled later to
    % account for polarity reversal.

    % Switches unused in this polarity need to operate at Dqmin
    Cframe(2)=Dqmin;
    Cframe(3)=Dqmin;

    if Cs>2 % Applying upper saturation
        Cs = 2;
```

```
    end

96      % Here we apply amplitude band-splitting, and use different encoding
    % levels depending on the value of Cs.
    if Cs>2-4*actDmin % High-range - duty ratios beyond limits!
        if (Cs>=2-1*actDmin)
            Cframe(1)=Dlev;
101         Cframe(2)=0;
            Cframe(3)=uint16((2-Cs)*Dlev); % Push switch 3 (NP) below Dmin
            Cframe(4)=Dlev;
        elseif (Cs>=2-2*actDmin)
            Cframe(1)=uint16((Cs-1+actDmin)*Dlev); % Push switch 1 (PP) over Dmax
106         Cframe(2)=0;
            Cframe(3)=Dqmin;
            Cframe(4)=Dlev;
        elseif (Cs>=2-3*actDmin)
            Cframe(1)=Dqmax;
111         Cframe(2)=uint16((-Cs+2-2*actDmin)*Dlev); % Push switch 2 (PN) below
                Dmin
            Cframe(3)=Dqmin;
            Cframe(4)=Dlev;
        else
            Cframe(1)=Dqmax;
116         Cframe(2)=Dqmin;
            Cframe(3)=Dqmin;
            Cframe(4)=uint16((Cs-1+3*actDmin)*Dlev); % Push switch 4 (NN) over
                Dmax
        end

121     elseif Cs>1-2*actDmin % Mid-range
        Cframe(1)=uint16((Cs-(1-2*actDmin))*Dlev)+Dqmin; % This switch is adjusted
        Cframe(4)=Dqmax; % This switch operates at maximum duty

    else % Low-Range
126     Cframe(1)=Dqmin; % This switch operates at minimum duty
        Cframe(4)=uint16(Cs*Dlev)+Dqmin; % This switch is adjusted
    end

    % Apply polarity reversal while writing the results to Dq
131 if pbias
        Dq(cx,:)=Cframe; % No polarity reversal needed
    else
        Dq(cx,1)=Cframe(3); % NP->PP
        Dq(cx,2)=Cframe(4); % NN->PN
136     Dq(cx,3)=Cframe(1); % PP->NP
        Dq(cx,4)=Cframe(2); % PN->NN
    end

end
141
%% Building the output bitstream
```

```
% This output bitstream is built with complementary edge decoding, since
% switches belonging to the same half-bridge are used together within
% one sample period.
Dlev=uint32(Dlev); % Converted to uint32 to avoid hitting the 16bit roof!
outstream=uint8(zeros(Nsamp*Dlev,4)); % There are fsys/fpwe bits per encoded
     sample
for cx=1:Nsamp
    % Switch PP
    % Sets to 1 the correct number of clock cycles
    % Starting from the beginning of the period
    frame_start=(cx-1)*Dlev + 1;
    frame_end=(cx-1)*Dlev + uint32(Dq(cx,1));
    outstream( frame_start:frame_end,1 )=1;
    % Switch PN
    % Sets to 1 the correct number of clock cycles
    % Starting from the ending of the period
    frame_end=(cx-1)*Dlev + uint32(Dq(cx,2));
    outstream( frame_start:frame_end,2 )=1;
    % Switch NP
    % Sets to 1 the correct number of clock cycles
    % Starting from the ending of the period
    frame_end=(cx-1)*Dlev + uint32(Dq(cx,3));
    outstream( frame_start:frame_end,3 )=1;
    % Switch NN
    % Sets to 1 the correct number of clock cycles
    % Starting from the ending of the period
    frame_end=(cx-1)*Dlev + uint32(Dq(cx,4));
    outstream( frame_start:frame_end,4 )=1;
end

%% Waveform plotter
figure();

sourc = subplot(3,1,1); % Plotting input sequence
plot(0:1/fpwe:(Nsamp-1)/fpwe,instream,'o');
ylim([-2 2]);
xlabel('time [s]');
ylabel('Amplitude');
title('Input sequence');

quant = subplot(3,1,2); % Plotting duty-quantized signal
plot(0:1/fpwe:(Nsamp-1)/fpwe,Dq(:,1),'o'); % PP switch
hold on
plot(0:1/fpwe:(Nsamp-1)/fpwe,-double(Dq(:,2)),'o'); % PN switch
plot(0:1/fpwe:(Nsamp-1)/fpwe,-double(Dq(:,3)),'o'); % NP switch
plot(0:1/fpwe:(Nsamp-1)/fpwe,Dq(:,4),'o'); % NN switch
ylim([-double(Dlev) double(Dlev)]);
xlabel('time [s]');
ylabel('Duty [on-sysclk-count]');
title('Encoded output');
```

```
bstre = subplot(3,1,3); % Plotting output bitstream
plot(0:1/fsys:Nsamp/fpwe-1/fsys,outstream(:,1)); % PP switch
hold on
plot(0:1/fsys:Nsamp/fpwe-1/fsys,1.2+double(outstream(:,2))); % PN switch
plot(0:1/fsys:Nsamp/fpwe-1/fsys,2.4+double(outstream(:,3))); % NP switch
plot(0:1/fsys:Nsamp/fpwe-1/fsys,3.6+double(outstream(:,4))); % NN switch
ylim([-0.1 4.7]);
yticks([0 1 1.2 2.2 2.4 3.4 3.6 4.6]);
yticklabels({'off','on','off','on','off','on','off','on'})
xlabel('time [s]');
ylabel('Logic level');
title('Bistream output');

linkaxes([sourc,quant,bstre],'x');
xlim([0 Nsamp/fpwe]);

%% Encoded file output (decoder-compatible)

% Open output file for writing
out_fid = fopen(output_file,'w');

% Output word format:
% 31..24 | 23..16 | 15..8 | 7..0
% DRVNN  | DRVNP  | DRVPN | DRVPP
% Dq(:,4)|Dq(:,3) |Dq(:,2)|Dq(:,1)

for cx=1:Nsamp
    binstring = strings(4,1);
    for cy=1:4
        binstring(cy) = dec2hex(Dq(cx,cy),2);
    end
    datastring = sprintf('%s%s%s%s',binstring(4), binstring(3), binstring(2),
         binstring(1));

    fprintf(out_fid,'%s\n',datastring); % Write current sample
end

fclose(out_fid);
```

D

FPGA PULSE WIDTH DECODER

This appendix includes the soft design of the `AWPulser8Decoder` FPGA IP core.

The first table documents the register mapping that can be accessed from the Avalon-MM bus.

The HDL code printed afterwards was written in a mix of Verilog and SystemVerilog, and uses an Intel FPGA proprietary embedded memory core to implement the `WrapBuf` storage. The instantiation hierarchy of the various modules is presented in the following list:

- `AWPulser8Decoder`:
  - `Avalon_Slave` instantiated as AVManager
  - `Controller` instantiated as CTRLi
  - `PWClockCore` instantiated as PWClocker
  - Generates 8 PulserChannel:
    - `WrapBuf` instantiated as WBuf
    - `PWDecoderCore` instantiated as PDecoder
    - `PWDecoderCore` instantiated as NDecoder

AVALON-MM REGISTER MAP

Address	Register name	R/W	Bitmask									
			31..24	23..16	15..8	7	6	5	4	3	2	1	0
0x0000	Status	R	X	X	X	X	X	X	X	X	X	CW/Burst	Busy/Idle
0x0001	Command	W	X	X	X	X	X	X	X	X	X	01: Start, 10: Stop	
0x0002	Channel Enable	R/W	X	X	X	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
0x0003	PW Length	R/W	X	X	X	Unsigned char (X-255)							
0x0004	Burst Count	R/W	X	X	X	Unsigned char (0: CW mode, 1-255: Burst mode)							
0x0005	Burst Length	R/W	X	X	(lsb) BL8	BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0
0x0006	PLL Config	ND	X	X	X	X	X	X	X	X	X	X	X
0x0007 0x0206	Channel 1 buffer	W	(NN)	(NP)	(PN)	(PP)							
0x0207 0x0406	Channel 2 buffer	W	(NN)	(NP)	(PN)	(PP)							
0x0407 0x0606	Channel 3 buffer	W	(NN)	(NP)	(PN)	(PP)							
0x0607 0x0806	Channel 4 buffer	W	(NN)	(NP)	(PN)	(PP)							
0x0807 0x0A06	Channel 5 buffer	W	(NN)	(NP)	(PN)	(PP)							
0x0A07 0x0C06	Channel 6 buffer	W	(NN)	(NP)	(PN)	(PP)							
0x0C07 0x0E06	Channel 7 buffer	W	(NN)	(NP)	(PN)	(PP)							
0x0E07 0x1006	Channel 8 buffer	W	(NN)	(NP)	(PN)	(PP)							

AWPULSER8DECODER

```
/*********************************************************************************
* AWPulser8Decoder                                                               *
*                                                                                *
* (c)2017, Pietro Giannelli, USCND-UNIFI                                         *
*********************************************************************************
*                                                                                *
* 8-channel synchronous pulse-width decoder for ultrasound.                      *
* Avalon slave IP core.                                                          *
*                                                                                *
*********************************************************************************/
module AWPulser8Decoder
    #(parameter Dws=8)
    (
    // Avalon slave interface signals
    input clock, reset, read, write,
    input [15:0] address,
    input [3:0] byteenable,
    input [31:0] writedata,
    output [31:0] readdata,

    // Exported signals
    // Pulser Drive Signals
    output [7:0] drvPP, // P-switch, P-side
    output [7:0] drvPN, // N-switch, P-side
    output [7:0] drvNP, // P-switch, N-side
    output [7:0] drvNN, // N-switch, N-side
    // Pulser Clock Signals
    output [1:0] drvClk,
    // Pulser status LEDs
    output [1:0] statusLEDs,
    // Sync
    output StreamSync // Pulses at the start of every burst output
    // If the pulser is operating CW, pulses at the start of every period
    );

    // Avalon reset MUST be synchronous
    wire int_sync_rst;
    assign int_sync_rst = reset;
    // Operational wire rerouted to the avalon slave submodule
    wire operational;

    // Config register wires
    wire [7:0] CSteps; // Holds the number of clock cycles per PW period
    wire [8:0] BurstLen; // Number of valid words in the buffers (all of them)
    wire [7:0] BurstCount; // Number of bursts to perform before stopping
    wire [7:0] ChEnable; // Channel enable bits
    // command wires
    wire bus_trigger;
```

```
    wire bus_stop;
    // Avalon slave module
    Avalon_Slave AVManager(
        .clock(clock),
        .read(read),
        .write(write),
        .address(address),
        .byteenable(byteenable), // Currently unimplemented
        .writedata(writedata),
        .readdata(readdata),

        .bus_trigger(bus_trigger),
        .bus_stop(bus_stop),
        .csteps(CSteps),
        .burstlen(BurstLen),
        .burstcount(BurstCount),
        .chenable(ChEnable),
        .status(statusLEDs),
        .operational(operational),
        .rst(int_sync_rst)
    );

    // Pulser clocking is disabled
    assign drvClk = 2'b11;
    // Clock resync signal
    wire ctrl_pwclk_rst;

    // This register is pulsed to terminate the decoders
    // (otherwise they will keep decoding the last feed samples).
    // IMPORTANT: Need to count CSteps number of cycles AFTER ctrl_pwclk_rst is
        asserted
    // before asserting terminate. This ensures that the current samples are fully
        decoded.
    reg terminate;
    wire [7:0]SSyncP; // Collects the sample syncs to generate the terminate
        signal
    wire [7:0]SSyncN; // Collects the sample syncs to generate the terminate
        signal
    wire GSync; // Global sample sync

    assign GSync = | {SSyncP, SSyncN}; // Reduce all these syncs

    reg termwaitcnt; // Waiting for counter done
    reg [7:0]termcd; // Count-up register

    always @(posedge clock)
    begin
        if (int_sync_rst)
        begin
            terminate <= 1'b0;
            termwaitcnt <= 1'b0;
```

```
            termcd <= 8'h00;
        end
        if (terminate)
            terminate <= 1'b0; // De-assert terminate after 1 cycle
    100 else if (operational && GSync) // When operational captures GSync
        begin
            termcd <= 8'h00;
            terminate <= 1'b0;
            termwaitcnt <= 1'b1;
    105 end
        else if (termwaitcnt) // If it is counting
        begin
            if (termcd < CSteps) // Counting not done
            begin
    110         // Count-up
                termcd <= termcd + 8'h01;
            end
            else // Counting done
            begin
    115         termcd <= 8'h00; // Reset counter
                if (~operational)
                begin
                    terminate <= 1'b1; // Kill the decoder when not operational
                    termwaitcnt <= 1'b0;
    120         end
            end
        end
        else
        begin
    125     terminate <= 1'b0;
            termwaitcnt <= 1'b0;
        end
    end

    130 // Sync signal coming out of the clock gen
    wire MainSync;
    // Instantiation of the PWD sync generator (one feeds all)
    PWClockCore #(.Dws(Dws)) PWClocker(
        .Sync(MainSync),
    135 .CSteps(CSteps),
        .SysClk(clock),
        .Rst(int_sync_rst || ctrl_pwclk_rst)
    );

    140 // Tapeout signal to each channel
    wire [7:0] tapeout;
    // Restart signal to all channels
    wire restart;
    // Rollback signal from each channel
    145 wire [7:0] rollback;
```

```
    // Instantiation of the pulser controller
    Controller CTRLi(
        .clock(clock),
        .Rst(int_sync_rst),
        .Trigger(bus_trigger), // Bus trigger - from Avalon instruction decoder (0x01[1:0])
        .Stop(bus_stop), // Bus stop - from Avalon instruction decoder (0x01[1:0])
        .PWSync(MainSync),
        .Rollback(| rollback), // rollback is reduced from all the WrapBufs
        .BurstCount(BurstCount), // Number of bursts to be performed before stopping
        .ChEnable(ChEnable), // Channel enable - from Avalon configuration register (0x02[7:0])
        .tapeout(tapeout), // Tapeout signals to WrapBufs
        .restart(restart), // Restart signals to WrapBufs
        .pwclockrst(ctrl_pwclk_rst), // Restarts the PWClock generator
        .operational(operational) // Signals that the decoder is working
    );

    // Output stream sync is OR'd from every WrapBuf
    wire [7:0] burst_sync;
    assign StreamSync = | burst_sync;

    // Generating the correct write enable signal depending on the memory bank being accessed
    reg [7:0] write_wb;
    always @(write, address) // This is combinatorial
    begin
        write_wb = 8'h00;
        if (write)
        begin
            write_wb[0] = ((address >= 16'h0007) && (address < 16'h0207))? 1'b1 : 1'b0; // Channel 1
            write_wb[1] = ((address >= 16'h0207) && (address < 16'h0407))? 1'b1 : 1'b0; // Channel 2
            write_wb[2] = ((address >= 16'h0407) && (address < 16'h0607))? 1'b1 : 1'b0; // Channel 3
            write_wb[3] = ((address >= 16'h0607) && (address < 16'h0807))? 1'b1 : 1'b0; // Channel 4
            write_wb[4] = ((address >= 16'h0807) && (address < 16'h0A07))? 1'b1 : 1'b0; // Channel 5
            write_wb[5] = ((address >= 16'h0A07) && (address < 16'h0C07))? 1'b1 : 1'b0; // Channel 6
            write_wb[6] = ((address >= 16'h0C07) && (address < 16'h0E07))? 1'b1 : 1'b0; // Channel 7
            write_wb[7] = ((address >= 16'h0E07) && (address < 16'h1007))? 1'b1 : 1'b0; // Channel 8
        end
    end

    generate // Channel logic generation
```

```
        genvar cx;
        for (cx=0; cx<=7; cx=cx+1)
        begin: PulserChannel // Block name
            // Connections between buffer and decoders
            wire [31:0] encdata; // Data transfer between WrapBuf and Decoder
            // [31 EncNN 24][23 EncNP 16][15 EncPN 8][7 EncPP 0]
            wire sync; // Sync signal from WrapBuf to Decoder
            // Instantiation
            WrapBuf WBuf(
                .clock(clock),
                .rst(int_sync_rst),
                // Here the Avalon slave interface directly connects to the memory
                .wr_en(write_wb[cx]), // Externally decoded
                .wr_addr(address-(7+512*cx)), // Memory offset is 7 + size * (
                    channel_id)
                .wr_data(writedata), // Word size is 32bit (4x8bit encoded words)
                .tapeout(tapeout[cx]),
                .data_lim(BurstLen),
                .restart(restart),
                .rollback(rollback[cx]),
                .rd_data(encdata),
                .data_rdy(sync),
                .burst_sync(burst_sync[cx])
            );
            PWDecoderCore #(.Dws(Dws), .Dbs(1)) PDecoder(
                .PDrv(drvPP[cx]) ,  // output  PDrv_sig
                .NDrv(drvPN[cx]) ,  // output  NDrv_sig
                .OSync(SSyncP[cx]) , // Output OSync_sig
                .PEnc(encdata[7:0]) ,   // input [Dws-1:0] PEnc_sig
                .NEnc(encdata[15:8]) ,  // input [Dws-1:0] NEnc_sig
                .CSteps(CSteps) ,   // input [Dws-1:0] CSteps_sig
                .DBSteps(1'b0) ,    // input [Dbs-1:0] DBSteps_sig
                .NLeads(1'b0) , // input  NLeads_sig
                .Sync(sync) ,   // input  Sync_sig
                .SysClk(clock) ,    // input  SysClk_sig
                .Rst(int_sync_rst || terminate)     // input  Rst_sig
            );
            PWDecoderCore #(.Dws(Dws), .Dbs(1)) NDecoder(
                .PDrv(drvNP[cx]) ,  // output  PDrv_sig
                .NDrv(drvNN[cx]) ,  // output  NDrv_sig
                .OSync(SSyncN[cx]) , // Output OSync_sig
                .PEnc(encdata[23:16]) , // input [Dws-1:0] PEnc_sig
                .NEnc(encdata[31:24]) , // input [Dws-1:0] NEnc_sig
                .CSteps(CSteps) ,   // input [Dws-1:0] CSteps_sig
                .DBSteps(1'b0) ,    // input [Dbs-1:0] DBSteps_sig
                .NLeads(1'b0) , // input  NLeads_sig
                .Sync(sync) ,   // input  Sync_sig
                .SysClk(clock) ,    // input  SysClk_sig
                .Rst(int_sync_rst || terminate)     // input  Rst_sig
            );
        end
```

```
    endgenerate

endmodule
```

AVALON_SLAVE

```
/*****************************************************************************
* Avalon_Slave                                                               *
*                                                                            *
* (c)2017, Pietro Giannelli, USCND-UNIFI                                     *
*****************************************************************************
*                                                                            *
* Avalon interface for AWPulser8Decoder.                                     *
*                                                                            *
*****************************************************************************/
module Avalon_Slave
    (
    // Avalon slave interface signals
    input clock, read, write,
    input [15:0] address,
    input [3:0] byteenable,
    input [31:0] writedata,
    output [31:0] readdata,

    // Custom module signals
    output bus_trigger,
    output bus_stop,

    output [7:0] csteps,
    output [8:0] burstlen,
    output [7:0] burstcount,
    output [7:0] chenable,

    output [1:0] status,

    input operational,
    input rst
    );

    // Slave details:
    // Fixed write latency: 0 cycles
    // Fixed read latency: TBD

    // Valid addresses: 0x0000 to 0x0005

    // Registers
    reg [1:0] status_register;      //0x0000
    reg [7:0] channel_en_register;  //0x0002
```

```
    reg [7:0] pw_length_register;   //0x0003
    reg [7:0] burst_count_register; //0x0004
    reg [8:0] burst_length_register;//0x0005

    reg bus_triggerR;
    reg bus_stopR;
    assign bus_trigger = bus_triggerR;
    assign bus_stop = bus_stopR;

    // Static assignments to AWPulser8Decoder
    assign csteps = pw_length_register;
    assign burstlen = burst_length_register;
    assign burstcount = burst_count_register;
    assign chenable = channel_en_register;

    wire [5:0] register_select;
    // Address decoder
    assign register_select[0] = (address == 16'h0000) & read; // read-only
    assign register_select[1] = (address == 16'h0001) & write; // write-only
    assign register_select[2] = (address == 16'h0002) & (read | write);
    assign register_select[3] = (address == 16'h0003) & (read | write);
    assign register_select[4] = (address == 16'h0004) & (read | write);
    assign register_select[5] = (address == 16'h0005) & (read | write);

    // Status manager
        assign status[0] = ~status_register[0];
        assign status[1] = ~status_register[1];
    always@(posedge clock)
    begin
        if (rst)
            status_register <= 2'b00;
        else
        begin
            status_register[0] <= operational;
            if (burst_count_register == '0) // Checks whether we are operating CW
                status_register[1] <= 1'b1;
            else
                status_register[1] <= 1'b0;
        end
    end

    // Command manager
    always@(posedge clock)
    begin
        if (rst)
        begin
            bus_triggerR <= 1'b0;
            bus_stopR <= 1'b0;
        end
        else if (register_select[1])
        begin
```

```
            if (writedata[1:0]==2'b01) // Bus triggering
            begin
                    bus_triggerR <= 1'b1;
                    bus_stopR <= 1'b0;
            end
            else if (writedata[1:0]==2'b10) // Bus stop
            begin
                    bus_triggerR <= 1'b0;
                    bus_stopR <= 1'b1;
            end
            else // When command is 11 or 00 return to 0
            begin
                    bus_triggerR <= 1'b0;
                    bus_stopR <= 1'b0;
            end
        end
        else
        begin
            bus_triggerR <= 1'b0;
            bus_stopR <= 1'b0;
        end
    end

    // Configuration writer
    always@(posedge clock)
    begin
        if (rst)
        begin
            channel_en_register <= '0;
            pw_length_register <= '0;
            burst_count_register <= '0;
            burst_length_register <= '0;
        end
        else
        begin
            if ((register_select[2]) && write)
                channel_en_register <= writedata[7:0];
            if ((register_select[3]) && write)
                pw_length_register <= writedata[7:0];
            if ((register_select[4]) && write)
                burst_count_register <= writedata[7:0];
            if ((register_select[5]) && write)
                burst_length_register <= writedata[8:0];
        end
    end

    reg [31:0]  readdataR;
    assign readdata = readdataR;
    // Readback
    always@(posedge clock)
    begin
```

```
        if (rst)
            readdataR <= '0;
        else
        begin
            if (read)
            begin
                case (register_select) // It's OK if this thing is latched
                    6'b000001: readdataR[1:0] <= status_register;
                    6'b000100: readdataR[7:0] <= channel_en_register;
                    6'b001000: readdataR[7:0] <= pw_length_register;
                    6'b010000: readdataR[7:0] <= burst_count_register;
                    6'b100000: readdataR[8:0] <= burst_length_register;
                endcase
            end
        end
    end

endmodule
```

PWCLOCKCORE

```
/*******************************************************************************
* PWClockCore                                                                  *
*                                                                              *
* (c)2017, Pietro Giannelli, USCND-UNIFI                                       *
*******************************************************************************
*                                                                              *
* NOTES:                                                                       *
*  - Sync is output synchronously with input SysClk                            *
*  - Period is forcefully restarted on sync reset                              *
*  - CSteps MUST be even to be compatible with the decoder logic               *
*                                                                              *
*******************************************************************************/
module PWClockCore
    #(parameter Dws=8) // Dws: decoder word
    (
    output Sync, // Sync output
    input[Dws-1:0] CSteps, // Length of PWE period
    input SysClk, Rst // Fast clock and sync reset
    );

    reg[Dws-1:0] CStepsR;
    reg[Dws-1:0] DCxR;
    reg SyncR; // Output sync register

    assign Sync = SyncR;

    always@(posedge SysClk)
```

```
    begin
        if (Rst)
        begin
            CStepsR <= CSteps;
            DCxR <= '0;
        end
        else if (DCxR == CStepsR) // Resetting to 1
            DCxR <= 1'b1;
        else // Increment the counter
            DCxR <= DCxR + 1'b1;

        if (Rst)
            SyncR <= 1'b0;
        else if (DCxR == 1'b1)
            SyncR <= 1'b1;
        else
            SyncR <= 1'b0;
    end

endmodule
```

CONTROLLER

```
/*****************************************************************************
* Controller                                                                 *
*                                                                            *
* (c)2017, Pietro Giannelli, USCND-UNIFI                                     *
*****************************************************************************
*                                                                            *
* Decoder controller logic.                                                  *
*                                                                            *
*****************************************************************************/
module Controller
    (
        input clock,
        input Rst,
        input Trigger, // Starts bursting AND restarts bursting
        input Stop, // Stops bursting
        input PWSync, // From PWClockCore, is redistributed through tapeout
        input Rollback, // Fed back from the WrapBufs (OR'd)
        input [7:0] BurstCount,
        input [7:0] ChEnable, // This signals enable the tapeouts
        // ChEnable can be changed during operation.

        output [7:0] tapeout, //
        output restart, // Restarts the WrapBufs (all of them)
        output pwclockrst, // Resets the PWClockGen
        output operational
```

```
    );

    reg operationalR; // Remains asserted while pulsing
    reg [7:0] tapeoutR; // Tapeout is delayed 1 cycle w.r.t. PWSync
    reg restartR; // WrapBuf restart signal
    reg pwclockrstR; // PWClockCore control signal (1=disabled)

    assign tapeout = tapeoutR;
    assign restart = restartR;
    assign pwclockrst = pwclockrstR;
    assign operational = operationalR;

    reg [7:0] BurstCounter; // Counts
    // Burst counter logic
    always@(posedge clock)
    begin
        if (Rst || BurstCount == '0)
            BurstCounter <= '0;
        else if (operational && Rollback)
            BurstCounter <= BurstCounter + 8'd1;
        else if ((~operational) || restartR) // This counter is also reset when
             retriggering
            BurstCounter <= '0;
        else
            BurstCounter <= BurstCounter;
    end

    // Feeds the PW clock to the selected channels
    always@(posedge clock)
        tapeoutR <= {8{PWSync}} & ChEnable;

    // Trigger logic
    always@(posedge clock)
    begin

        if (Rst)
        begin
            operationalR <= 1'b0;
            restartR <= 1'b1; // WrapBufs are kept at address 0
            pwclockrstR <= 1'b1; // Turns off the PW clock generator
        end

        else if (Trigger && operationalR) // Already running, restart!
        begin
            operationalR <= 1'b1; // Still busy!
            restartR <= 1'b1; // WrapBufs are kept at address 0
            pwclockrstR <= 1'b1; // Disables the PW clock generator
        end

        else if (Trigger && ~operationalR) // Start!
        begin
```

```
            operationalR <= 1'b1;
            restartR <= 1'b0; // WrapBufs are free to tapeout
            pwclockrstR <= 1'b1; // PW clock still off (waiting de-assertion of
                trigger)
        end
80
        else if (operationalR) // Run! Also, check for the stop condition
        begin
            if (Stop) // Stop the thing!
            begin
85              operationalR <= 1'b0; // No longer operational
                restartR <= 1'b1; // WrapBufs are kept at address 0
                pwclockrstR <= 1'b1; // Turns off the PW clock generator
            end

90          else if ((BurstCount != '0) && (BurstCounter >= BurstCount)) // Stop
                the thing!
            begin
                operationalR <= 1'b0; // No longer operational
                restartR <= 1'b1; // WrapBufs are kept at address 0
                pwclockrstR <= 1'b1; // Turns off the PW clock generator
95          end

            else // Run normally
            begin
                operationalR <= 1'b1;
100             restartR <= 1'b0;
                pwclockrstR <= 1'b0; // Tapeout enabled
            end
        end

105     else // Do nothing
        begin
            operationalR <= operationalR;
            restartR <= restartR;
            pwclockrstR <= pwclockrstR;
110     end

    end

endmodule
```

WRAPBUF

```
1   /*****************************************************************************
    * WrapBuf                                                                   *
    *                                                                           *
    * (c)2017, Pietro Giannelli, USCND-UNIFI                                    *
```

```
/*****************************************************************************
*                                                                            *
* Circular buffer holding the encoded data.                                  *
*                                                                            *
*****************************************************************************/
module WrapBuf
    (
    // RAM inside has 512 words, meaning we need 9 bit addresses
    input clock,
    input rst, // Synchronous reset

    // Filling ports. These are connected directly to the memory
    input wr_en,
    input [8:0] wr_addr,
    input [31:0] wr_data,

    // Tapeout ports
    input tapeout, // When tapeout is de-asserted, last output is retained - THIS IS THE DECODER SYNC SIGNAL -
    input [8:0] data_lim, // Returns to zero when data_lim == internal address counter
    input restart, // Forces return to zero of counter, regardless of data_lim
    output rollback, // Asserted when output data is last word before rollback. This signal is one cycle long
    output [31:0] rd_data,
    output data_rdy, // Data ready signal
    output burst_sync // Signal pulsing whenever the first sample is output (pulse length = 1PWClock)
    );

    reg [8:0] rd_addr; // Internal address counter
    reg [31:0] rd_dataR; // Output data register

    reg rd_buf; // Read enable signal for the buffer
    reg rd_latch; // Latches the output memory into the output register
    reg rollbackR; // Used to signal the output that a restart has happened
    reg data_rdyR; // Used by the next stage to sample rd_data
    reg burst_syncR;

    wire [31:0] buf_out; // Buffer output bus

    // Static assignments
    assign rollback = rollbackR;
    assign rd_data = rd_dataR;
    assign data_rdy = data_rdyR;
    assign burst_sync = burst_syncR;

    // Memory instance
    RAMBuf buffer( .clock(clock), .data(wr_data), .rdaddress(rd_addr), .rden(rd_buf), .wraddress(wr_addr), .wren(wr_en), .q(buf_out) );

```

```
    // Handles the counter address generator
    always@(posedge clock)
    begin
        if (rst || restart)
            rd_addr <= '0;
        else if (data_rdyR) // The counter is updated after every read and decode has been performed! (otherwise we would skip 0)
        begin
            if (rd_addr == data_lim || rd_addr == '1) // Reached set limit or self-limit
                rd_addr <= '0; // Rollback!
            else
                rd_addr <= rd_addr + 1'b1; // Increase the counter
        end
        else // Nothing new under the sun
            rd_addr <= rd_addr;
    end

    // Handles the burst sync signal generation
    always@(posedge clock)
    begin
        if (rst || restart)
            burst_syncR <= 1'b0;
        else if (rd_addr == '0 && data_rdyR == 1'b1) // Toggled on at the first sample
            burst_syncR <= 1'b1;
        else if (data_rdyR == 1'b1) // Toggled off at any other data_rdy (just to be sure)
            burst_syncR <= 1'b0;
        else // Keep
            burst_syncR <= burst_syncR;
    end

    // Rollback signal generator
    always@(posedge clock)
    begin
        if (rst || restart)
            rollbackR <= 1'b0;
        else if (tapeout && (rd_addr == data_lim-1 || (rd_addr+1) == '1))
            rollbackR <= 1'b1; // Signal this outside
        else
            rollbackR <= 1'b0; // Returns to zero
    end



    // Generates the read enable
    always@(posedge clock)
    begin
        if (rst)
```

```
            rd_buf <= 1'b0;
        else if (tapeout) // Starts reading
            rd_buf <= 1'b1; // Causes buffer read at next clock cycle
        else
            rd_buf <= 1'b0; // Returns to 0
    end

    // Generates the latch data output
    always@(posedge clock)
    begin
        if (rst)
            rd_latch <= 1'b0;
        else if (rd_buf) // Buffer output has been updated
            rd_latch <= 1'b1;
        else
            rd_latch <= 1'b0;
    end

    // Actually does the data output latching
    always@(posedge clock)
    begin
        if (rst)
            rd_dataR <= '0;
        else if (rd_latch) // Latch the buffer at the output
            rd_dataR <= buf_out;
        else
            rd_dataR <= rd_dataR;
    end

    // Asserts data ready on output latching
    always@(posedge clock)
    begin
        if (rst)
            data_rdyR <= 1'b0;
        else if (rd_latch) // Decoder has valid data
            data_rdyR <= 1'b1;
        else
            data_rdyR <= 1'b0;
    end

endmodule
```

PWDECODERCORE

```
/*****************************************************************************
* PWDecoderCore                                                              *
*                                                                            *
* (c)2017, Pietro Giannelli, USCND-UNIFI                                     *
```

```
/*****************************************************************************
*                                                                            *
* NOTES:                                                                     *
*  - Sync (PWE period) is generated externally, and MUST BE synchronous with *
*      SysClk. Otherwise nothing works                                       *
*  - Decoder is disabled while Rst high                                      *
*  - Sync signal is ONE SysClk tic long                                      *
*  - NLeads=1 means N-switch operates leading-edge                           *
*                                                                            *
*****************************************************************************/
module PWDecoderCore
    #(parameter Dws=8, Dbs=4) // Dws: decoder word, Dbs: deadband word
    (
    output PDrv, NDrv, // Decoded PWM outputs
    output OSync, // Output sync signal
    // Data inputs
    input[Dws-1:0] PEnc, // Encoded duty positive switch
    input[Dws-1:0] NEnc, // Encoded duty negative switch
    // Configuration inputs
    input[Dws-1:0] CSteps, // Length of PWE period
    input[Dbs-1:0] DBSteps, // Length of deadband (currently unused)
    input NLeads, Sync, SysClk, Rst
    );

    reg[Dws-1:0] PEncR; // Registered P encoded stream word
    reg[Dws-1:0] NEncR; // Registered N encoded stream word
    reg[Dws-1:0] CStepsR; // Registered length of PWE period
    reg[Dbs-1:0] DBStepsR; // Deadband length. Not yet implemented.

    reg OSyncR; // Output signal synchronous to start of PW decoded output
    assign OSync = OSyncR;

    // Submodule interconnects and instances below
    wire PDec, NDec; // Outputs from decoders, feed to LUT
    wire PLSync, NLSync; // These are delayed before output (to account for LUT
        delay)
    wire[Dws-1:0] PCount; // P counter output
    wire[Dws-1:0] NCount; // N counter output

    // Parametrized constants
    parameter[Dws-1:0] UPCntStart = {{(Dws-1){1'b0}},1'b1}; // Used to reset the
        decoder counter to 1

    // P-Switch decoder logic
    UDCounter #(.Cws(Dws)) PDecCx(.COut(PCount), .LSync(PLSync), .LoadUp(
        UPCntStart), .LoadDn(CStepsR), .En(~Rst), .Load(Sync), .UDb(~NLeads), .
        SysClk(SysClk));
    CmpDec #(.Cws(Dws)) PDecCmp(.PWDec(PDec), .Enc(PEncR), .Cnt(PCount));

    // N-Switch decoder logic
```

```
    UDCounter #(.Cws(Dws)) NDecCx(.COut(NCount), .LSync(NLSync), .LoadUp(
        UPCntStart), .LoadDn(CStepsR), .En(~Rst), .Load(Sync), .UDb(NLeads), .
        SysClk(SysClk));
    CmpDec #(.Cws(Dws)) NDecCmp(.PWDec(NDec), .Enc(NEncR), .Cnt(NCount));

    // Output LUT logic
    ClampLUT PDLUT(.OutP(PDrv), .OutN(NDrv), .InP(PDec), .InN(NDec), .SysClk(
        SysClk));

    // Sync delayer
    always@(posedge SysClk)
    begin
        if (Rst)
            OSyncR <= 1'b0;
        else if (PLSync | NLSync)
            OSyncR <= 1'b1;
        else
            OSyncR <= 1'b0;
    end

    // Input and configuration registers
    always@(posedge SysClk)
    begin
        if (Rst)
        begin
        // Clearing the inputs
            PEncR <= '0;
            NEncR <= '0;
            CStepsR <= '0;
            DBStepsR <= '0;
        end
        else if (Sync)
        begin
        // Latching the inputs
            PEncR <= PEnc;
            NEncR <= NEnc;
            CStepsR <= CSteps;
            DBStepsR <= DBSteps;
        end
        else
        begin
        // Keep the data
            PEncR <= PEncR;
            NEncR <= NEncR;
            CStepsR <= CStepsR;
            DBStepsR <= DBStepsR;
        end
    end

endmodule
```

```
// MODULE BELOW IS CURRENTLY UNUSED
// module AlignmentMux
/* Used to select the correct decoded output.
 * This module has a registered output.
 */
    // (
    // output DOut, // Selected PWM output
    // input Sel, // Mux selector (0: selects Lead, 1: selects Trail)
    // input SysClk, // Register clock
    // input Lead, Trail // Leading and trailing-edge decoded stream
    // );

    // reg DOutR;
    // assign DOut = DOutR;

    // always@(posedge SysClk)
        // case (Sel)
            // 0: DoutR <= Lead;
            // 1: DoutR <= Trail;
            // default DoutR<=1'b0;
        // endcase

// endmodule

module ClampLUT
/* Converts 00 in 11 to activate the pulser clamp.
 * This module has a registered output.
 */
    (
    output OutP, OutN,
    input InP, InN,
    input SysClk
    );

    reg[1:0] OutReg;
    assign OutP = OutReg[0];
    assign OutN = OutReg[1];

    always@(posedge SysClk)
        case ({InN, InP})
            0: OutReg<='1; // Enables active clamp
            1: OutReg<=2'b01;
            2: OutReg<=2'b10;
            3: OutReg<=2'b00; // Leaves pulser in Hi-Z
            default: OutReg<='1;
        endcase

endmodule

module UDCounter
/* Synchronous up/down-counter with dual load ports
```

```
150 * Counter will load the inputs upon wrap-around!
    * NOTE: for proper operation counter should be loaded with
    * either 1 on up or PWE on down.
    */
       #(parameter Cws=8)
155    (
       output[Cws-1:0] COut,
       output LSync, // Load sync signal
       input[Cws-1:0] LoadUp, // Value loaded when counting up
       input[Cws-1:0] LoadDn, // Value loaded when counting down
160    input En, Load, UDb /* Counts up when 1, down otherwise */,
       input SysClk
       );

       reg[Cws-1:0] CxR; // Counter register
165    assign COut = CxR;

       reg LSyncR; // Load sync register
       assign LSync = LSyncR;

170    always@(posedge SysClk)
       begin
           if (Load) // Load dominates over En
           begin
               LSyncR <= 1'b1;
175            if (UDb) // Load counter from different sources
                   CxR <= LoadUp;
               else
                   CxR <= LoadDn;
           end
180        else if (En)
           begin
               LSyncR <= 1'b0; // Clear Lsync
               if (UDb) // Counting up
               begin
185                if (CxR == '1) // Counting over
                       CxR <= LoadUp;
                   else
                       CxR <= CxR+1'b1;
               end
190            else // Counting down
               begin
                   if (CxR == {{(Cws-1){1'b0}},1'b1}) // Counting over at 1
                       if (LoadDn == '0)
                           CxR <= {{(Cws-1){1'b0}},1'b1}; // This is done because
                                LoadDn could be 0
195                    else
                           CxR <= LoadDn; // If LoadDn >= 1 it can be loaded
                   else
                       CxR <= CxR-1'b1;
               end
```

```
        end
        else // Retain current state
        begin
            CxR <= CxR;
            LSyncR <= 1'b0; // Clear Lsync
        end
    end

endmodule

module CmpDec
/* Pulse width decoder
 * Assumptions: UpCounter starts from 1 and DnCounter
 * starts from PWE. Leading or trailing output is decided by
 * the direction of the counter.
 * This module is purely combinatorial, expecting registers
 * in parent module.
 */
    #(parameter Cws=8)
    (
    output PWDec,
    input[Cws-1:0] Enc, // Encoded word
    input[Cws-1:0] Cnt // Input form counter
    );

    reg PWDecR;
    assign PWDec = PWDecR;

    always@(Enc, Cnt)
    if (Cnt<=Enc)
        PWDecR = 1'b1;
    else
        PWDecR = 1'b0;

endmodule
```

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Project Pandora was funded
by Texas Instruments Inc.

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This document was typeset using the typographical look-and-feel `classicthesis` developed by André Miede (`https://bitbucket.org/amiede/classicthesis/`).

Final version as of January 18, 2018.