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DESIGN OF A DEMULTIPLEXER FOR A REGENERATIVE SATELLITE

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In this paper the design of a demultiplexer for the on-board interfacing of FDMA and TDMA links in a regenerative satellite is presented. In particular, we focus here only on per-channel structure based on the analytic signal method that allows a high modular and flexible implementation. A theoretical analysis and computer simulation are reported in order to evaluate the performance degradation due to the finite arithmetic implementation of the demultiplexer.

1. INTRODUCTION

The development of space communications has required a new generation of satellites. In the past, satellites have operated using analog modulation of the carrier, and accessing the satellite was accomplished with frequency-division multiple access (FDMA). The satellite simply translated the carrier frequency and retransmitted the signal in a wide beam covering a large geographic area. Today the new systems employ time-division multiple access (TDMA), new efficient modulation techniques, multiple beam antennas, and on-board processing for a higher system efficiency.

The on-board signal processing offers several advantages to satellite communication systems. A typical and interesting feature is the separation of the uplinks and downlinks, thus allowing their separate and independent optimization. For example, in many applications, such as mobile communication services, the use of uplink FDMA techniques (with the inherent low-cost earth stations) and downlink TDMA techniques (that can fully exploit the satellite transponder output power without intermodulation) is an attractive solution. However, the feasibility of this approach depends on efficient means of translating between the two multiple access formats on board the satellite. The on-board system implementation complexity (including the VLSI design) and power consumption are, of course, of primary concern.

The on-board processing system receives an input FDMA signal and supplies an output TDMA signal; therefore, it must accomplish the functions of the separation of each individual channel and of its demodulation. An appropriate name for the on-board processing system is the 'multicarrier demodulator' (MCD). Two main functions are implemented by a MCD: formerly the demultiplexing and consequently the demodulation. We focus here only on the digital demultiplexer (DEMUX), that is a signal processor for translating signals from FDM to TDM formats. The demodulation operation, following the DEMUX, can be performed by any of the available implementation of digital demodulators.

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The DEMUX design has been carried out by assuming the QPSK modulation, because it is well known that this modulation technique permits the achievement of a good trade-off between bandwidth and performance degradation. However, the DEMUX design can also be carried out for different modulation techniques suitable for satellite communications such as, for example, the MSK modulation. For the digital DEMUX design two basic approaches exist: the block methods [1] and the non-block methods [2]. The block methods require a FFT block processor while this is not used for the non-block methods. We focus here only on the non-block methods that allow a high modular and flexible implementation structure. The DEMUX design has been carried out in order to reduce the overall implementation complexity and includes the finite precision design. It has been carried out in particular aiming at its possible implementation by means of custom VLSI digital circuits.

2. ANALYTIC SIGNAL APPROACH FOR THE DEMUX

We consider the analytic signal approach for the DEMUX implementation [2]. This approach is a per-channel method that avoids any digital product modulator and any block processor. It has the specific feature to relax the filter specifications, thus achieving a lower implementation complexity with respect to other per-channel approaches. Further, the analytic signal approach directly leads to a per-channel and high modular structure; this structure is directly matched to the per-channel implementation of the demodulators. Therefore, a certain degree of integration of the DEMUX and DEMOD functions is conceivable. Another advantage of the analytic signal approach is its high flexibility: differently from the other methods, in the case that some specific applications should benefit from the unequal channel bandwidth, the analytic signal structure could vary on demand the bandwidth

assigned to each channel, simply by switching to a suitable new set of DEMUX parameters. The principle of operation of the analytic signal method is illustrated in [2] and will be briefly recalled in the following.

The structure of the DEMUX according to the analytic signal method is shown in Fig. 1 [2],[4]. The FDM input signal is sampled, according to the sampling theorem [3], at the high-rate frequency $f_u = 1/T_u$ (uplink) and processed in order to obtain N_c TDM digital signals, each sampled at the low-rate frequency $f_d = 1/T_d$ (downlink), N_c being the number of multiplexed channels. In Fig. 1, $H_i(fT_u)$, $H_i'(fT_u)$ represent the conjugate symmetric and antisymmetric parts, respectively, of the high-rate complex bandpass filter $\bar{H}_i(fT_u)$ which can be regarded as a frequency translated version of a low-pass prototype $\bar{H}(fT_u)$ such that [2]:

$$(1)\quad \bar{H}_i(fT_u)=H_i(fT_u)+jH'(fT_u)=\bar{H}[2\pi(f-iW-W/2)T_u]$$

where W is the channel spacing. In the same figure, $G_i(fT_d)$ and $G_i'(fT_d)$ represent the conjugate symmetric and antisymmetric parts, respectively, of the complex low-rate filter $\bar{G}_i(fT_d)$ which can be defined as [2]:

$$(2)\quad \bar{G}_i(fT_d)=G_i(fT_d)+jG_i'(fT_d)=\bar{G}\{[f-(-1)^i W/2]T_d\}$$

Thus, each filter $\bar{G}_i(fT_d)$ is related, according to eq. (2), to a low-pass prototype. It can be noted from eq. (2) that the number of different filters $G(fT_d)$ is actually two: one for the odd channels and the other for the even channels. Taking into account eqs. (2) and (3), we have in the frequency domain [2]:

$$(3)\quad X_i(fT_d)=S(fT_d+i\pi)[H_i(fT_d+i\pi)\cdot G_i(fT_d+i\pi) - H_i'(fT_d+i\pi)\cdot G_i'(fT_d+i\pi)]/N_c$$

according to the implementation structure shown in Fig. 1. It must be noted that a decimation factor equal to the number N_c of multiplexed channels is involved.

3. FINITE ARITHMETIC IMPLEMENTATION EFFECTS

The implementation of a digital signal processing system necessarily requires a finite arithmetic. Although it is possible to conceive and actually implement floating-point arithmetic for digital signal processing systems, however it is deemed that the fixed-point arithmetic implementation will still represent the more convenient solution in the near to medium term. Thus, we consider here only the effects of a fixed-point finite arithmetic implementation.

The error sources derived from the finite length of the digital registers are: a) quantization of the input signal; b) quantization of the filter coefficients; and c) rounding of the multiplication operations. For the first source of error the sampled input signal is quantized in amplitude in order to be represented by a set of numbers in binary form. We suppose that the input signal will be modeled as a random Gaussian signal. This assumption comes from the consideration that the input FDMA signal is the sum of several independent signals. Under this hypothesis the signal-to-quantization noise ratio SNR_q can be expressed in dB as [3]:

$$(4)\quad (SNR)_{dB} = 6.02\, b_q - 7.27 \text{ dB}$$

where b_q is the number of bits employed for the quantization of the input signal. Assuming that the dynamic range of the analog-to-digital converter (A/D) is in the range $\pm$ 1, we suppose that an Automatic Gain Control (AGC) is used in order to constrain the output signal (input to A/D) within the range $\pm$ 1. Further, we shall assume that the output signal from any filter is in the range $\pm$ 1. This can be guaranteed by a suitable scaling of the digital filter coefficients (included in the filter design and implementation).

For the second source of error the minimum wordlengths of the filter coefficients are determined by computer rounding in order to guarantee that they still verify the required filtering specifications. For the third source of error it must be observed that a FIR implementation is the most suitable one for the digital filters of Fig. 1. A FIR filter implemented by P multiplications each rounded to b_m bits produces an output noise error with mean power equal to that introduced by an output quantization to b_a bits, according to:

$$(5)\quad P\,\frac{2^{-2b_m}}{3} = \frac{2^{-2b_a}}{3}$$

Let us suppose to have determined (through analytic or simulation tools) the number of bits b_a required for the output signal quantization to achieve some specified performance, then the number of bits b_m for the multiplication roundings inside the filter is determined as:

$$(6)\quad b_m = b_a + \lceil (\log_2 P)/2 \rceil$$

where $\lceil x \rceil$ denotes the minimum integer greater than or equal to x.

The block diagram of the DEMUX according to the analytic signal approach and including the multiplication rounding model previously described is reported in Fig. 2. In this figure, S_i denotes the power of the input FDM signal assumed uniformly distributed among N_c channels, N_i is the mean power of the noise introduced in the uplink and N_q is the quantization noise power due to the input A/D conversion, both supposed white, Gaussian and uniformly distributed among the N_c channels. The term $S_t/2$ represents the power of the signals at the output of the filters $H_i(fT_u)$, $H_i'(fT_u)$ and also at the output of the filters $G(fT_d)$, $G'(fT_d)$ under the assumption that they are of the all-pass type. In the same figure, S_t is the power of the signal at the i-th output of the DEMUX, N_t is the overall noise power for each DEMUX output which will be defined in the following, N_{a_1} denotes the noise

power due to the finite arithmetic implementation of the filters $H_i(fT_u)$, $H_i'(fT_u)$ due to the quantization of their outputs at b_{a1} bits. In the same way, N_{a2} represents the power of the noise introduced by the finite arithmetic implementation of the filters $G_i(fT_d)$, $G_i'(fT_d)$.

In order to evaluate the signal-to-noise ratio SNR_t at each DEMUX output, in addition to the contributions previously considered, the effects of the decimation process must also be included. The decimation process gives rise to a noise contribution at each DEMUX output independent of the other disturbances with mean power given by [4]:

$$(7) \quad N_d = S_i \, \delta_2^2$$

where δ_2^2 is the maximum acceptable squared out-of-band ripple and assuming $N_C >> 1$. It can be noted that eq. (7) is derived according to a worst-case analysis because we have assumed the out-of-band ripple constant in the filtering bandwidth and equal to its maximum values δ_2.

Now, under the hypothesis that the filters $G_i(fT_d)$, $G_i'(fT_d)$ are of the all-pass type, by setting $N_a = N_{a1} + N_{a2}$ and assuming $N_{a1} = N_{a2}$ (equal quantization bits at the output of the high-rate and low-rate digital filters), the overall noise power N_t at any output of the DEMUX is given by:

$$(8) \quad N_t = \frac{N_i}{N_C} + \frac{N_q}{N_C} + S_i \, \delta_2^2 + 2 N_a$$

Thus, the signal-to-noise ratio at each DEMUX output is [4]:

$$(9) \quad \frac{1}{SNR_t} = \frac{1}{S_t/N_t} = \frac{1}{S_i/N_i} + \frac{1}{S_i/N_q} + \frac{2}{S_i/N_a} + N_C \, \delta_2^2$$

where we have assumed $S_t = \frac{S_i}{N_C}$.

Thus, the finite arithmetic wordlengths at each point of the DEMUX structure must be determined in order to introduce an overall degradation with respect to the input signal-to-noise ratio smaller than a specified value.

4. DESIGN RESULTS

In this section, the design results of the demultiplexer according to the analytic signal methods are presented for a QPSK modulation technique with a data rate R = 2.048 Mb/s. The number of input channels N_C is assumed equal to 8 and the filtering bandwidth B equal to 572.3 [4]. The channel spacing W is chosen equal to 1.536 MHz in order to minimize the overall numbers of multiplications required per second and per channel, and to guarantee an integer number of samples per symbol (3 samples/symbol). Under these assumptions, according to the procedure described in [4], the filtering specifications are the following:

- maximum acceptable in band-ripple: $\delta_1 = 4.84 \cdot 10^{-3}$ (max. freq. amplitude 0.042 dB);
- minimum out-of-band attenuation: $\delta_2 = 6.31 \cdot 10^{-3}$ (-44 dB).

It must be pointed out that these specifications represent the overall filtering requirements. Thus, the high-rate and low-rate low-pass prototypes have been designed according to different specifications [4]: their cascade must satisfy the overall filtering specifications reported herein.

The design of these digital filters has been carried out by using the Equiripple method [5]. The filtering specifications are satisfied by employing FIR digital filters with a number of coefficients equal to 35 and 23 for the high-rate and low-rate low-pass prototypes, respectively. The overall number of multiplications required per channel and per second [4] is thus equal to 124.42 Mmults/s/ch. The finite arithmetic design is carried out according to that outlined in sect. 3. The number of bits used for the quantization of the filter coefficients is derived through a computer rounding in order to still verify the filter coefficients. The other finite arithmetic wordlengths are chosen, according to eq. (9), in order to introduce an overall degradation less than 0.2 dB with respect to the input signal-to-noise ratio which guarantees an ideal bit-error rate equal to 10^{-9}.

The finite arithmetic wordlengths that result for the demultiplexer design are reported in Tab. 1. The results obtained through the theoretical analysis explained in sect. 3 and the computer simulation of the demultiplexer are reported in Tab. 2. In this table the input signal-to-noise ratio SNR_i is derived taking into account the equivalent noise bandwidth B_n=1.454 MHz of the actually designed filters, and the signal-to-noise ratio SNR_t is evaluated at each output of the DEMUX. In Fig. 3 the degradations introduced by the finite arithmetic implementation are reported as a function of the input signal energy to noise density ratio. It can be noted that the results obtained through computer simulation (simulation results) show a satisfactory agreement with those obtained through the theoretical analysis (analytic results), that represents a worst-case analysis.

5. CONCLUSIONS

In this paper a complete digital DEMUX design suitable for on-board interfacing FDMA and TDMA links has been presented. We have focused only on the analytic signal approach as this design method leads to a per-channel and high modular structure; the analytic signal approach has the advantage of a high flexibility, i.e. the resulting structure could vary on demand the bandwidth assigned to each channel simply by switching to a suitable new set of system parameters, and of more relaxed finite arithmetic wordlengths with respect to the other DEMUX approaches (i.e. block methods). In conclusion, the DEMUX design described herein represents an appropriate solution for the on-board processing system interfacing FDMA and TDMA links; in particular, it has been carried out aiming at its possible implementation by means of custom VLSI digital circuits.

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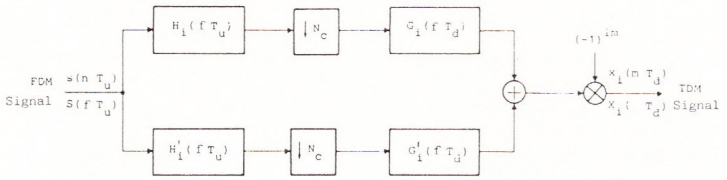

Fig. 1

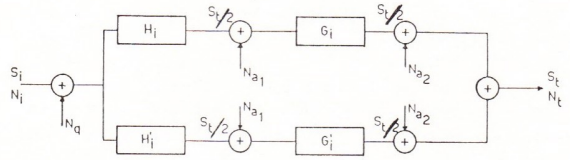

Fig. 2

INPUT SIGNAL QUANTIZATION	FILTERS $\bar{H}(fT_u)$			FILTERS $\bar{G}(fT_d)$		
b_q	b_c	b_m	b_a	b_c	b_a	b_a
8	12	11	8	11	11	8

TAB. 1 - 2.048 Mb/s finite Arithmetic Design.
Analytic Signal Approach.
b_q - Input signal wordlength.
b_c - Filter coefficient wordlength.
b_m - Filter arithmetic wordlength.
b_a - Output filter wordlength.

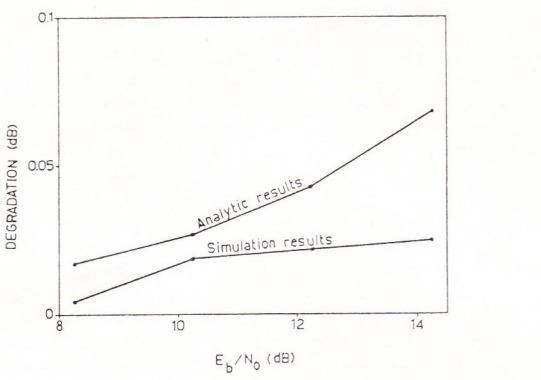

Fig. 3

E_b/N_o (dB)	8.25		10.25		12.25		14.25	
	A	S	A	S	A	S	A	S
SNR_i (dB) (in the DEMUX noise filter bandwidth)	9.74	9.846	11.74	11.846	13.74	13.846	15.74	15.846
SNR_t (dB) (at the DEMUX output)	9.723	9.842	11.713	11.827	13.697	13.825	15.672	15.821
DEGRADATION (dB)	0.017	0.004	0.027	0.019	0.043	0.021	0.068	0.025

TAB. 2 - 2.048 Mb/s finite Arithmetic Design.
A - Analytic results.
S - Simulation results.
B_n - 1.454 MHz (noise filter bandwidth).