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TECHNIQUES AND TECHNOLOGIES FOR MULTICARRIER DEMODULATION IN FDMA/TDM SATELLITE SYSTEMS

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ABSTRACT
Regenerative, On-board Processing FDMA/TDM payloads have been recently proposed as valid candidates for user-oriented satellite systems.
Both Business Traffic for Fixed Services (e.g. INTELSAT Business Services, IBS) and Mobile Satellite Systems can potentially take advantages of the peculiarities of such payloads, which substantially require MultiCarrier Demodulation (MCD) of the uplink FDMA carriers to recover the individual modulating streams, which are in turn TDM-formatted to modulate a unique downlink carrier.
The present paper expands on the most suitable techniques/technologies to implement on-board MCD, also providing some recent data on present hardware performance and time-scale for technologies maturity.

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1. INTRODUCTION

One of the most attractive architectures for business-services satellite systems recently proposed envisages different access methods in the two links, i.e. Frequency Division Multiple Access in the uplink and Time Division Multiplexing in the downlink (Refs. 1-to-3).
In this way, the user uplink RF power requirements are proportional to the individual bandwidths (differently from TDMA which requires power levels proportional to the transponder bandwidth), and, to some extent, network synchronization procedures are not requested.
In the downlink, TDM permits the on-board High Power Amplifier (HPA) to be saturated or slightly backed-off, due to absence of multicarrier intermodulation.
Such an architecture, therefore, attempts to optimize the system RF power resources, however requiring non-trivial access format conversion on-board from FDMA to TDM.
The heart of the (regenerative) payload is then composed by a "MultiCarrier" Demodulator (MCD), which recovers the individual modulating sequences of the (N) FDMA uplink carriers; a subsequent TDM formatter builds-up a higher data rate information stream to modulate a unique downlink carrier (see fig. 1).
Some kind of network synchronization is anyway requested to keep reasonable the MCD complexity.
This requirements is even more stringent in the presence of a high number of low data rate carriers, whose (clock) misalignment at the satellite input may drastically complicate the processing payload, and in limit cases even prevent any reasonable implementation.
A typical INTELSAT-EUTELSAT 120-Mbps transponder (83.3 MHz gros bandwidth) may support several hundred carriers, and the situation is even heavier in Mobile Services, where the transmission rates are of the order of a few Kbps.
Hence, synchronization problems may arise, and should be solved by using proper techniques (Refs. 4 and 6).
In the following sections the most attractive solutions to the MCD problems (with emphasis on the Demultiplexing section) will be reviewed relatively to IBS data rates, which, in the presence of 6.7%-data overhead and rate-1/2 convolutional encoding (3-bit soft-decision Viterbi decoding) and QPSK modulation, range from 137 Kbps to 4.369 Mbps.
In particular, the paper will expand on the following approaches to the MCD implementation problem:

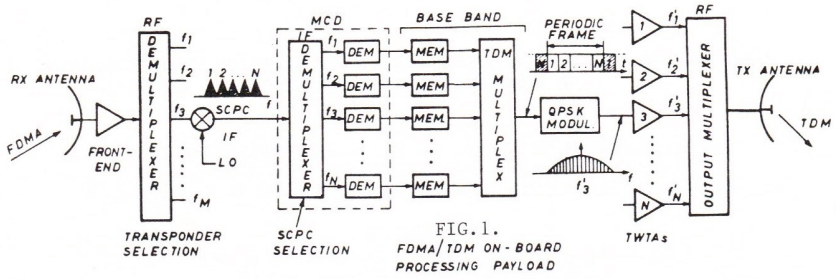
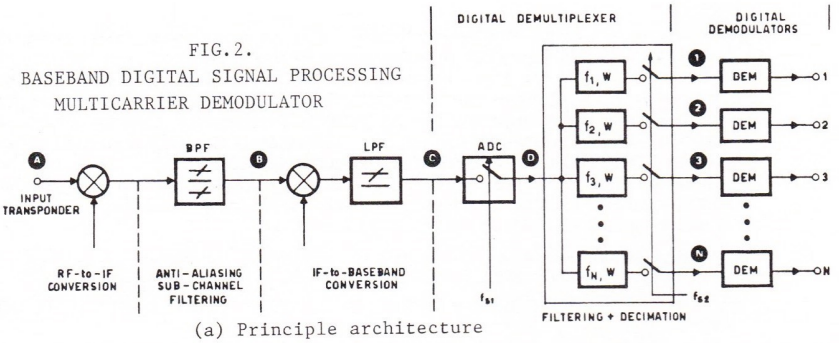
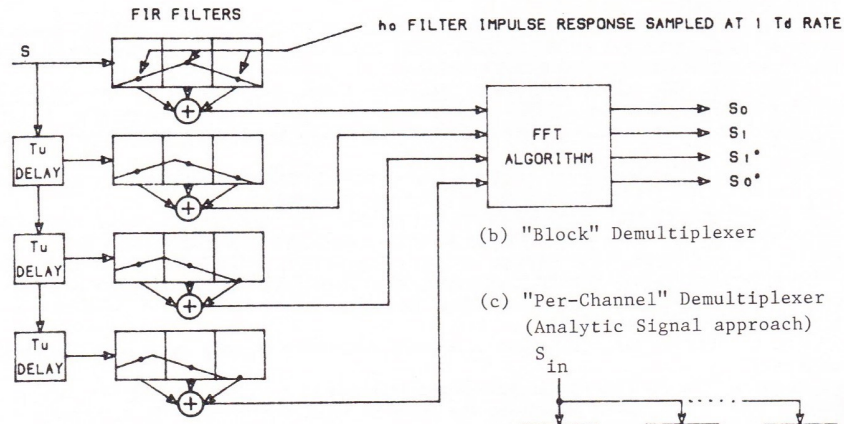


FIG. 1.
FDMA/TDM ON-BOARD PROCESSING PAYLOAD

FIG. 2.
BASEBAND DIGITAL SIGNAL PROCESSING MULTICARRIER DEMODULATOR

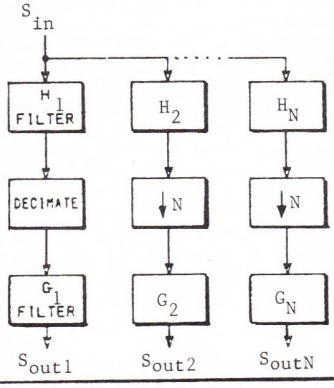


(a) Principle architecture

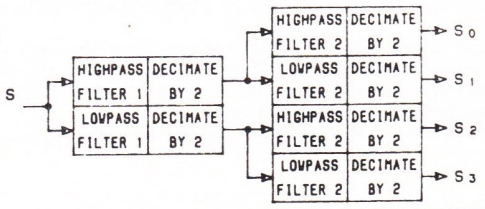


(b) "Block" Demultiplexer

(c) "Per-Channel" Demultiplexer (Analytic Signal approach)



(d) "Multistage" Demultiplexer (4 channels)



- Baseband Processing
- Chirp Fourier Transform (CFT) SAW Processing
- Integrated Optics

2. BASEBAND PROCESSING

2.1. Digital Demultiplexer

From a general point of view, the demultiplexing of uplink SCPCs (to be subsequently demodulated) can be implemented using three different approaches: (i) per-channel, (ii) block and (iii) multistage, as shown in Fig. 2.

The per-channel method performs the demultiplexing operation essentially by means of a bank of bandpass filters.

Selection of each input signal and its translation to a low-frequency band are achieved by a compound operation of digital filtering and decimation (i.e. decrease of the signal sampling rate).

The block method implements the demultiplexing by using a set of digital filters ("Polyphase" Network) followed by a "block" processor - usually of the FFT type - that processes the output signals from the digital filters altogether.

This procedure of processing the input FDMA signal to obtain an output TDM one hystorically derives from studies on "Transmultiplexers" (Refs. 8, 9), which were originally conceived for the inverse transformation TDM-FDM, to transmit PCM (time-division) signals through analog (FDM) channels.

The multistage method can be considered as a binary tree of two-channel demultiplexers. Each demultiplexing stage performs a lowpass and a highpass filtering with subsequent decimation by a factor of two.

In the following we will briefly summarize the main characteristics and performance of the three approaches.

(i) Per-channel methods

Within the class of per-channel methods, an effective solution from the implementation complexity point of view is represented by the Analytic Signal (AS) approach (Ref. 7).

A specific feature of the AS method is to greatly relax the filter specifications in terms of transition bandwidths, thus achieving a lower implementation complexity with respect to other per-channel approaches.

The implementation structure of the Analytic Signal method envisages a cascade of "H_i" and "G_i" digital filters separated by a decimator (by a factor N).

H_i are bandpass filters performing a rough selection of i-th channel (out of N input channels to the Demultiplexer), having passband and transition bandwidths approximately equal to the channel spacing. They operate at the input (high) sampling rate and supply the output at the low rate after decimation of the signal by a factor N.

The G_i filters, operating at the low sampling frequency, carry out the required additional filtering to select the channels and translate them to the proper low-frequency band after the output adder. The sign inversion of every other output sample for the odd channels (i odd) is necessary to get a non-inverted spectrum for those channels.

It should be noted that the AS method requires an excellent (ideally perfect) matching of the H and G filters frequency responses. Such a matching is obtained by designing complex (quadrature) filters whose "in-phase" branch is made up by the filters corresponding to the real part of the complex impulse response, whereas the "quadrature" branch includes the filters corresponding to the imaginary part.

Linear phase FIR filters are conveniently utilized in this kind of approach to avoid phase distorsions and obtain high implementation efficiency of digital multirate structures: as a matter of fact, decimation is achieved with FIR filters merely not computing the samples to be discarded (IIR filters, on the contrary, are computationally less effective, as they in any case compute all the samples included those to be discarded subsequently upon decimation).

The required number of multiplications-per-second and per-channel required by the Analytic Signal method has been derived in the frame of ESA/ESTEC Contract 6096/84/NL/GM ("Multicarrier Demodulator Design") and is given by:

$$M_{AS} = K_{AS} \times W^2 \left[W(N+4)-2B(N+2)\right] / \left[(W-2B)(W-B)\right] \qquad (1)$$

where:

- $K_{AS} = (2/3) \log \left[2/(10\,\delta_1\,\delta_2)\right]$
- N = number of demultiplexer input channels
- W = channel spacing

- B = one-side bandwidth of the signal spectrum
- δ_1 = pass band amplitude ripple
- δ_2 = shop band amplitude ripple

(ii) Block methods

As shown in fig. 2, a block processor consists of a bank of N FIR polyphase filters followed by a N-point FFT processor.
Both the filters and the FFT processor operate at the lower (output) sampling frequency, thus reducing the overall computational complexity.
The N channels to be demultiplexed should be a power of two, in order to fully exploit the advantages of FFT processor. In this case the overall number of real multiplications-per-second is given by (same reference):

$$M_{FFT} = 2W\left[L_{FT} + M_{FT}\right] \tag{2}$$

where:

$$L_{FT} = (4/3)\ N\ W \log\left[1/(10\delta_1\delta_2)\right] / (W - 2B) \tag{2'}$$

$$M_{FT} = 8\ W\ N\log_2 N \tag{2''}$$

(iii) Multistage method

As in the block method, the multistage method is rather attractive whenever the number N of the demultiplexer channels is a power of two. The implementation structure for N = 4 is shown in fig. 2. At each stage the signal spectrum is split down into a couple of sub-bands by half-band filters and decimated by a factor of two. After L stages, $2^L = N$ channel are obtained.
A peculiarity of the method is the possibility to use the same design for all the half-band filters. Assuming to employ complex filters, much relaxed specifications can be required, decreasing the computational complexity.
With the multistage method, the overall number of real multiplications per second has been derived in the frame of INTELSAT Contract INTEL-479 ("Low-bit Rate on-board Demultiplexing and Demodulation"), and is given by:

$$M_{MS} = (64/3)\ N \times W \log\left[1/(10\delta_1\delta_2)\right]\left[\log_2 N + 2B/(W - 2B)\right] \tag{3}$$

Equations (1), (2) and (3) allow to compare the complexities of the different demultiplexing methods.
For small values of N the difference in complexity - function of channel spacing, W, once the other parameters have been fixed - tends to vanish, while it may be relevant for large values of N.
An optimum value of W may be selected to minimize the computional complexity; however, a nearly optimum value of W is determined by trading-off such different factors as spectrum utilization and convenience of selecting an output (low) sampling frequency corresponding to an integer number of samples-per-symbol. In many cases a convenient choice turns out to be 3 samples/symbol, corresponding to a channel spacing W equal to 3/4 times the transmission bit rate.
From an implementation point of view, some considerations and conclusions can be drawn about the three approaches, based upon both theoretical features and results from the mentioned studies for ESA and INTELSAT:

(i) per-channel methods generally have higher computational complexity, smaller finite-precision arithmetic sensivity, greater flexibility, smaller control circuit complexity;

(ii) block methods have lower computational complexity, higher finite-precision arithmetic sensitivity, smaller flexibility, greater control circuit complexity;

(iii) multistage methods have computational complexity comparable with that of block methods, finite-precision arithmetic sensitivity and control circuit complexity comparable to per-channel methods, intermediate degree of flexibility.

On the basis of some obtained results, the finite-precision arithmetic implementation of the block methods generally require 2-to-3 bits more than the other methods, due to the greater finite-precision arithmetic sensitivity of the FFT block processor.
The control circuit complexity for the block method may be comparable with (or in some limit cases even greater than) the complexity of the computational part, although a custom VLSI implementation of the control part might remove this drawback.

Flexibility may be a critical issue for the demultiplexer.
In the IBS applications different transmission rates are foreseen from 137 Kbps to 4.369 Mbps and likely the Multicarrier Demodulator will have to operate on many of them during the satellite lifetime, to allow for reconfigurability of traffic pattern.
The transmission rates are in general multiple of the smallest one by factors as 2, 3, 5 and combinations of them. If we require the demultiplexer to operate at different rates for a fixed processed bandwidth the number of channels N is inversely proportional to the transmission rate. Thus we can observe that:

(i) block methods are able to operate only at a fixed value of N (i.e. number of points of the block processor), therefore a specialised demultiplexer is required for each individual transmission rate.

(ii) per-channel structures are well suited to variations of transmission rates and number of processed channels N: it is only required to vary the filter characteristics (i.e. coefficients) and decimation factor, using only the necessary (N) branches of the structure designed for the highest possible value of N (lowest data rate). Moreover, the per-channel methods allow to process channels with different transmission rates within the same demultiplexer, as the N paths are substantially independent.

(iii) multistage structures have an intermediate degree of flexibility, as it allows variations of the transmission data rates, although limited to powers of two.

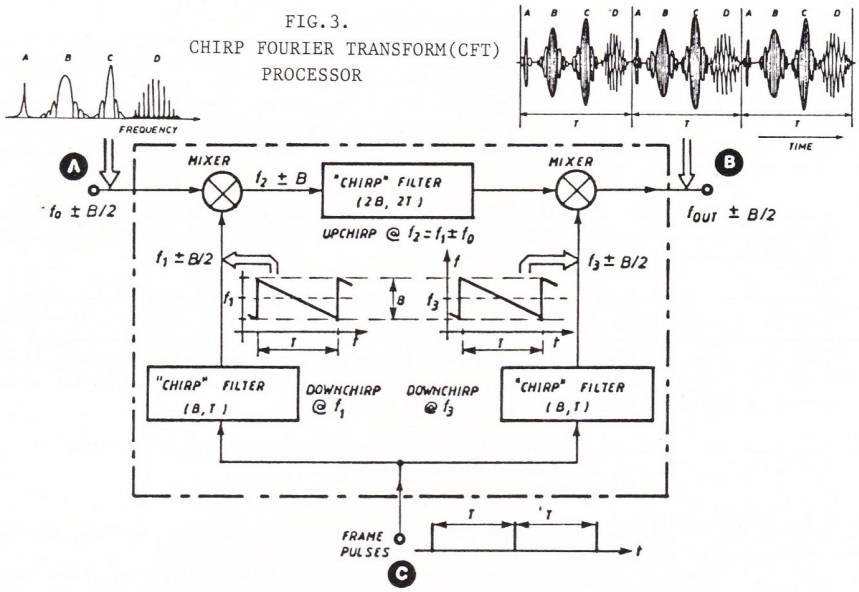
2.2. Digital Demodulator
The most demanding parts of the demodulator are the carrier and timing recovery circuits. Their choice depends on whether the MCD works in continuous or burst-mode.
For burst-mode operation (the most demanding), a suitable structure for the carrier recovery circuit could be the digital version of that proposed in Ref. 12 (Non-linear Phase estimation by Viterbi), that guarantees a fixed acquisition time.
Simulations have shown that 6 bit arithmetic is sufficient to obtain a carrier phase estimate very close to the floating-point implementation.
Ref. 13 proposes a suitable and simple digital timing recovery circuit, where only two samples-per-symbol are required. The algorithm is suitable for both acquisition and tracking modes of operation. For a QPSK modulated signal the error e(n) used to adjust a timing error corrector is evaluated for the n-th symbol according to:

$$e(n) = X_I\left(n-\frac{1}{2}\right)\left[X_I(n) - X_I(n-1)\right] + X_Q\left(n-\frac{1}{2}\right)\left[X_Q(n) - X_Q(n-1)\right] \qquad (4)$$

where X_I, X_Q are the in-phase and quadrature components of the signal.
Results obtained from theoretical analysis and computer simulation have shown that the degradations introduced by these two recovery circuits are of the order of a few tenths of dB.

3. CHIRP FOURIER TRANSFORM (CFT) IF PROCESSING
Having in mind the IBS transmission rates, the filter bank of fig. 1 might be in principle implemented via analog demultiplexers at a convenient IF, exploiting Surface Acoustic Wave (SAW) devices. Such devices exhibit rather peculiar compacteness and lightweight; however, the narrower the (useful and/or transition) bandwidth, the longer the filters are, being substantially composed by InterDigital Transducers (IDTs) etched on a piezoelectric crystal (Quartz, Lithium-Niobate,...), reproducing a sampled version of the filter impulse response (Ref. 14). Hence, practical implementation constraints prevent from envisaging large, narrowband SAW filter banks, as the previously mentioned compactness of the overall Demultiplexer would no longer hold true. This fact requires the user data rate to be around 1 Mpbs or more to use SAW demultiplexers, which in this configuration implement a kind of "per-channel" approach.
However, SAW devices can be effectively be employed in an alternative way to implement a "block" demultiplexer, as depicted in fig. 3 which exploits SAW spectrum analyzers implementing "Chirp" Fourier Transform (CFT). To build-up such a kind of Fourier Transformers, Linear Frequency Modulators (LFM or "Chirp" filters) may be used, having group delay which increases ("up-chirp") or decreases ("down-chirp") linearly with frequency.
A chirp filter or LFM can be suitably realized using SAW Reflective Array Compressor (RAC, Refs. 14 and 15).
Several RAC devices can be combined in a couple of configurations known as "Multiply-Convolve-Multiply" (M-C-M) and "Convolve-Multiply-Convolve" (C-M-C) chirp transformer. The frequencies within the useful bandwidth B - which is a requirement for the design of the Fourier Transformer, as it only can operate over a finite and limited frequency range - are displayed subsequently on a time division basis, the overall band B being converted into a time interval T.

FIG.3.
CHIRP FOURIER TRANSFORM(CFT)
PROCESSOR



If trains of T-spaced periodical pulses are provided at the input ports of the LFM(s) feeding the multiplier(s), such T-duration time intervals repeat periodically. Inside each time interval the time position of each frequency of the useful band is shifted proportionally to the absolute value of frequency.

Due to the necessary time-windowing to perform the Fourier transform, the displayed spectrum in the time position relative to the particular center frequency is actually the convolution between the true spectrum and a (sinx/x)-like function (Fourier transform of the time-window).

Thus, such an arrangement can be used as Multicarrier Demodulator with the addition of suitable baseband processing (tailored to deal with the selected modulation format) for data demodulation (including carrier and clock recovery).

It is, however, worthwhile to point out that the T frame duration should be chosen equal to (theoretically one but in practice) some multiple of symbol interval, and, in principle, in that interval all the SCPC waveforms should be time-aligned (i.e. the timing of the different uplink carriers made synchronized) in order to allow a short-term spectrum estimation consistent for each carrier in the T frame (one or more symbols) period.

However, some kind of arrangement (i.e. bank of filters at the CFT output to perform a kind of matched receiver by selecting the filter with highest output power) can relax or even remove the mentioned constraint; the subsequent carrier and clock recovery circuit, tailored to the particular CFT structure and modulation format, does not exhibit peculiar criticality, and is not addressed here.

However, the "block" demultiplexing operation does not easily allow for flexibility, as the SCPC data rate should be the same and kept fixed for each CFT demultipexer.

Moreover, a "ping-pong" configuration in generally envisaged to assure a 100%-duty cycle, as the convolution in the (2T, 2B) C_2 chirp filter causes a processing time within the CFT longer than T, not allowing in principle a continuous FDMA input signals demultiplexing.

Lastly, it has to be mentioned that practical BxT limitations constrain the T duration (i.e. one or more symbol periods) not to be higher than 50-100 usecs; the data rates able to be processed by the CFT demultiplexers, therefore, should not be lower than some (2 or 3) hundred Kbps. The upper bound, on the contrary, is totally compatible with user-oriented systems data rates (e.g. 4369 Kbps in the IBS).

4. INTEGRATED OPTICS (BRAGG CELLS)

Integrated Optics Signal Processing is probably one of the most promising techniques for 1990's implementation within a number of spacecraft electronic subsystems like mo-dems, demultiplexers, switching matrices, combiners,....

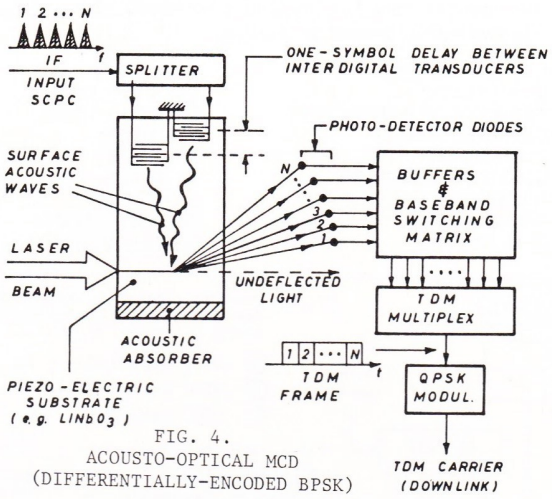


FIG. 4.
ACOUSTO-OPTICAL MCD
(DIFFERENTIALLY-ENCODED BPSK)

The level of integration can be really significant, although a number of technological issues have still to be solved, particularly in the field of temperature stability and frequency resolution.

Concerning our MCD application, one particularly simple method for demultiplexing a SCPC signal (where carrier recovery is not needed) is sketched in fig. 10 of Refs. 3 and 5, valid for differentially-encoded BPSK carriers(reproduced here in fig.4).

Owing to that scheme, demultiplexing and demodulation can be carried out on a single chip using a (modified) Integrated Acousto-Optical Spectrum Analyser (IAO-SA), which serves as a demultiplexing filter for the IF carrier. One optical detector per SCPC carrier would be used. To carry out the demodulation two SAW launchers are used, with a one bit or one symbol delay between the two launchers.

With no phase change between adjacent bits, the acoustic waves from each launcher will add and result in the light being deflected to the appropriate detector. If there is a 180-degree phase change, the two acoustic waves will destructively interfere (i.e. cancel) and there will be no deflection of the incident light to the appropriate detector. Thus, each detector will produce a signal only when there is no change of phase in its carrier (i.e. between adjacent bits). In this way the modified acousto-optical spectrum analizer can demultiplex (and demodulate) many carriers.

It has to be mentioned that, using this arrangements, the photo-detector diodes are actually facing a situation whereby the input signal is substantially ON-OFF keyed, avoiding some non-trivial problems of continuous light-to-electric voltage transduction if a coherent demodulation were envisaged.

Furthermore, the mentioned configuration, although handling differentially-encoded BPSK signals, is not exactly a differential (multicarrier) demodulator, as the recovered signal out-of-photodiodes does depend upon a number of different geometrical and electrical factors rather than merely phase difference between adjacent symbols.

Thus, the degradation figure with respect to coherent detection (about 0.5 dB and 2.3 dB in a binary and quaternary modulation, respectively) is not strictly valid here - probably it is too optimistic -, although a QPSK arrangement - implemented by doubling the fig. 7 circuit in such a way to build-up a quadrature receiver, each path processing a binary sequence at symbol rate - would be anyway preferred to save 3 dB of RF bandwidth.

The timing recovery is performed as usual, whilst the carrier recovery, as already pointed out, is not needed with the mentioned scheme.

Table 1 depicts some key parameters of Integrated Acousto-Optical MCD, as achievable with today technology.

Photodetector diodes are commonly available on the market in chip form with time-multiplexed serial output primarily in powers of two for FFT processors.

512-1024 diode chips are usual, the diode size being rather small such as the frequency resolution (i.e. angular spacing between any two adjacent detectors) is not limited by the diode dimension. However, it is difficult at the present status of technology to go below 100-200 KHz resolution (depending on temperature range and IF bandwidth), so that for the present application only data rates close to the Mbps range sound viable for IAO-SA realization.

TABLE 1 - TECHNICAL CHARACTERISTICS OF SOME BRAGG CELL DEVICES
(as desumed by present production)

CENTER FREQUENCY	0.5 - 3 GHz
BANDWIDTH	100 MHz - 2 GHz
FREQUENCY RESOLUTION	100 KHz - 3 MHz
DYNAMIC RANGE	40 - 70 dB
CROSSTALK	30 - 60 dB
LASER DIODE POWER	1 - 20 mW
DIODE SIZE	10 - 50μm
DIODE ARRAY	256 - 1024 diodes
SUBSTRATE	$LiNbO_3$, Quartz

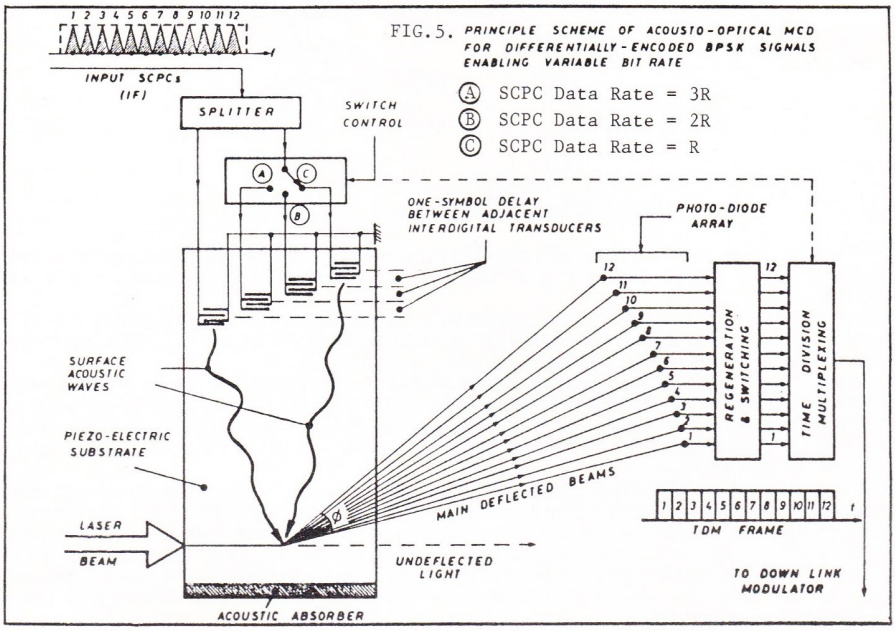


FIG. 5. PRINCIPLE SCHEME OF ACOUSTO-OPTICAL MCD FOR DIFFERENTIALLY-ENCODED BPSK SIGNALS ENABLING VARIABLE BIT RATE

Open points with this approach are temperature stability (primarily) and frequency resolution, whilst the instantaneous bandwidth is not a problem.
Reconfigurability might be achieved as outlined in fig. 5. An input Single Pole-Triple Throw (SP3T) switch selects one out of three (or more in principle) possible delays between pairs of Interdigital Transducers, allowing three possible data rates (R, 2R,3R) to be detected on different diodes (minimum data rate: all diodes interested; 2R data rate: alternate diodes; 3R data rate: one diode interested every three ones). More data rates can in principle be envisaged with similar arrangements.

5. COMPARISON AMONG TECHNOLOGIES - CONCLUSIONS

Table 2 resumes some relevant data on the discussed MCD technologies.
Baseband processing MCD: are capable of operate across the whole range of IBS data rates, whilst Acousto-Optics only seem applicable to the highest portion (several hundred Kbps); CFTs only exclude the lowest data rate.
Concerning hardware complexity IAO-MCD and semicustom CMOS assure the lowest weight and power consumption, although Integrated Optics permit the demultiplexing - and associate demodulation - of a higher number of channels within the same chip.
Development times are reasonable for each configuration.
In conclusion, MultiCarrier Demodulators have been shown to be implemented in several technologies, the relative complexities being such as to permit reasonable spacecraft implementation in mid 90's FDMA/TDM satellite systems.
More R+D activity is requested in this area, relevant to the development of user-oriented satellite systems.

TABLE 2. COMPARISON OF MCD TECHNOLOGIES.

Parameter / Technology	Availability	Transmission Rate Min (bit/s)	Transmission Rate Max (bit/s)	Maximum number of demultiplexed channels at rate Min	Maximum number of demultiplexed channels at rate Max	Physical parameters for a 4.3 Mbit/s MCD: Number of channels	powers consumption (W)	weight (kg)	Development time (months)
Digital Standard Chips	now	137K	4.3M	64	2	2	110	4.5	8
Advanced Digital Semicustom (CMOS)	within 10 years		20M		2	8	20	1	4
IAO-MCD	now	3.2M	4.3M	36	24	24	15	1.5	12 (*)
SAW CFT	now	270K	4.3M	60	22	22	40	7	12 (*)

(*)Extrapolated data from manufacturers

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